High-speed CMOS Logic Family

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DATA HANDBOOK

Philips Semiconductors



PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

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In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

High Speed CMOS Logic Family

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published late
Product specification	This data sheet contains final product specifications.
Limiting values	

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

INTRODUCTION

HIGH-SPEED CMOS (HCMOS) LOGIC IC FAMILY

The HCMOS family of logic ICs is manufactured using a self-aligning $3\,\mu m$ polycrystalline silicon-gate CMOS process combined with local oxidation of silicon (LOCOS). HCMOS ICs have the low power consumption, high immunity to input noise and wide operating temperature range of earlier silicon-gate CMOS circuits together with the high-speed and drive capability of bipolar, low-power Schottky TTL (LSTTL). They are also immune to latch-up and all types are available in DIL packages and in space-saving SO packages.

Many HCMOS circuits are pin-compatible with existing 54/74 LSTTL and HE4000B CMOS logic ICs. HCT types are ideal replacements for LSTTL. HCT types can also interface between TTL and CMOS ICs.

Three types of HCMOS ICs are available:

- 74HC: CMOS input switching levels 30%V_{CC} and 70%V_{CC} (typical switching threshold 50%V_{CC}), supply voltage 2 V to 6 V
- 74HCT: TTL input switching levels 0.8 V and 2 V (typical switching threshold 28%V_{CC}), supply voltage 4.5 V to 5.5 V
- 74HCU: CMOS input switching levels 20%V_{CC} and 80%V_{CC} (typical switching threshold 50%V_{CC}), supply voltage 2 V to 6 V; unbuffered to allow operation in the linear mode

The HCMOS family also includes several complex circuits for switching or multiplexing analog signals. These circuits have low crosstalk and feedthrough, and a very large frequency bandwidth.

There are also two FIFOs and three PLLs in the HCMOS range, of which one (HC/HCT297) is a fully digital type.

HCMOS FEATURES

- Very low power dissipation
- The switching levels of 74HC types are 30% and 70% of VCC
- DC noise margin of 74HC types three times that of TTL ICs
- \bullet Logic output levels 0.1 V and V_{CC} 0.1 V
- · All types, except 74HCU are fully buffered
- Typical gate propagation delay of 8 ns
- Can operate up to 60 MHz (typical)
- Fanout capability of 10 LSTTL loads (4 mA); this is increased to 15 LSTTL loads (6 mA) for types with bus-driver outputs
- Wide supply voltage range
- · Latch-up free
- Inputs protected against electrostatic discharge
- Functions and pinning identical to most popular LSTTL and CMOS HE4000B families
- Analog switching types operating up to 10 V
- Symmetrical output sourcing and sinking currents and equal output rise and fall times
- All types available in plastic SO packages for surface mounting and plastic DIL packages
- Choice of operating temperature range:
 -40 to +85 °C or -40 to +125 °C
- Approved to JEDEC standard No. 7A

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- ZAHCT: TTL input switching levels 0.8 V and 2 V (typical switching threshold 28%V_{CC}), supply voltage 4.5 V to 5.5 V
- 74HCU: CMOS input switching levels 20%V_{CC} and 80%V_{CC} (typical switching threshold 50%V_{CC}), supply voltage 2 V to 6 V; unbuffered to allow operation in the linear mode

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- Symmetrical output sourcing and sinking outrents and
- AB types available in plastic SO packages for surface mounting and plastic DIL packages
 - Choice of operating temperature range
 40 to + 85 °C or -40 to + 125 °C.
 - Approved to JEDEC standard No. 7A

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SELECTION GUIDE

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Functional index

Numerical index

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type no.	description	pins	classification	page
NAND/NOR gates/E	VOLUCIVE NOR goton			
HC/HCT00	quad 2-input NAND gate	14	SSI	107
HC/HCT02	quad 2-input NOR gate	14	SSI	HOHICTSELL
HC/HCT03	quad 2-input NAND gate (with open collector outputs)	VO1401-HO	SSI	115 @MOAOH
HC/HCT10	triple 3-input NAND gate	te 14 el W	OU-SI SSI	137 030AOH
HC/HCT20	dual 4-input NAND gate	14 195	SSI	153 TOHOH
HC/HCT27	triple 3-input NOR gate	14	SSI	161
HC/HCT30	8-input NAND gate	14	SSI	165
HC/HCT133	13-input NAND gate	14	SSI	263
HC/HCT4002	dual 4-input NOR gate	14	SSI	789
HC7266	quad 2-input EXCLUSIVE-NOR gate	14	SSI	1209
AND/OR/EXCLUSIVE	E-OR gates			
HC/HCT08	quad 2-input AND gate	8 14v goll	-cil e SSI leub	133 10 40 4
HC/HCT11	triple 3-input AND gate	14	SSI	141
HC/HCT21	dual 4-input AND gate	14	SSI	157 TOHOR
HC/HCT32	quad 2-input OR gate	14	SSI	169 TOHIOH
HC58	dual AND/OR gate	14	SSI	177
HC/HCT86	quad 2-input EXCLUSIVE-OR gate	14	SSI	207
HC/HCT4075	triple 3-input OR gate	14	SSI	961
Invertors/buffers/line	e drivers/level shifters			
HC/HCT04	hex invertor	114 1991	-diff e SSI I sub	121 TOHOH
HCU04	hex invertor (unbuffered)	14	SSI	125
HC/HCT125*	quad driver/line driver; 3-state; output enable active LOW	14 gol	MSI	243
HC/HCT126*	quad driver/line driver; 3-state; output enable active HIGH	14	MSI	249
HC/HCT240*	octal buffer/line driver; 3-state; inverting	20	MSI	485
HC/HCT241*	octal line driver; 3-state; output enable active LOW or HIGH	20 1 manager	MSI	491 ************************************
HC/HCT244*	octal line driver; 3-state; output enable active LOW	20	MSI	509 TOHOH
HC/HCT365*	hex buffer/line driver; 3-state	16	MSI	603
HC/HCT366*	hex buffer/line driver; 3-state; inverting	16	MSI	607 607
HC/HCT367*	hex buffer/line driver; 3-state	16	MSI	611
HC/HCT368*	hex buffer/line driver; 3-state; inverting	16	MSI	615

HIGH SPEED CMOS LOGIC FAMILY

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FUNCTIONAL INDEX				
type no. ⁹⁹⁸⁹	description	pins	classification	page on egyl
HC/HCT540*	octal buffer/line driver; 3-state;	1	PMSI BVIBULIOXE	669 MG/AM
701	inverting	etap GMAM		HOMETON
HC/HCT541*	octal buffer/line driver; 3-state		MSI DEUD	6750ТОНДОН
HC4049 am	hex inverting HIGH-to-LOW level shifter	16 д СИАИ :		8650TOHIOH
HC4050	hex HIGH-to-LOW level shifter		SSI elgid	871 гонон
HC/HCT7540*	octal Schmitt trigger buffer/line driver; 3-state; inverting	20 д ОИАИ	MSI laub	1269 ОНОН
HC/HCT7541*	octal Schmitt trigger buffer/line driver; 3-state	20 etsp 0	MSI ggi-8	1275
Flip-flops/latches/regis	ters 881			
789		NOR gate	dual 4-input	HC/HCT4002
HC/HCT73	dual JK flip-flop with reset; negative-edge trigger; supply on centre pins	exclustive	quad 2-Input	HOY266 181
HC/HCT74	dual D-type flip-flop with set and	14600 (104)	JucFFS baup	1870TOH\OH
HC/HC174	reset; positive-edge trigger		tuani-E elatt	
HC/HCT75	quad bistable transparent latch		SSI	193 гонон
HC/HCT107	dual JK flip-flop with reset;		FF S DEUD	217 стонон
110/1101101	negative-edge trigger			
HC/HCT109	dual JK flip-flop with set and reset; positive-edge trigger	16 JONA	OVGMA laub FF fuqui-S baup	223 223 223 223
HC/HCT112	dual JK flip-flop with reset; negative-edge trigger		Irible 3-inout FF ine drivers/level st	229 ATOHOH
HC/HCT173*	dual D-type flip-flop; positive-edge trigger; 3-state	16	MSI	нолното е68 непом
HC/HCT174	hex D-type flip-flop with reset; positive-edge trigger	16 ann ani		375 ТОНОН
HC/HCT175	quad D-type flip-flop with reset; positive-edge trigger	16 symb eni	MSI psup	381 гонон
HC/HCT259	8-bit addressable latch		MSI	545 стондон
HC/HCT273	octal D-type flip-flop with reset;	20	MSI	551 ***********************************
HC/HCT373*	octal D-type transparent latch; 3-state	20		619
HC/HCT374*	octal D-type flip-flop; positive edge trigger; 3-state	.20 ste-8 nev		625 STOHIOH
HC/HCT377	octal D-type flip-flop with data	20	MSI	631; СТОНДОН
HC/HCT533*	octal D-type transparent latch;	20	MSI Nevn	657
HC/HCT534*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting	20	MSI yen	663 СТОНОН
HC/HCT563*	octal D-type transparent latch; 3-state; inverting; bus oriented pin-out	20	MSI	681

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type no.	description	pins	classification	page
HC/HCT564*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting; bus oriented pin-out	20 mag na	MSI della servicione de	687 TOHOH
HC/HCT573*	octal D-type transparent latch; 3-state; bus oriented pin-out	20	MSI	693
HC/HCT574*	octal D-type flip-flop; positive-edge trigger; 3-state; bus oriented pin-out	20	MSI	699
HC/HCT670*	4 × 4 register file; 3-state	16	MSI	777 TOHOR
HC/HCT7030	9-bit × 64-word FIFO register; 3-state	28	LSI	1141
HC/HCT40105	4-bit × 16-word FIFO register; 3-state	16	MSI	1383
HC/HCT7403	4-bit × 64-word FIFO register; 3-state	16	LSI	1213
HC/HCT7404	5-bit × 64-word FIFO register; 3-state	18/20	LSI	1241
Shift registers				
HC/HCT164	8-bit serial in/parallel-out shift register	14 400 nw	MSI	351
HC/HCT165	8-bit serial in/parallel-out shift register	16	MSI	357
HC/HCT166	8-bit serial in/parallel-out shift register	16 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	MSI	363 TOHOR
HC/HCT194	4-bit bi-directional universal shift register	16	MSI	445
HC/HCT195	4-bit parallel access shift register	16	MSI	453
HC/HCT299*	8-bit universal shift register; 3-state	20	MSI	577
HC/HCT594	8-bit shift register with output register	16	MSI	711
HC/HCT595	8-bit serial-in/serial-or parallel-out shift register with output latches; 3-state	16 alu	MSI opeo	721 0904T0H0H
HC/HCT597	8-bit shift register with input flip-flops	16	MSI	733
HC/HCT4015	dual 4-bit serial-in/parallel-out shift register	16	MSI	793 TOHOH
HC/HCT4094	8-stage shift-and-store bus register	16	MSI	965 TOHOH
HC/HCT7597	8-bit shift register with input latches	16	MSI	1281
HC/HCT7731	quad 64-bit static shift register	16	LSI GOS	1291
HC/HCT40104*	4-bit bi-directional universal shift register; 3-state	16 000 m	MSI	1377
Arithmetic circuits				
HC/HCT85	4-bit magnitude comparator	16	MSI	199 TOHOH
HC/HCT181	4-bit arithmetic unit	24	MSI	387
HC/HCT182	look-ahead carry generator	16	MSI	401
HC/HCT280	9-bit odd/even parity generator/checker	14	MSI	557 557
HC/HCT283	4-bit binary full adder with fast carry	16	MSI	563
HC/HCT583	4-bit BCD full adder with fast carry	16	MSI	705

type no.	description	pins	classification	page
HC/HCT688	8-bit magnitude comparator	20	MSI	783 -on s
HC/HCT7080	16-bit odd/even parity sgbs-svi		oill somsi latoo	1189 TOH
	generator/checker			
Counters				
HC/HCT93	4-bit binary ripple counter	1/	MSI MSI	211
HC/HCT160	presettable synchronous BCD decade counter; assynchronous reset	16 golf	octal IRMoe flip-	321 _{8.TOM}
HC/HCT161	presettable synchronous 4-bit binary counter; assynchronous reset	16	MSI A X A	329 _{aTOH}
HC/HCT162	presettable synchronous BCD decade counter; synchronous reset	16	MSI MSI MO-4	335
HC/HCT163	presettable synchronous 4-bit binary counter; synchronous reset	16 OTIE	MSI MG-M	343 TOH
HC/HCT190	presettable synchronous BCD decade up/down counter	16	MSI	409 [54.1]
HC/HCT191	presettable synchronous 4-bit binary up/down counter	16 Includes	MSI NO 8	419 TOH
HC/HCT192	presettable synchronous BCD decade up/down counter	16	MSI	429
HC/HCT193	presettable synchronous 4-bit binary up/down counter	16	MSI	437
HC/HCT390	dual decade ripple counter	16	MSI	637
HC/HCT393	dual 4-bit binary ripple counter	14	MSI	643
HC/HCT4017	Johnson decade counter with 10 decoded outputs	16	MSI MSI BOTTHER BOTTHE	811
HC/HCT4020	14-stage binary ripple counter	16	MSI	819
HC/HCT4024	7-stage binary ripple counter	14	MSI	825
HC/HCT4040	12-stage binary ripple counter	16	MSI	831
HC/HCT4059	programmable divide-by-n counter	24	MSI	915
HC/HCT4060	14-stage binary ripple counter with oscillator	16, 002-1	MSIggs-8	925 ATOH
HC/HCT4510	BCD up-down counter	16	8-bit agent films tid-8	1027
HC/HCT4516	binary up/down counter	16	MSI	1059
HC/HCT4518	dual synchronous BCD counter	16	of all MSI raines	1069
HC/HCT4520	dual synchronous 4-bit binary counter	16	MSI	1075
НС/НСТ6323А	programmable ripple counter with oscillator; 3-state	8 _{samos}	MSI	1123
HC/HCT40102	8-stage synchronous BCD down	16	4-bit antimetic s ISM look-anesid cam	1359
HC/HCT40103	8-bit synchronous down counter	16 Vins	MSI NO TICLE	1367

type no. spag	description	pins	classification	page on equi
Multiplexers	14 551			HC/HCT4086
HC/HCT151	8-input multiplexer		MSI 15-8	291-ТОНЛОН
HC/HCT153	dual 4-input multiplexer	16 loillumeb	MSI	297
HC/HCT157	quad 2-input multiplexer		MSI DEUD	309
HC/HCT158	quad 2-input multiplexer; inverting	16 bn	WSI WSI	315
HC/HCT251			s lennerto-8	521
HC/HCT253*	8-input multiplexers; 3-state	16	MSI	
HC/HCT257*	dual 4-input multiplexer; 3-state		MSI	527 TOMOH
HC/HCT258	quad 2-input multiplexer; 3-state		MSIgnum	533
HC/HC1256	quad 2-input multiplexer; 3-state; inverting	16 olens lenn rexsigitiumeb	miple IZMan	539 TOHOH
HC/HCT354*	8-input multiplexer/register with transparent latches; 3-state	20	MSI	218 / 585 man 208
HC/HCT356*	8-input multiplexer/register; 3-state	20	MSI mevni	595
Decoders/demultiplexe	rs ISM At efet			
HC/HCT42	BCD to decimal decoder (1-of-10)			173STOHOH
HC/HCT137	3-to-8 line decoder/demultiplexer with			267 ТОНОН
	address latches			
HC/HCT138	3-to-8 line decoder/demultiplexer; inverting		MSI Islaa	275 8TO HOM
HC/HCT139	dual 2-to-4 line decoder/demultiplexer			281 ТОНОН
HC/HCT147		16		287
HC/HCT154	4-to-16 line decoder/demultiplexer		MSI SISS	303
HC/HCT237	3-to-8 line decoder/demultiplexer with	16 19 19 28 1	MSI Isioo	4718TOHOH
	a delega a la tala a a			
HC/HCT238	3-to-8 line decoder/demultiplexer	16	MSP 18-8	479
HC/HCT4511	BCD to 7-segment	16	MSI	21037 mmdo2
	latch/decoder/driver			
HC/HCT4514	4-to-16 line decoder/multiplexer with input latches	24.8 ОИАИ 1		1045 гонон
HC/HCT4515	4-to-16 line decoder/demultiplexer with input latches; inverting	24	MSI	1053
HC/HCT4543	DOD ISM	16	SchmilsM	1091
Switches/multiplexers/d	demultiplexers os enthrettud			
HC/HCT4016	quad bilateral switches		SSI Tavno	799
	(uncompensated switches)			
HC/HCT4051	8-channel analog	16	MSI TOVID	877
	multiplexer/demultiplexer			
HC/HCT4052	dual 4-channel analog	16 gamevai :		889
1353		chmitt Ingger		
HC/HCT4053	triple 2-channel analog multiplexer/demultiplexer	16	MSI) nisio	901

		nina	alaccification	naga 00 90VI
type no. 2029	description	pins	classification	page
HC/HCT4066	quad bilateral switches	14	SSI	935
HC/HCT4067	16-channel analog multiplexer/demultiplexer	24 haxalqitlum	MSI and S	947 ТОМОН
HC/HCT4316	quad bilateral switches with separate analog ground	16 religitum h	MSI	971 гонон
HC/HCT4351	8-channel analog multiplexer/demultiplexer with latch	20	MSI	985
HC/HCT4352	dual 4-channel analog multiplexer/demultiplexer with latch	20		999
HC/HCT4353	triple 2-channel analog multiplexer/demultiplexer with latch	20	MSI haup pamevai	1013 OHOH
Bus transceivers				
HC/HCT242*	guad bus transceiver; 3-state;	14 etapathaxalqı	MSI	497
HC/HCT243*	quad bus transceiver; 3-state	14	MSI	503
HC/HCT245*	octal bus transceiver; 3-state	20 0000 1877	MSI 008	515 TOHIOH
HC/HCT640*	octal bus transceiver; 3-state; inverting	20	MSI 201-8	741 TOMOH
HC/HCT643*	octal bus transceiver; 3-state; true/inverting	20	MSI	747 TOHOH
HC/HCT646*	octal bus transceiver/register; 3-state	24 0000 601	MSI	753 TOHOH
HC/HCT648*	octal bus transceiver/register;	24	MSI	761 TOHIOH
	3-state; inverting			
HC/HCT652	octal bus transceiver/register; 3-state	24	MSI 3-01-8	769
HC/HCT7245*	octal Schmitt-trigger transceiver; 3-state	20 290	MSI NOS	1205 888TOHAOH
Schmitt triggers				
HC/HCT14	hex inverting Schmitt trigger	14 nevnbins	SSI	145
HC/HCT132	quad 2-input NAND Schmitt trigger	114 Neboseb	SSI	255
HC7014	hex non-inverting precision Schmitt-trigger	14 unet/het/oneb	SSI entrol-ol-4	1137 616 TOHOH
HC/HCT7132	quad preciscion adjustable Schmitt-trigger/comparator with		MSI	1195
HC/HCT9014	nine wide Schmitt trigger buffer/line driver; inverting		MSI humabizaswata	1299
HC/HCT9015	nine wide Schmitt trigger buffer/line driver	20 five bata		1305
HC/HCT9114	nine wide Schmitt trigger buffer; open drain output; inverting	20 agricument		1347 3304 TOHNOR
HC/HCT9115	nine wide Schmitt trigger buffer; open drain output	20 algillumet		1353 6304TOHIOH

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type no.		description	pins	classification	page
One-shot mul	tivibrators				
HC/HCT123			quad 2-16 ¹⁰ quad 2-input	MSI	235
HC/HCT221		dual non-retriggerable monostable and multivibrator with reset	quad 2-161ut	MSI	459
HC/HCT423		dual retriggerable monostable multivibrator with reset	16 ym xarl	MSI	649
HC/HCT4538		dual retriggerable precision monostable multivibrator	unple 3-i Sur	MSI	1081
HC/HCT5555		programmable delay timer with oscillator	Inple 3-intended 16 intended in the control of the	MSI	1101
Miscellaneous	153				
HC/HCT297		digital phase-locked-loop filter	16	MSI	569
HC/HCT4046A	rar	phase-locked-loop with VCO	16 Salqui	MSI	837
HC/HCT7046A	681	phase-locked-loop with lock detector	16	MSI	1159
НС/НСТ9046А	173 173	PLL with bandgap controlled VCO	duad 2-inut 16 BOD to deal	MSI	1311

Note

^{*} Types with a bus-driver output stage.

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HC/HCT02	quad 2-input NOR gate	111	
HC/HCT03	quad 2-input NAND gate (with open collector outputs)	115	
HC/HCT04	hex invertor	121	
HCU04	hex invertor (unbuffered)	125	
HC/HCT08	quad 2-input AND gate	133	
HC/HCT10	triple 3-input NAND gate	137	
HC/HCT11	triple 3-input AND gate	141	
HC/HCT14	hex inverting Schmitt trigger	145	
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HC/HCT21	dual 4-input AND gate	157	
HC/HCT27	triple 3-input NOR gate	161	
HC/HCT30	8-input NAND gate	165	
HC/HCT32	quad 2-input OR gate	169	
HC/HCT42	BCD to decimal decoder (1-of-10)	173	
HC58	dual AND/OR gate	177	
HC/HCT73	dual JK flip-flop with reset; negative-edge trigger; supply on centre pins	181	
HC/HCT74	dual D-type flip-flop with set and reset; positive-edge trigger	187	
HC/HCT75	quad bistable transparent latch	193	
HC/HCT85	4-bit magnitude comparator	199	
HC/HCT86	quad 2-input EXCLUSIVE-OR gate	207	
НС/НСТ93	4-bit binary ripple counter	211	
HC/HCT107	dual JK flip-flop with reset; negative-edge trigger	217	
HC/HCT109	dual JK flip-flop with set and reset; positive-edge trigger	223	
HC/HCT112	dual JK flip-flop with reset; negative-edge trigger	229	
HC/HCT123	dual retriggerable monostable multivibrator with reset	235	
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HC/HCT241*		octal line driver; 3-state; output enable active LOW or HIGH	491	
HC/HCT242*		quad bus transceiver; 3-state; inverting	497	
HC/HCT243*		quad bus transceiver; 3-state	503	
HC/HCT244*		octal line driver; 3-state; output enable active LOW	509	
HC/HCT245*		octal bus transceiver; 3-state	515	
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HC/HCT258		quad 2-input multiplexer; 3-state; inverting	539	
HC/HCT259		8-bit addressable latch	545	
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HC/HCT273	octal D-type flip-flop with reset; positive-edge trigger	551	
HC/HCT280	9-bit odd/even parity generator/checker	557	
HC/HCT283	4-bit binary full adder with fast carry	563	
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HC/HCT354*	8-input multiplexer/register with transparent latches; 3-state	585	
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HC/HCT4002	dual 4-input NOR gate	789
HC/HCT4015	dual 4-bit serial-in/parallel-out shift register	793
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HC/HCT4017 808	Johnson decade counter with 10 decoded outputs	811
HC/HCT4020	14-stage binary ripple counter	819
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HC/HCT4040 TAST	12-stage binary ripple counter	831
HC/HCT4046A	phase-locked-loop with VCO	837
HC4049 8721	hex inverting HIGH-to-LOW level shifter	865
HC4050 1831	hex HIGH-to-LOW level shifter	871
HC/HCT4051 1981	8-channel analog multiplexer/demultiplexer	877
HC/HCT4052	pht/synf nevidual 4-channel analog multiplexer/demultiplexer	889
HC/HCT4053 8081	triple 2-channel analog multiplexer/demultiplexer	901
HC/HCT4059	programmable divide-by-n counter	915
HC/HCT4060	studiuo nisib 14-stage binary ripple counter with oscillator	925
HC/HCT4066	quad bilateral switches	935
HC/HCT4067	16-channel analog multiplexer/demultiplexer	947
HC/HCT4075	triple 3-input OR gate	961
HC/HCT4094	8-stage shift-and-store bus register	965
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HC/HCT4351	8-channel analog multiplexer/demultiplexer with latch	985
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HC/HCT4510	BCD up-down counter	1027
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HC/HCT4515	4-to-16 line decoder/demultiplexer with input latches; inverting	1053
HC/HCT4516	binary up/down counter	1059
HC/HCT4518	dual synchronous BCD counter	1069
HC/HCT4520	dual synchronous 4-bit binary counter	1075
HC/HCT4538	dual retriggerable precision monostable multivibrator	1081
HC/HCT4543	BCD to 7-segment latch/decoder/driver for LCDs	1091
HC/HCT5555	programmable delay timer with oscillator	1101
HC/HCT6323A	programmable ripple counter with oscillator; 3-state	1123
HC/HCT7014	hex non-inverting precision Schmitt-trigger	1137

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type no.		description				page	
HC/HCT7030		9-bit × 64-wor	d FIFO regist	ter; 3-state		1141	
HC/HCT7046A		phase-locked-	loop with loc	k detector		1159	
HC/HCT7080		16-bit odd/eve	n parity gene	erator/checker		1189	
HC/HCT7132		quad preciscio	on adjustable	Schmitt-trigge	er/comparator	1195	
		with output lat	ches; 3-state	quad bilate			
HC/HCT7245*		octal Schmitt-	rigger transc	eiver; 3-state		1205	
HC7266		quad 2-input 8	EXCLUSIVE-	NOR gate		1209	
HC/HCT7403		4-bit × 64-wor	d FIFO regist	ter; 3-state		1213	
HC/HCT7404		5-bit × 64-wor	d FIFO regist	ter; 3-state		1241	
HC/HCT7540*		octal Schmitt t	rigger buffer	/line driver; 3-s	state; inverting	1269	
HC/HCT7541*		octal Schmitt t	rigger buffer	/line driver; 3-s	state	1275	
HC/HCT7597		8-bit shift regis	ster with inpu	it latches		1281	
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HC/HCT9114		nine wide Sch	mitt trigger b	uffer; open dra	ain output;	1347	
		inverting					
HC/HCT9115		nine wide Sch	THEN IN DEPOSIT UP	1211 II 1251 (\$700 I		1353	
HC/HCT40102		8-stage synch	ronous BCD	down counter		1359	
HC/HCT40103		8-bit synchron	ous down co	unter		1367	
HC/HCT40104*	176	4-bit bi-direction	onal universa	al shift register	3-state	1377	
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Note

^{*} Types with a bus-driver output stage.

SELECTION GUIDE

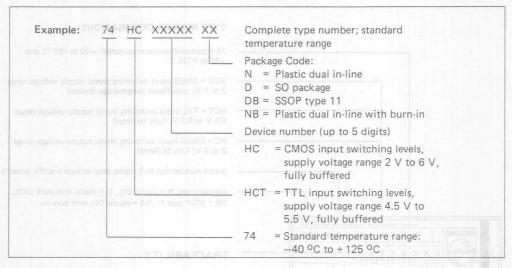
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SELECTION GUIDE

Marking information

Product status and definitions

HIGH-SPEED CMOS PRODUCTS PART NUMBERING SYSTEM



ORDERING

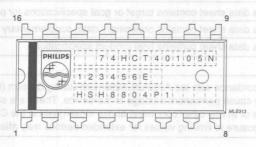
When ordering, please state:

- the quantity required;
- the package code (N = plastic DIL, D = plastic SO mini-pack, DB = SSOP type 11);
- screening class (B) if burn-in option is required (only applicable for NB package).

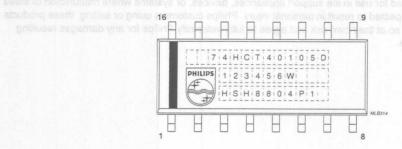
MARKING TYPE NUMBER DESIGNATIONS 74 = standard temperature range: -40 to +85 °C and -40 to +125 °C HCU = CMOS input switching levels; supply voltage range 2 to 6 V; unbuffered (single-stage devices) HCT = TTL input switching levels; supply voltage range 4.5 V to 5.5 V; fully buffered HC = CMOS input switching levels; supply voltage range 2 to 6 V; fully buffered device number (up to 5 digits; may include a suffix letter*) package code: N = plastic DIL, D = plastic mini-pack (SO), DB = SSOP type 11, NB = plastic DIL with burn-in. PHILIPS XXXXXXXXXXX XXXXXXXXX TRACEABILITY MLB315 PRODUCTION INFORMATION layout number and product status CECC quality assessment level date code factory identification

^{*} Example suffix "B": this type has bus driver output capability in contrast with the plain version.

MARKING EXAMPLES



Example of 16-lead dual in-line plastic package.



Example of 16-lead small-outline plastic SO mini-pack package.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.

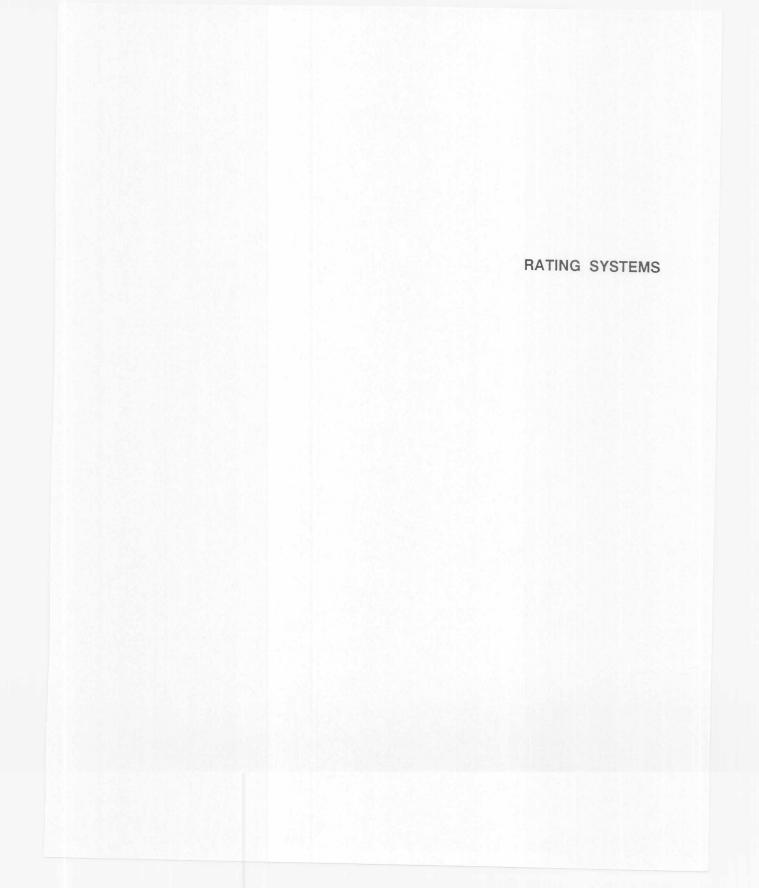
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.



RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED Electronic device.

An electronic tube or valve, transistor or other semiconductor device.

Note: This definition excludes inductors, capacitors, resistors and similar components.

Characteristic

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating

A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note: Limiting conditions may be either maxima or minima.

Rating system

The set of principles upon which ratings are established and which determine their interpretation.

Note: The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

RATING SYSTEMS

The rating systems described are those recontracted by the interna-

DEFINITIONS OF TERMS USED

An alectronic high or valve, translator or other semiconductor device.

Note: This definition excludes inductors, capacitors, resistors and

Characteristic

A characteristic is an inherent and measural the property of a device. Such a property may be electrical, mentantical, thermal, hydraulic, electro-magnetic, or nuclear, and dan be expressed as a velue for electro-magnetic or nuclear, and dan be expressed as a velue for recognized conditions. A characteristic may also be a set of released values, usually shown in gogitical form.

Boney electronic device

An electronic device whose characteristics have the published nonlinal values for the type. A Budgy electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Reting

A value which establishes alther a limiting capability or a limiting condition for an electronic device, it is determined for specified values of environment and operation, and may be stated in any suitable terms.

ota: Limiting conditions may be either mexima or minima.

Rating system

The set of principles upon which retings are established and which determine their intercretation.

Note: The rating specien indicates the division of responsibility between the device manufacturer and the securid designer, with the between of ensuring that the working conditions do not exceed the ratings.

ARSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and enumonmental conditions, applicable to any electronic device of a specified. Type as defined by its published date, which should not be exceeded under the worst property conditions.

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DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limining values of operating and arwinonmental conditions applicable to choosy electronic device of a specilied type as defined by its published data, and should not be expected

These values are obsern by the device manufacturer to provide acceptable serviceability of the device, taking exponeibility for the abuse, taking a changes in operating ordificing due to validations in the observer states of the electronic device under conscidention.

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DESIGN CENTRE RATING SYSTEM

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The equipment manufacturer should design so that, milially, no design centre, value for the intended service is exceeded with a cogety search of excelling equipment operating at the stated normal supply voltage.

USER GUIDE

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INTRODUCTION

The 74HC/HCT/HCU family is a comprehensive range of high-speed CMOS (HCMOS) integrated circuits. Whilst retaining all the advantages of CMOS technology - wide operating voltage range, very low power consumption, high input noise immunity and wide operating temperature range - these circuits have the high-speed and drive capabilities of low-power Schottky TTL (LSTTL). An extensive product range (most TTL functions and some devices from the successful HE40008 series: analog multiplexers, long time-constant multivibrators, phase-locked loops) and the aforementioned performance open new avenues in system design.

For comparison, the key performance parameters of HCMOS are shown with those of other technologies in Table 1. The propagation delay of metal-gate CMOS ruled out CMOS for many applications until the arrival of our HE4000B series. Now, our $3\mu m$ gate HCMOS technology has a speed comparable to LSTTL while retaining the important CMOS qualities, see Fig.1.

Table 2 compares the operating characteristics of the 74HC and 74HCT IC types with those of LSTTL in more

detail. 74HC and 74HCT devices are ideal for use in new equipment designs and, as alternatives to TTL devices, in existing designs. The 74HCT circuits which are direct replacements for LSTTL circuits also enhance performance in many respects.

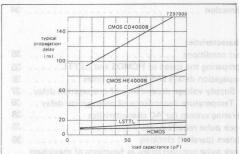


Fig. 1 Propagation delay as a function of load capatance; V_{CC} = 5 V, T_{amb} = 25 °C.

Table 1 Comparison of CMOS and TTL technologies; supply voltage V_{CC} = 5 V; ambient temperature T_{amb} = 25 °C; load capacitance C_L = 15 pF

	technology	HCMOS	metal gate CMOS	standard TTL	low-power Schottky TTL	Schottky TTL	advanced low-power Schottky TTL	advanced Schottky TTL	Fairchild advanced Schottky TTL
parameter	family	74HC	4000 CD HE	74	74LS	74S	74ALS	74AS	74F
Power dis	sipation, typ. (mW)				18	noitsalea	b rawas d	With LST	nozine armo:
	static	0.0000025	0.001	10	2	19	1.2	8.5	5.5
Gate	dynamic @ 100 kHz	0.075	0.17933	10	2	19	1.2	8.5	5.5
	static	0.000005	0.001	300	100	500	60	_	190
Counter	dynamic @ 100 kHz	0.125	0.120	300	100	500	60		190
Propagation	on delay (ns)		begso nig spi	Pipay	學			qu-	lattery back
	typical	8	94 40	10	9.5	3 . philqu	c4eb bns n	1.5 0000	03 UZ 15WO
Gate	maximum	14	190 80	20	15	5	7	2.5	4
Delay/pov	wer product (pJ)	1							
Gate	at 100 kHz	0.52	9 4	100	19	57	4.8	13	16.5
Maximum	clock frequency (MHz)								
	typical	55	4 12	25	33	100	60	160	125
D-type fli	P				0.00				emuonia se
	minimum	30	2 6	15	25	75	40	- 1 - 1 2	100
Counter	typical	45	2 6	32	32	70	45	1 - 20	125
Codinter	minimum	25	1 3	25	25	40	_ : semit 1	allesh rug	100
Output dr	rive (mA)				88				ermination
	standard outputs	4	0.51 0.8	16	8	20	8	20	20 0 000
	bus outputs	6	1.6	48	24	64	24	48	64
Fan-out (LS-loads) ability menu a	o ni nous	Ting Inform	Nom	88		27110		to antiquo:
	standard outputs	1000 1000		40	20	50	20	50	50
	bus outputs	15	4	120	60	160	60	120	160

Table 2: Comparison of HCMOS and LSTTL circuits (V_{CC} = 5 V unless stated otherwise; C_L = 50 pF)

characteristic 1 consistent overlap operate the transfer of transfer of metal-passes of metal-	74HCXXX (note 1) 74HCTXXX	74LSXXX
Max. quiescent power dissipation over temp, range at V _{CCmax}	shows the constituction of a bis	process, Figure .
per gate (mW) and supplied 2014 and notified a	0.027 OWOH at bis sense at	0016 and mort
per flip-flop (mW) nociliaving noisithin, maysi poemed bankogse	0.11 TENT SOMOH & TO SIED IN	
per 4-stage counter (mW)	0.44 Wee and another ablice	175
Para la company de la company	0.055	
		60 enoisul
Max. dynamic power dissipation (C _L = 50 pF)	lation, with the polysilicon gat	nulg mi nai paizu
at fi (MHz)	0.1 squal ant 10 smalqm	0.1 to 1 10
per gate (mW)	0.25 2.25 22	6 22
per filp-flop (mvv)	0.35 2.5 24	22 27
per 4-stage counter (mW)	0.70 3 27	175 200
per buffer/transceiver (mW)	0.30 2.5 24	60 90
Operating supply voltage (V)	2 to 6 (HC)	4.75 to 5.25
(speriov planterit) - epiticy grap x	4.5 to 5.5 (HCT)	shows the poverin
Operating temperature range (°C)	-40 to +85	0 to +70
ever the Comparation range (6)		0 10 +70
	-40 to +125	0.7/0.4
Max. noise margin $(V_{NMH}/V_{NML}V; I_{OHCMOS} = 20 \mu A; I_{OLSTTL} = 4 mA)$	1.4/1.4 (HC)	0.7/0.4
age CMOS The threshold voltage is typically 0.7 V for HCMOS.	2.9/0.7 (HCT)	
Input switching voltage stability over temp, range	±60 mV	±200 mV
Min. output drive current at Tamb max and VCCmin (mA)		
source current (V _{OH} = 2.7 V; note 2)		
standard logic	-8	-0.4
bus logic	-12 жонаан	-2.6
sink current	fernals-n	2.0
standard logic (V _{OL} = 0.4 V)	4	4
standard logic (VOI = 0.5 V)	6	8
bus logic (V _{OL} = 0.4 V)	8	
bus logic (V - V = 0.5 V)		12
bus logic ($V_{OL} = 0.5 \text{ V}$)	9	24
Typ. output transition time (ns) ($C_L = 15 pF$)	91.	
standard logic		
t _{TLH}	6	15
^t THL	6	6
bus logic	20 000	
t _{TLH}	4	15
t _{THL}	4	6
Typ. propagation delay (ns) (C ₁ = 15 pF; note 3)	Annual Continue and	
gata +- /+	8/8	8/11
flip-flop tpLH	14 2 Besic inverser (less) 5/6	
		15
^t PHL Typ. clock rate of a flip-flop; note 5 (MHz)	14	22
	50	33
Max. input current (μA)	L. C. P. C.	
IL STATE OF THE ST	-1	-400 to -800
TH THE TANK	1	40
3-state output leakage current ($\pm \mu A$)	5	20
Reliability (%/1000 h at 60% confidence level)	0.0005	0.008 (note 4)

- 1. Data valid for HCMOS between $-40~^{\circ}$ C and $+85~^{\circ}$ C.
- V_{OH} for a few LSTTL bus outputs is specified as 2.4 V.
 Refer to data sheets for the effect of capacitive loading.

- 5. Measured with a 50% duty factor for HCMOS. For LSTTL, per industry convention, the maximum clock frequency is specified with no constraints on rise and fall times, pulse width or duty factor.

CONSTRUCTION (30 06) Comparison of HCMOS and USTTL directits (V_{CO} = 8 V unless stated otherwise; C_L = 50 pF) (PCMOS and USTRUCTION)

Our HCMOS family is a result of a continuing development programme to enhance the proven polysilicon-gate CMOS process. Figure 2 shows the construction of a basic inverter from the HE4000B series and its HCMOS successor.

The polysilicon gate of a HCMOS transistor is deposited over a thin gate oxide before the source and drain diffusions are defined. Source and drain regions are formed using ion implantation, with the polysilicon gates acting as masks for the implantation. The source and drain are automatically aligned to the gate, minimizing gate-to-source and gate-to-drain capacitances. In addition, the junction capacitances, which are proportional to the junction area, are reduced because of the shallower diffusions. Figure 3(c) shows the parasitic capacitances in a CMOS inverter.

In a metal-gate CMOS transistor, the source and drain are formed before the gate is deposited. Moreover, the metal gate must overlap the source and drain to allow for alignment tolerances. This is why a metal-gate CMOS

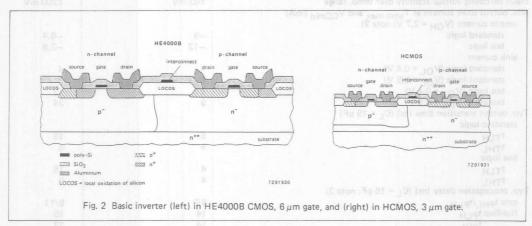
transistor has a higher overlap capacitance than an HCMOS transistor. Furthermore, the deeper diffusions of metal-gate CMOS make the junction capacitance larger.

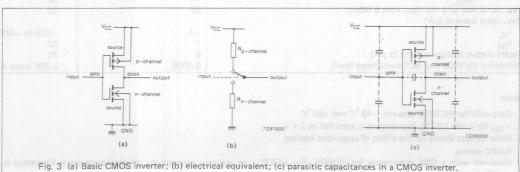
In a silicon-gate MOS transistor, there are three interconnect layers (diffusion, polysilicon and metal) instead of the two layers (diffusion and metal) in a metal-gate MOS transistor. This makes a silicon-gate MOS transistor more compact. The shorter gate length means higher drive capability, which in turn increases the speed at which a silicon-gate MOS transistor can charge or discharge junction capacitance. The drain current of a saturated MOS transistor which determines the speed of the transistor is:

$$I_{DS} = \frac{-\beta}{2} \times \frac{\text{gate width}}{\text{gate length}} \times (\text{gate voltage - threshold voltage})^2$$

where β is the current gain factor which is proportional to the thickness of the oxide layer.

The threshold voltage is typically 0.7 V for HCMOS.





AC CHARACTERISTICS

Test conditions

The propagation delays and transition times specified in the HCMOS data sheets are guaranteed when the circuits are tested according to the conditions stated in the chapter 'Family Characteristics', section 'Family Specifications'. For some circuits such as counters and flip-flops, the test conditions are defined further by the a.c. set-up requirements specified in the data sheet.

Values given in the data sheets are for the whole operating temperature range ($-40~\rm to~+125~^\circ C)$ and the supply voltages used are 2.0 V, 4.5 V and 6.0 V for 74HC devices, and 4.5 V for 74HCT devices. This is a much tougher specification than that commonly used for LSTTL, where the characteristics are usually only specified at 25 $^\circ C$ and for a 5 V supply. Furthermore, the published a.c. characteristics of HCMOS are guaranteed for a capacitive test load of 50 pF, a more realistic load than the 15 pF specified for LSTTL and one that loads the device as the output switches. The published values for HCMOS are therefore representative of those measured in actual systems.

Comparing the speed of HCMOS and LSTTL

A feature of a HCMOS circuit is its speed - in general, comparable to that of its LSTTL equivalent. Owing to the different (more informative) way of specifying data for HCMOS devices, it will be useful to indicate how to compare the published data for HCMOS and LSTTL.

For example, in an LSTTL specification, the use of a 15 pF load instead of a 50 pF one means the maximum propagation delays and enable times published for the LSTTL device will be up to 2.5 ns (typ. 1.3 ns) shorter than those for the HCMOS equivalent. In addition, measuring at the nominal LSTTL supply voltage of 5 V instead of 4.5 V (HCMOS) reduces propagation delays and enable times by a further 10%. So, a 30 ns propagation delay for a HCMOS device is equivalent to a (30-2.5)0.9=25 ns delay for an LSTTL device measured at 4.5 V and with a 15 pF load.

Disable times are measured under different test conditions too - for HCMOS with a 50 pF, $1\,\mathrm{k}\Omega$ load, for LSTTL with a 5 pF, $2\,\mathrm{k}\Omega$ load or for a 45 pF, $667\,\Omega$ load. To compare a HCMOS disable time with that for a LSTTL device with a 5 pF load, subtract 4 ns from the published HCMOS disable time and multiply by 0.9. To compare a value for a 45 pF load, subtract 2 ns and multiply by 0.9. For example, a 30 ns HCMOS disable time is equivalent to (30 - 4)0.9 = 23 ns for a 5 pF load and (30 - 2)0.9 = 25 ns for a 45 pF load.

Set-up hold and removal times are not affected by output load, only by supply voltage. To compare a pub-

lished HCMOS value with an LSTTL value, multiply the HCMOS value by 0.9.

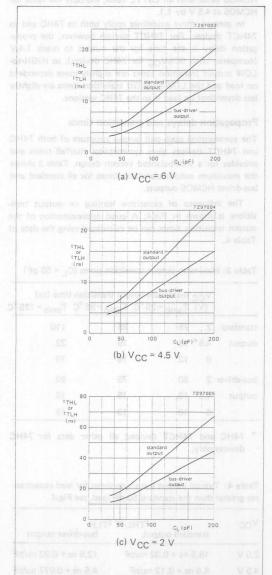


Fig. 4 Typical output transition times as a function of load capacitance; T_{amb} = 25 °C; for 74HCT circuits the data at V_{CC} = 4.5 V only is valid.

Operating frequency is also unaffected by output load, but is affected by supply voltage. To compare a published HCMOS value with an LSTTL value, multiply the value for HCMOS at 4.5 V by 1.1.

In general, these guidelines apply both to 74HC and to 74HCT devices. For 74HCT devices however, the propagation delay is the time for the output to reach 1.4 V (compared with 50%VCC for 74HC devices), so HIGH-to-LOW output transition times are slightly more dependent on load and the LOW-to-HIGH transition times are slightly less dependent on load than the 74HC versions.

Propagation delays and transition times

The symmetrical push-pull output structure of both 74HC and 74HCT devices gives symmetrical rise/fall times and provides for a well-balanced system design. Table 3 shows the maximum output transition times for all standard and bus-driver HCMOS outputs.

The influence of capacitive loading on output transitions is shown in Fig.4; A good approximation of the output transition times can be calculated using the data of Table 4.

Table 3: Maximum output transition times (C_L = 50 pF)

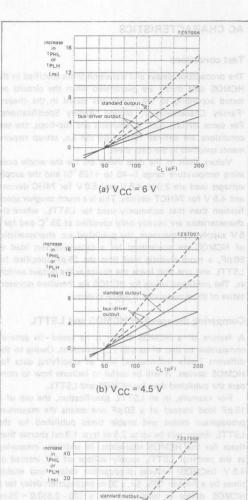
			tput transition T _{amb} = 85 °C	time (ns) T _{amb} = 125°C
standard	2	75	95	110
output			19	22
	6	13 2.4 = 00	16	19
bus-driver	2	60	75	90
output	4.5*	12	15	18
2	6	10	13	15

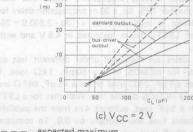
^{* 74}HC and 74HCT devices; all other data for 74HC devices only.

Table 4: Typical output transition times for load capacitances greater than the standard 50 pF load, see Fig.4

Vcc	t _{THL} or	tTLH
	standard output	bus-driver output
2.0 V	18.5 ns + 0.32 ns/pF	12.5 ns + 0.22 ns/pF
4.5 V	6.6 ns + 0.12 ns/pF	4.5 ns + 0.077 ns/pF
6.0 V	5.6 ns + 0.10 ns/pF	3.8 ns + 0.065 ns/pF

Note: values in pF are the load capacitance minus 50 pF.

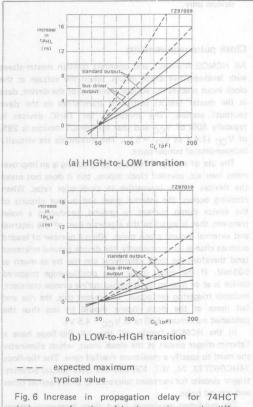




--- expected maximum
typical value

Fig. 5 Increase in propagation delay for 74HC devices as a function of load capacitance; $T_{amb} = 25$ °C.

A parameter specified for TTL devices is the output short-circuit current HIGH (IOS). Originally intended to reassure the TTL user that the device would withstand accidental grounding, this parameter has become a measure of the ability of the circuit to charge the line capacitance and is used to calculate propagation delays. In CMOS devices however, there is no need to specify IOS because the purely capacitive loads allow extrapolation of the a.c. parameters over the whole loading range. Figure 5 (for 74HC devices) and Fig.6 (for 74HCT devices) show the increase in propagation delay for loads greater than 50 pF. The additional delay can be calculated from the output saturation current (short-circuit current). Referring to the output characteristics (Figs 33 to 36), the propagation delay is the time taken for the output voltage to reach 50%



devices as a function of load capacitance; the different values for t_{PHL} and t_{PLH} are due to the asymmetrical reference level of 1.3 V at the outputs; $t_{PL} = 25\,^{\circ}\text{C}$; $t_{CC} = 4.5\,\text{V}$.

of V_{CC} for 74HC devices, or 1.4 V for 74HCT devices. Since a saturated output transistor acts as a current source, the additional delay is Δ CV/I, where Δ C is the load capacitance minus 50 pF, V is the voltage swing at the output to the switching level of the next circuit, and I is the average source current of the saturated output.

Supply voltage dependence of propagation delay

The dynamic performance of a CMOS device depends on its drain characteristics. These are related to the switching thresholds and the gate-to-source voltage VGS which is equal to the supply voltage VCC. A reduction in VCC adversely affects the drain characteristics, increasing the propagation delays.

Over the supply voltage range of 74HCT devices, 4.5 V to 5.5 V, the effects of different propagation delays on performance are minimal. Over the supply voltage range of 74HC circuits, 2 to 6 V, the effects on performance are significant, see Figs 7 and 8.

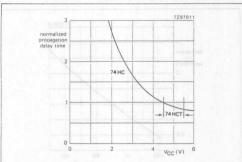


Fig. 7 Propagation delay as a function of supply voltage; $T_{amb} = 25 \,^{\circ}\text{C}$; $C_L = 50 \, \text{pF}$.

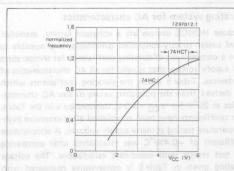


Fig. 8 Operating frequency as a function of supply voltage; $T_{amb} = 25 \,^{\circ}\text{C}$; $C_{L} = 50 \, \text{pF}$.

Temperature dependence of propagation delay

In TTL circuits, β (current gain), internal resistances and forward-voltage drops are all temperature-dependent. In HCMOS circuits, essentially only the carrier mobility, which affects the propagation delay, is temperature dependent. In general, propagation delay increases by about 0.3% per °C above 25 °C.

Between 25 °C and 125 °C

$$t_p = t_p'(1.003)^{T_amb^{-25}}$$

vhere

tp' is the propagation delay at 25 °C,

Tamb is the ambient temperature in °C.

$$t_p = t_p'(0,997)^{25-T_{amb}}$$

Figure 9 shows the temperature dependence of a characteristic such as propagation delay.

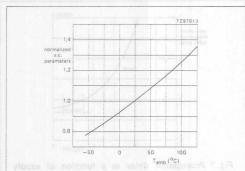


Fig. 9 Typical influence of temperature on AC parameters; $V_{CC} = 5 \text{ V}$.

Derating system for AC characteristics

Because HCMOS devices are a coherent family, manufactured under strictly-controlled conditions, it is possible to have a common set of derating coefficients for temperature and supply voltage that is valid for all AC characteristics of all devices. Table 5 shows the derating coefficients which are derived from the published values of the AC characteristics at 25 °C for $V_{\rm CC}$ = 4.5 V, denoted by x in the Table. The coefficients have been established after extensive high-temperature testing at many supply voltages. A temperature coefficient of -0.4%°C was established after comparing the test results with worst-case calculations. The voltage derating given in Table 5 is conservative compared with that shown in Fig.7 for propagation delay. For operating frequencies (Fig.8), the reciprocal of the derating coefficients shown should be used.

Table 5: Derating coefficients for the AC characteristics of HCMOS devices

NASERIENY	orusated and acto	ent Asia issa "Fili	accidental on
supply	ambient temp	85 °C lib ant to 1	125 °C
2 V	5 (5x)		7.5 (5z)
4.5 V*	1 (x)	1.25 (y = 1.25 x)	1.5 (z = 1.5x)
6 V	0.85 (0.85x)	1.0625 (0.85y)	1.275 (0.85z)

All coefficients are derived from the value of the AC characteristic at V_{CC} = 4.5 V and T_{amb} = 25 °C denoted in the table by x.

Clock pulse requirements

All HCMOS flip-flops and counters contain master-slaves with level-sensitive clock inputs. When the voltage at the clock input reaches the voltage threshold of the device, data in the master (input) section is transferred to the slave (output) section. The threshold for 74HC devices is typically 50% of VCC and that for 74HCT devices is 28% of VCC (1.4 V at VCC = 5 V). The thresholds are virtually independent of temperature.

The use of voltage thresholds for clocking is an improvement over a.c. coupled clock inputs, but it does not make the devices totally insensitive to clock-edge rates. When clocking occurs, the internal gates and output circuits of the device dump current to ground, producing a noise transient that is equal to the algebraic sum of the internal and external ground plane noise. When a number of loaded outputs change simultaneously, the device ground reference (and therefore the clock reference) can rise by as much as 500 mV. If the clock input of a positive-edge triggered device is at or near to its threshold during a noise transient, multiple triggering can occur. To prevent this, the rise and fall times of the clock inputs should be less than the published maximum (500 ns at V_{CC} = 4.5 V).

In the HCMOS family, all the J-K flip-flops have a Schmitt-trigger circuit at the clock input, which eliminates the need to specify a maximum rise/fall time. The flip-flops 74HC/HCT73, 74, 107, 109 and 112 have special Schmitt-trigger circuits for increased tolerance to slow rise/fall times and ground noise.

The published maximum input clock frequency ratings for clocked devices are for a 50% duty factor input clock. At these rated frequencies, the outputs will swing between V_{CC} and GND, assuming no DC load on the outputs. This is a very conservative and reliable method of rating the

^{* 74}HC and 74HCT devices; all other data for 74HC devices only.

clock-input-frequency limits for HCMOS devices which are always at least as good as those for LSTLL even though they may appear to be inferior. This is because the maximum operating frequency of a TTL device is published, not for a 50% duty factor clock, but for a minimum clock pulse width.

System (parallel) clocking

In synchronously-clocked systems, spreads in the clock threshold levels of devices can cause logic errors if slow clock edges are used. For example, if data in one circuit changes before the clock threshold of the next sequential circuit is reached, a logic error will occur, see Fig.10.

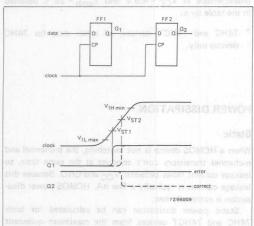


Fig. 10 In synchronously-clocked systems, changing the data in one device before the clock switching threshold of the next has been reached can cause logic errors. V_{ST1} is the clock threshold of device 1; V_{ST2} is the clock threshold of device 2.

To prevent this type of logic error, the maximum rise or fall time of the clock pulse should be less than twice the propagation delay of the flip-flop.

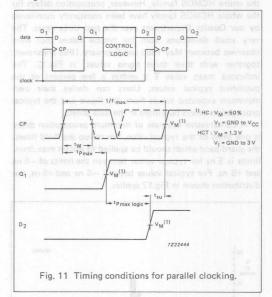
For a HCMOS device, the rise/fall time must be limited to 1000, 500 or 400 ns for $V_{\rm CC}$ = 2 V, 4.5 V and 6 V respectively. If these times are exceeded, noise on the input or power supply rails may cause the outputs to oscillate during transitions, causing logic errors and excessive power dissipation.

Clock pulse considerations as functions of maximum frequency

The minimum input frequency is measured with a clock that has a 50% duty factor. For a stand-alone flip-flop, the following direct relationship exists between the minimum required width of the clock pulse $t_{\rm W}$ LOW or $t_{\rm W}$ HIGH (whichever is the longest) and the measured maximum frequency:

$$f_{max} = 1/2t_{w}$$

If two or more flip-flops are synchronously clocked in parallel, other timing conditions may cause a lower maximum frequency than that which can be calculated from the pulse width measurements. An example is shown in Fig.11.



The maximum frequency is now determined by:

$$f_{max} = \frac{1}{t_{p max}(CP \text{ to } Q_1) + t_{p max}(control logic) + t_{su}(D_2 \text{ to } CP)}$$

The measured minimum width (t_w) of the clock pulse as shown in Fig.11 would suggest a higher obtainable frequency in this example. This parallel clocking scheme is often encountered in counter circuits (e.g. '160' or '190' series).

If the internal delays and set-up times exceed the minimum required duration for the clock pulse, the maximum frequency will be entirely determined by these internal delays and set-up times.

Cascading HCMOS counters in a parallel clocking scheme may also result in lower maximum frequencies than those given for stand-alone ICs. This is because the frequency will then be determined by the propagation delay of a count output, for example the delay of the intermediate logic and the set-up time between the clock enable and the count input of the succeeding counter IC.

Minimum AC characteristics

Minimum propagation delays are not specified in the data sheets. However, an increasing number of HCMOS users are asking for minimum propagation delay values so that they can make conclusive data handling calculations. Since our test programs don't include lower limits for propagation delays, it's impossible for us to guarantee these values for the entire HCMOS family. However, propagation delays for the whole HCMOS family have been constantly monitored by our Quality Department over the past three years. The very small deviations from the typical values that were observed between May 1985 and February 1988 are shown. together with their three sigma values, in Fig.12. The indicated mean value \overline{x} is within a few percent of the published typical values. Users can derive their own minimum expected values from this figure and the typical propagation delays published in the data sheets.

A conservative estimate of minimum propagation delay is one third of the typical value. For set-up and hold times, the guard-band which should be applied to obtain max./min. limits is 5 ns for typical values between the limits of -5 ns and +5 ns. For typical values beyond -5 ns and +5 ns, the distribution shown in Fig.12 applies.

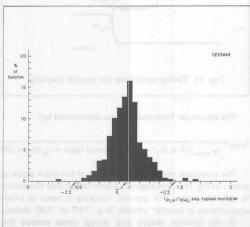


Fig. 12 Batch-to-batch variation of propagation delay (tp_{LH}/tp_{HL}) .

Table 6 gives the derating coefficients for calculating the minimum propagation delays of HCMOS devices at various supply voltages and temperatures.

Table 6: Derating coefficient for the expected minimum propagation delay of HCMOS devices

supply voltage	ambient temperatu 25 °C	re _40 °C
2 V	2 (2x)	1.67 (2y)
4.5 V*	1 (x)	0.83 (y = 0.83 x)
6 V	0.8 (0.8x)	0.66 (0.8y)

Note: The minimum value is reached at the lowest possible temperature.

All coefficients are derived from the value of the AC characteristic at V_{CC} = 4.5 V and T_{amb} = 25 °C denoted in the table by x.

* 74HC and 74HCT devices; all other data for 74HC devices only.

POWER DISSIPATION

Static

When a HCMOS device is not switching, the p-channel and n-channel transistors don't conduct at the same time, so leakage current flows between V_{CC} and GND. Because this leakage current is typically a few nA, HCMOS power dissipation is extremely low.

Static power dissipation can be calculated for both 74HC and 74HCT devices from the maximum quiescent current specified in the data sheets, see Table 7.

Table 7: Maximum quiescent current of HCMOS devices at V_{CCmax}^* ($V_1 = V_{CC}$ or GND; $I_0 = 0$)

device		quiescen	t current	current
complexity	typical at 25 °C	25 °C	maximum 85 °C	125 °C
SSI	2 nA	2 μΑ	20 μΑ	40 μΑ
FF half ad 12	4 nA	4 μΑ	40 μΑ	80 μΑ
MSI	8 nA	8 μΑ	80 μΑ	160 μΑ
LSI	50 nA	50 μΑ	500 μΑ	1000 μΑ

^{* 6} V for 74 HC; 5.5 V for 74 HCT.

Dynamic

When a device is clocked, power is dissipated charging and discharging on-chip parasitic and load capacitances. Power is also dissipated at the moment the output switches when both the p-channel and the n-channel transistors are partially conducting. However, this transient energy loss is typically only 10% of that due to parasitic capacitance.

The total dynamic power dissipation per device (PD) is:

$$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$$
 (1)

CpD is the power dissipation capacitance per package

is the input frequency

fo is the output frequency

is the total external load capacitance per output.

The second term of equation (1) implies summing the product of the effective output load capacitance and frequency for each output. However, a good approximation of the total dynamic power dissipation of an HCMOS system can be obtained by summing the published CPD values and load capacitance for the HCMOS devices used and, assuming an average frequency, using equation (1).

For one-shot circuits, gates configured as oscillators, phase-locked loops and devices used in a linear mode, additional dissipation is caused by static supply currents (ICC) whose values are given in the device data sheets.

Power dissipation capacitance

CPD is specified in the device data sheets, the published values being calculated from the results of tests described in this section. The test set-up is shown in Fig.13. The worst-case operating conditions for CPD are always chosen and the maximum number of internal and output circuits are toggled simultaneously, within the constraints listed in the data sheet. Table 8 gives the pin status for HCMOS devices during a CpD test. Devices which can be separated into independent sections are measured per section, the others are measured per device.

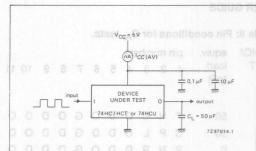


Fig. 13 Test set-up for determining CpD. The input pulse is a square wave between V_{CC} and GND; $t_r = t_f \le 6 \text{ ns}$; $T_{amb} = 25 ^{\circ}\text{C}$. All switching outputs are loaded with 50 pF (including test jig capacitance). Unused inputs are connected to V_{CC} or GND.

The recommended test frequency for determining CPD is 1 MHz, but this is best increased to 10 MHz when ICC is low and the device quiescent current influences ICC(AV). Loading the switched outputs gives a more realistic value of CpD, because it prevents transient 'through-currents' in the output stages. Furthermore, automatic testers often introduce about 30 pF to 40 pF on each device pin.

The values of CPD in the data sheet have been calculated using: 0 0 0 0 0

$$C_{PD} = \frac{I_{dyn(device)}}{V_{CC}f_i}$$

$$I_{dyn(load)} = \Sigma (C_L V_{CC} f_o)$$

HIGH SPEED CMOS 74HC/HCT/HCU LOGIC FAMILY

USER G	UIDE																												
Table 8:	Pin cond	litio	ns	for	C	tes	ts.																						
74HC/	equiv.		า ทเ																										
НСТ	load (pF)	1		3		5	6	7	8	9	10	11	12	13	14	15	16	17	18		20	21	22	2 23	3 24	4 2	5 2	6 27	7 28
00	50	P	Н	C	D	D	0	G	0	D	D	0	D	D	٧	-	-	-	-	7/8	-	o¥.	171	3 =	1 -	DV	390	= 0	9-1
02	50	C	P	L	0	D	D	G	D	D	0	D	D	0	٧	-	-	-	-	-	-	-	-	-	-	-	-	en um	N -
03	0	P	Н	В	D	D	0	G	0	D	D	0	D	D	٧	ger:	1	0.01	1008	DOM		nnit	acia	-	9\\ <u>\\</u>	10 2	tt ai	0-	0_
04	50	P	C	D	0	D	0	G	0	D	0	D	0	D	٧	-	-	-	_	-	-	ADIO AD	upe upe	nit fi	Jegs.	m 8	t al	_	-
	50	P	С	D	0	D	0	G	0	D	0	D	0				nor ti		3.763	ioso		sof	IST I	93 X 8	1157	of a	to ei	5	5-
08	50	P	Н	C	D	D	0	G	0	D	D	0	D				102 3 <u>8</u> 9				noi quir	16W	1 es 11 <u>12</u> 8	o n	the the	bn to	10	ub <u>o</u> n	9_
10	50	P	Н	D	D	D	0	G	0	D	D	D	C	Н	V	16 1	goop	-	(187	SVANO		nuit;	HO	dos	9 7	01	yons	ups	-
11	50	Р	Н	D	D	D	0	G	0	D	D	D	С	H	V	m ga a d zi	iror Id i it	ioisi i t ri	1910) 1 - 1	ili m ili ti n	WO.	V -)	ben ben	0 15 6 7 0	3 - 1	one d =	10 ft	oina nate	(2 - 1
14	50	P	C	D	0	D	0	G	0	D	0	D	0	D	V	sa <u>i</u> vi	p 3	ON	οĤ	ord)	10)	900	stip	80 <u>8</u> :	bs	ol_j	ns_	eau)	W.
20	50					Hi t in			0				D	D	٧	lozo lozo		pais ber	u j ugit	rons ros	ect n	it o	ps 18 el Tu	VE I	101	inim la-9i	uses to 1	o-il	-
21 10 90	50					H							D	D	٧		b a	2109 2109	b e	dr e	i n	IVIS	STE	256	dev	320	dis	lan	-
27	entered to the same				D	D						D	С	L	V	-	-	_	-	-	-	-	-	-	-	-	-	-	-
30	50	P	H	Н	H	Н	Н	G	C		0	Н	Н	0	٧	-	-	-	-	-8	9(25)	1126	qeo	UTO.	der	1122	b 20	9 AVITO	-
32	50	P	L	C	D				0		D		D	D	٧		64	100	erie erier	61 <u>2</u> 18 201	<u>50</u>)	Vely	943	rai ralu	bell ols:	to ac	e al	(H)	9-
42	100	С	С		0	0	0	0	G	0	0	0	L	L		1.97	٧	DV	yarlı	ai	qu-s	92	357	on T	.0	oita	98 8	idi	ni -
58	50	Р	D		D	D	0	G	0	L	L	L	Н			110	n D	Bo	i la	i noi mair	úlic	29	irau	a in	WE	bear	1 91	i br	16_
73	50	Р	Н	Н	V	D	D	D	0	0	D	G	C	C	Н	-	nist V st	-	-	tr mi	riziv	-	euros o	tane lde l	-	-	e lege	b 88	_
74	50	Н	Q	Р	H	C	C	G	0	0	D	D	D	D	٧		ic i n			y Eg	gi T 8	0-1	265	350	17	Dit.	D =	ol v s	b-
75	50	C	Q	D	D	V	D	D	0	0	0	0	G	P	0	0	C	uc_ t	9910	2690	1_91	B _2	10 <u>i</u> 7:	182	ing)	in <u>ac</u>	app	03	11_
85	50	L	Н	Р	Н	0	С	0	G	L	L	L	L	L	L	L	٧	-	-	-	.8	- avic	791	i pa	- Amst	om.	571B. 1	then:	-
86	50	P	L	С	D	D	0	G	0	D	D	0	D	D	V	_	_	_	_	_	_	_		_	_		_	_	_
93	47	Q	L	L	D	V	D	D	C	C	G	C	C	D	V	_	_	_	_	_	_	_	_	_	_	_	_	_	_
107	50	Н	C	C	Н	0	0	G	D	D	D	D	P	Н	V	_	_	_	_	_	_	_	_	_	_	_	_	_	_
109	50	Н	Н	L	P	Н	С	C	G	0	0	D	D	D	D	D	V	_	_	_	_	_	_	_	_	_	_	_	_
112	50	Р	Н	Н	Н	С	С	0	G	0	D	D	D	D	D	Н	٧	-	-	-	-	-	-	-	-	_	-	-	_
123	100	L	Н	Р	С	0	0	0	G	D	D	D	0	С	0	R	V												
125	50	L	Р	C	D	D	0	G	0	D	D	0	D	D	V	_	_		_		_		_				_		
126	50	Н	P	C	D	D	0	G	0	D	D	0	D	D	V													1	
132	50	Р	Н	C	D		0			D		0	D	D	V												Ī		
102	00	,	1.1	0		0	0	4	0	0	0	0	U	0	V							111						_	

PHHHHHGCHHHHHV -

USER GUIDE UOHATOHAOHAT

HIGH SPEED CMOS 74HC/HCT/HCU LOGIC FAMILY

Table 8:	Pin cond	litio	ns	for	C _{PO}		ts.																					
74HC/	equiv.	pir	า ทเ	ımb	ers																							
HCT	load	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25 26	27	28
	(pF)																	0										
137	100	P	L	L	L	L	Н	0	G	0	0	0	0	0	C	C	V	0	74	-	5	-)	-1	-51	-	001	-	238
138	100	P	L	L	L	L	Н	0	G	0	0	0	0	0	C	C	V	-	-	-	-	-	-	-	-		-	-
139	100	L	P	L	C	C	0		G	0	0	0	0	D	D	D	V	7	0	0	70	70	70		-	- 02	-	FAS
147	50	H	Н	Н	Н	Н	0	0	G	C	Н	P	H	Н	0	0	V	Ð	70	70	0	79	0	-	-	- 05	-	242
151	100	D	D	L	Н	C	C	L	G	L	L	P	D	D	D	D	V	B	70	70	73	70	70	-	-	- 08	-	243
153	50	L	L	D	D	L	H	C	G	0	D	D	D	D	P	D	V	0	0	0	U	70	79	-	-	- oa	-	244
																				a								
154	100	C	C	0	0	0	0	0	0	0	0	0	G	0	0	0	0	0	L	L	L	L	L	P	V		-	-
157	50	P	L	Н	C	L	L	0	G	0	L	F	0	L	L	L	V	7	0	0	7-1	-1	0	a	-	001	-	251
158	50	P	L	Н	C	L	L	0	G	0	L	-	0	L	L	6	V	5	TH	7	70	d	-	-	-	50	-8	253
160	55	Н	P	D	D	D	D	Н	G	H	Н	C	C	C	C	C	V	0	0	70	0	H	7	79	-	- 05	-	257
161	50	Н	P	D	D	D	D	Н	G	Н	Н	C	C	C	C	C	V	7	70	0	5	TH	-	79	-	08	-	885
162	55	Н	Р	D	D	D	D	Н	G	Н	Н	С	C	С	С	C	V	-	-	-	-	-	-	-	-		-	-
163	50	Н	P	D	D	D	D	H	G	Н	A	C	C	C	C	C	V	0	0	0	O	0	0	H	-	25	-	273
164	200	Q		C	C	C	C	G	P	Н	С	C	С	С	V	ŢĮ.	5	Đ	0	0	IJ	ō		ij	-	100	-	280
165	50	Н	P	D	D	D	D	C	G	C	Q	D	D	D	D	L	V		H	79	0	-)	TH	ō	-	250	-	283
166	25	Q	D	D	D	D	L	P	G	Н	D	D	D	C	D	H	V	0	7	0	TCI_	H	H	Ŧ	-	12	-	297
170	25	-		0	V		0	0	0	Þ	0	0	9	0	0	H	0											
173	25	L	L	С	0	0	0	P	G	L	L	D	D	D	Q	L	V	-	-	-	-	-	-	-	-		-	-
174	25	Н	C	Q	D	0	0	0	G	P	0	D	0	D	D	0	٧	J.	0	0	0	Ū	D.	0	-	100	-	354
175	50	Н	C	C	Q	D	0	0	G	P	0	0	D	D	0	0	٧	Ō	0	Ū	70	Ō.	0.	Q	-	50	-	356
181	300	P	H	Н	L	L	Н	Н	L	C	C	S	G	C		С	C	C	P	H	-	H	L	Н	V	- 50		365
182	150	Н	L	H	L	Н	L	0	G	C	0	C	C	8	Н	L	V	Ō	ā	ō	Ō	ō	0	J	-	50	-	366
190	55	D	C	C	L	L	С	С	G	D	D	H	С	C	P	D	٧	Ō	0	0	0	0	79	-	-	- 08	-	367
191	53	D	C	C	L	L	C	C	G	D	D	H	С	C	P	D	V	0	0	ō	d	ō.	9	7	-	50	-	388
192	55	D	C	C	Н	8	C	C	G	D	D	Н	C	C	P	D	٧	ō	ō	ō	ō	Ō	ō	1	-	25	-	373
193	50	D	C	C	Н	8	C	C	G	D	D	Н	C	C		D	V	ā	ō	ō	7	ō	0	J	7	25	-	374
194	100	H	Q	D	D	D	D	D	G	H	L	P	C	C	C	C	V	D	ō	0	ō	0	0	7	-	25	-	377

74HC/ HCT	equiv.	•		ımb						•			10	10							-		-			25			
1101	(pF)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17								25			
195	125	Н	Н	LS	D	D	D	D	G	Н	P	C	C	C	C	C	٧	-7	-8	-8	-4	_8	-9	-1	_	DB	QI :	. 1	OH.
221	100	L	Н	P	С	0	0	0	G	D	D	D	0	С	0	R	V	_	-	-	-	_	_	-	-	-(-1	9)		
237	100	P	L	L	L	L	Н	0	G	0	0	0	0	0	С	C	V	_	_	-	_	_	_	_	_	_	_		-
238	100	P	L	L	L	L	Н	0	G	0	0	0	0	0	C	C	V	0	1			_		_9	-	_00	1	_ 1	1.87
240	50	L	P	0	D	0	D	0	D	0	G	D	0	D	0	D	С	D	٧	_	-	-	-	_	-	_	_		-
241	50	L	P	0	D	0	D	0	D	0	G	D	0	D	0	D	C	D	V	_	0	_	-9	_	-	_00	1	_ 6	139
242	50	L	0	P	D	D	D	G	0	0	0	C	0	L	V	0	5	0	0	7	H	H	H	1	-	_ 0	3	_ 1	14
243	50	L	0	P	D	D	D	G	0	0	0	C	0	L	٧	-	9	-1	-0	-0	-13	-	10	0	-	_00	13		81
244	50	L	P	0	D	0	D	0	D	0	G	D	0	D	0	D	C	D	٧	-	_0	0	-	-	-	- 0	2	- 6	ar
245	50	Н	P	D	D	D	D	D	D	D	G	0	0	0	0	0	0	0	٧	-	_	-	-	-	-	-	-		
251	100	D	D	L	Н	C	C	L	G	L	L	Р	D	D	D	D	V	2	-	-	2		-	-	-	- 9	9		15
253B	50	L	L	D	D	L	Н	C	G	0	D	D	D	D	P	D	٧	7	-	-	-0	-	-	-	-	-	<u>=</u>		151
257	50	P	L	Н	C	D	D	0	G	0	D	D	0	D	P	D	٧	-	-	-3	-2	7	-	7	-	_ 0	9		161
258	50	P	L	Н	C	D	D	0	G	0	D	D	0	D	P	D	V	_	_0	_	-		-	-	-	-	2		ar
259	25	L	L	L	C	0	0	0	G	0	0	0	0	Q	P	Н	٧	-	-	- a	-	-	-	-	-	-	-		-
									V	0	0	0	5																
273	25	Н	C	Q	D	0	0	D	G	P	0	D	D	0	0	D	D	0	٧	-	-	7	-1	0	-	- 9	0		16
280	100	L	L	0	L	C	C	G	P	L	L	L	L	L	V	-	-	5	-	-	-0	2	q	14	-		-		2.5
283	250	C	Н	L	C	P	Н	L	G	C	C	H	L	C	L	Н	٧	9	-	0	0	0	-0	-0	-	- 2	-		16
297 299	12 250	Н	H	Н	P	Q	L	C	G	D	D	0	0	D	Н	Н	V	-	- 0	-	-	-		-	-	-	-		
299	250	Н	L	L	C	С	С	С	C	Н	G	Q	P	C	С	С	C	C	D	-	V	0		J	-	- 8	2	. 8	77
354	100	D	D	D	D	D	D	L	Н	2	G	L	P	0	P	L	2	Н	C	C	V	0	0	H	_	_ 8	2	6	77
356	50	D	D	D	D	D	D	D	Q	P	G	2	L	0	0	L	D	H	C	C	V	9	0	L	_	_ 0	ē .	- 3	17
365	50	L	P	C	D	0	D	0	G	0	D	0	D	0	D	5	V	H	H	_1		H	H	9	_	00	€ .	1	81
366	50	L	P	С	D	0	D	0	G	0	D	0	D	0	D	P	V	0		H	_]	H		B	-	50_	<u>_</u> .	_ §	18
367	50	L	P	C	D	0	D	0	G	0	D	0	D	0	D	L	٧	2	2		-	0	0	7	-	_ 6	<u>c</u> .		19
368	50	L	P	C	D	0	D	0	G	0	D	0	D	0	D	L	٧	-	-0	- 0	7 3	7	70	7	-	- 0	<u> </u>	- 1	19
373	25	L	C	Q	D	0	0	D	D	0	G	P	0	D	D	0	0	D	D	0	٧	2	2	0	-	- 0	2 .	- 9	O.F.
374	25	L	C	Q	D	0	0	D	D	0	G	P	0	D	D	0	0	D	D	0	V	0	3	- 1	-	00	-	- 0	19
377	25	L	C	Q	D	0	0	D	D	0	G	P	0	D	D	0	0	D	D	0	٧	70	-	-	-	700	-		0.1
390	50	P	L	С	Q	С	С	С	G	0	0	0	D	0	D	D	V	_	_	_				_		_			
393	47	P	L	С	C	С	С		0			0	D	D	V	_	_	_	_	_	_	_	_	_	_				

74HC/	equiv.	pii	ก กเ	ımb	ers																						
HCT	load	1			4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19						25 26	
	(pF)																										
423	100	L	P	Н									0											0	-	- 0	4051_
533	25	L	C	Q	D	0	0	D	D	0	G	P	0	D	D	0	0	D	D	0	V	0	0	0	-	_ 0_	4052
534	25	L	C		D		0						0			0		D	D	0	V	0	0	0	-	_ 0_	4053
540	50	L	P	D	D	D	D	D	D	D	G	0	0	0	0	0	0	0	C	P	V	0	2	D	-	30L	10804
541	50	L	P	D	D	D	D	D	D	D	G	0	0	0	0	0	0	0	C	L	V	-	-	-	-		-1-
563	25	L	Q	D	D	D	D	D	D	D	G	P	0	0	0	0	0	0	0	C	V	D	0	0	-	_ 0_	_980F
564	25	L	Q	D	D	D	D	D	D	D	G	P	0	D	0	0	0	0	0	C	V	0	0	0	_	0_	4087_
573	25	L	P	D	D	D	D	D	D	D	G	Н	0	0	0	0	0	0	0	C	V	Ω		9	_	78_	4075_
													0														
574	25	L	Q	D	D	D	D	D	D	D	G	P	0	0	0	0	0	0	0	C	V	Ω	Ω.	0	_	_ 0_	4316_
583	200	Н	Н	Н	L	H	C	C	G	C	C	C	19	P	H	H	V	_1	0	0	0	0	0	0	-	_ 12	4351_
594	225	C	C	C	C	C	C	C	G	C	H	P	P	H	Q	C	V	4	0	0	0	0	Ω	0	_	_ 0_	4352_
595	225	C	C	C	C	C	C	C	G	C	H	P	P	P	Q	C	V	_	0	0	0	0	Ω	0	_	_ 0_	4353_
597	25	D	D	D	D	D	D	D	G	C	H	P	D	H	Q	D	V	٥	0	_1	Ω	О	0	_	_	_55_	4510_
640	25	Н	P	D	D	D	D	D	D	D	G	P	0	0	0	0	0	0	C	L	V	Н	_I	_	_	DOS	4511_
643	50	Н	P	D	D	D	D	D	D	D	G	P	0	0	0	0	0	0	C	0	V	_	9	H	_	100	4574
646	50	D	L	Н	P	D	D	D	D	D	D	D	G	0	0	0	0	0	0	0	C	L	D	D	V	DOL	4815_
648	50	D	L	Н	P	D	D	D	D	D	D	D	G	0	0	0	0	0	0	0	C	D	D	D	٧	_50_	4516_
652	50	D	L	Н	P	D	D	D	D	D	D	D	G	0	0	0	0	0	0	0	C	Ď.	D	D	V	_45_	4518_
670	200	L	L	L	L	P	C	C	G	C	C	6	H	0	D	0	V	_/	0	0	0	9	H	9	_	47	4520_
688	50	L	P	L	L	L	L	L	L	L	G	L	L	L	L	L	L	L	L	V	_	_	-	-	_		
4002	50	C	P	L	L	L	0	G	0	D	D	D	D	0	V	0	Ð	_]	9		1	_					
4015	100	P	C	0	0	0	D	D	G	D	0	C	C	C	L	Q	V	-	_	_ 6	lda:	¥1qq	16 (1				
4016	0	0	0	0	0	D	D	G	0	0	0	0	D	P	٧	_	y	3	0	0	Ð	0					
4017	55	C	C	C	C	C	C	C	G	C	C	C	C	L	P	P	V	Ð	0	0	0	0	D				
4020	48	C	C	C	C	C	C	C	G	C	P	L	C	C	C	C	V	0	0	0	9	٥,	Đ				
4024	48	P	L	C	C	C	C	G	0	C	0	C	C	0	V	_1	Ð	0	0	H	0						
4040	48	С	C	C	C	C	C	C	G	C	P	L	C	С	C	C	V	_	_		_	_	5				
4046A	50	0	C	L	0	Н	0	0	G	L	0	0	0	0	Р	0	V	-	_	_ 5	des	ilqo	(B) 10				
4049	50	V	C	Р	0	D	0	D	G	D	0	D	0	0	D	0	0	0	Ú	0	0	0	9				
4050	50	V	С	P	0	D	0	D	G	D	0	D	0	0	D	0	0	0	0	0	D	0	_				

HIGH SPEED CMOS 74HC/HCT/HCU LOGIC FAMILY

74HC/ HCT	equiv. load (pF)		n nu		ers																						
4051	0	0	0	0	0	0	L	G	G	L	Lo	P	0	0	0	0	V	-	-	-	_	-	-0				
4052	0				0																-0	-	-				
4053	0	0	-	0												0					-0	70	-0				
4059	17	P	D	Н	L	L	L	L		L						L		L		L	L	L	L	C	٧		
4060*	106	C	C	C	C	C	C	C	G	C	C	P	6	C	C	C	٧	70	-0	-0	-0	-0	- q				
4066	0	0	0	0	0	D	D	G	0	0	0	0	D	P	V	TU	70	70	-0	-0	-0	70					
4067	0	0	0	0	0	0	0	0	0	0	P	L	G	Ц	40	L	0	0	0	0	0	0	0	0	٧	- 85	
4075	75	P	L	D	D	D	0	G	P	C	0	D	D	D	٧	TO	70	70	70	Ta	70	70					
4094	250	Н	Q	P	C	C							C				٧	-	-	-	-	-	-				
4316	0		0	0		P										D					TO		TO				
4351_	.0	0		0		0			Н											0			H	TH	-		
4352_	0	0		0		0	0													0			70	70	-		
4353	0	0		0																0			70	70	-		
4510	55	L		D	D	L													70	TQ	TO	70					
4511	200	L	L	Н	Н	L	5	6	G	C	C	0	0	C	0	C	V	U	U	.70	T	70	79				
4514_	100	Н	P	L	0	0	0	0	0	0	0	C	G	0	0	0	0	0	0	0	0	1	1	1	\/		
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HIGH SPEED CMOS 74HC/HCT/HCU LOGIC FAMILY

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		(pF)																								
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4	0103	3	P	Н	L	L	L	L	L	G	Н	L	L	L	L	C	Н	V	-	-	-	_	-	-		
4	0104	100	Н	Q	D	D	D	D	D	G	Н	L	P	C	C	С	C	V	-	-	-	-	-	-		
4	0105	200	L	C	P	Q	Q	Q	Q	G	L	C	C	C	C	С	P	V	-	-	-	-	-	_		
*	load wo	ord;																								
0:		0		0			0			0)															
1:		1		1			1			1																
2:		X		X			X			X	(
3:	14.5	X		X			X			X	(

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Key		
V	=	Vcc (+5V)
G	=	ground (Fig)
Н	=	logic 1 (V _{CC}) - inputs at V _{CC} for HC types; 3.5 V for HCT types
L	=	logic 0 (ground) = V 9 0 0 0 0 H D 0 0 0 0 9 0 J 825 4047
D	=	don't care - either H or L but not switching a page of a good of a
С	=	a 50 pF load to ground is allowed
0	=	an open pin; 50 pF to ground is allowed
P	=	input puise (see ilustration)
Q	=	half frequency pulse (see illustration)
R	=	1 $k\Omega$ pull-up resistor to an additional 5 V supply other than the
		V _{CC} supply V D O O O O O O O D D D D D D D D D D D
В	=	both R and C. V 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
		ABTO2 S PHELLEGHLELEGHV

USER GUIDE

Conditions for Con tests

Gates All inputs except one are held at either VCC or GND, depending on which stare causes the output to taggle. The remaining input is toggled at a known fraquency. Cop is specified per-gate.

Decoders. One input is toggled, causing the outputs to toggle at the same rate (normally one of the address-scient pins is switched while the decoder is enabled). All other inputs are tied to Voc or OND, whichever enables operation, Ond is specified per-independent-decoder.

Multiplexers. One data input is fied HIGH and the other is tied LOW. The address-sciect and enable inputs are configured such that toggling one address input selects the two data inputs alternately, causing the susports to toggle. With three-state multiplexers, CpD is specified per output feaction for enabled outputs.

Bilateral switches. The switch inputs and outputs are opencircuit. With the enable lopus active, one of the select inputs is toggled, the others are fied RIGH or LOW, Cpg is specified per switch.

Three-state buffers and transceivers. Cop is specified per outfer with the outputs enabled. Measurement is as far simple gardes.

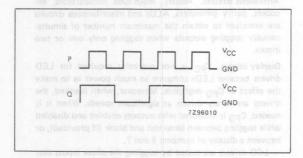
Larches. The device is clocked and data is regaled on alternate clock pulses. Other preser or clear inputs are held so that output toggling is enabled. If the device has common-locking latches, one laten is toggled by the clock. Three-state latches are measured with their outputs enablid. Cpt is specified per latch.

Flip-flops, Messurement is performed as for larches. The inputs to the device are toggled and any preset or clear inputs are held inactive.

Shift registers. The register is clocked and the strial data input is toggled at alternate chock pulses (as osciolad for latches). Clear and load inputs are held inactive and parallel data are neld at VCC or GND. Three-state devices are measured with outputs enabled. If the device is for parallel loading only, it is loaded with 101010..., clocked to thirt the data out and then reloaded.

Counters. A signal Is applied to the clock input but other lear or load inputs are held inactive. Separate values for Cop are given for each ocuprer in the device.

Input pulses



control the segment and naciplane waveforms outputs.

then the lauches are set to a flow-through mode.

Oceahat riquits. In some cases, when the device $I_{\rm CC}$ is separation, $C_{\rm PD}$ is not specified. When it is specified, $C_{\rm PD}$ is measured by reggling one trigger input to make the output a squarewaye. The timing resistor is field to a separate supply (equal to $V_{\rm CC}$) to eliminate its power contribution.

Additional power dissipation in TAHCT devices

When the inputs of a 74HCT device are driven by a TTC device at the specified minimum HIGH output level of $V_{\rm OH} = 2.4$ $\rm M_{\odot}$, the input stage p-channel transistor does not completely switch off and there is an additional quiescent upply current ($\Delta I_{\rm CC}$). This current has been considerably educed by proprietary development of 74HCT input rages, see 74HCT inputs.

The value of $\Delta I_{\rm CO}$ specified in the data sheats is par input and at the worst-case input voltage of $V_{\rm CC}$ 2.1 V for $V_{\rm CC}$ between 4.5 and 5.5 V. The value of 2.1 V is the maximum voltage drop across a TTL output HIGH (minimum $V_{\rm CC}$) and minimum $V_{\rm CR}$), see Table 9.

The additional power distingation P is:

S - ACC x TICC x onth jeclos HICH x nut long coefficient

The unit load coefficient for an input is a factor by which the value of $\Delta t_{\rm CC}$ given in the data sheet has to be multiplied. A unit load coefficient is published for each Z4HCT levice. It is a function of the size of the input prohammal vanistor.

Conditions for CpD tests

Gates. All inputs except one are held at either V_{CC} or GND, depending on which state causes the output to toggle. The remaining input is toggled at a known frequency. C_{PD} is specified per-gate.

Decoders. One input is toggled, causing the outputs to toggle at the same rate (normally one of the address-select pins is switched while the decoder is enabled). All other inputs are tied to $V_{\hbox{CC}}$ or GND, whichever enables operation. CpD is specified per-independent-decoder.

Multiplexers. One data input is tied HIGH and the other is tied LOW. The address-select and enable inputs are configured such that toggling one address input selects the two data inputs alternately, causing the outputs to toggle. With three-state multiplexers, C_{PD} is specified per output function for enabled outputs.

Bilateral switches. The switch inputs and outputs are opencircuit. With the enable input active, one of the select inputs is toggled, the others are tied HIGH or LOW. C_{PD} is specified per switch.

Three-state buffers and transceivers. C_{PD} is specified per buffer with the outputs enabled. Measurement is as for simple gates.

Latches. The device is clocked and data is toggled on alternate clock pulses. Other preset or clear inputs are held so that output toggling is enabled. If the device has common-locking latches, one latch is toggled by the clock. Three-state latches are measured with their outputs enabled. CpD is specified per-latch.

Flip-flops. Measurement is performed as for latches. The inputs to the device are toggled and any preset or clear inputs are held inactive.

Shift registers. The register is clocked and the serial data input is toggled at alternate clock pulses (as described for latches). Clear and load inputs are held inactive and parallel data are held at $V_{\rm CC}$ or GND. Three-state devices are measured with outputs enabled. If the device is for parallel loading only, it is loaded with 101010..., clocked to shift the data out and then reloaded.

Counters. A signal is applied to the clock input but other clear or load inputs are held inactive. Separate values for C_{PD} are given for each counter in the device.

Arithmetic circuits. Adders, magnitude comparators, encoders, parity generators, ALUs and miscellaneous circuits are exercised to obtain the maximum number of simultaneously toggling outputs when toggling only one or two inputs.

Display drivers. C_{PD} is not normally required for LED drivers because LEDs consume so much power as to make the effect of C_{PD} negligible. Moreover, when blanked, the drivers are rarely driven at significant speeds. When it is needed, C_{PD} is measured with outputs enabled and disabled while toggling between lamp test and blank (if provided), or between a display of numbers 6 and 7.

LCD drivers are tested by toggling the phase inputs that control the segment and backplane waveforms outputs.

If either type of driver (LCD or LED) has latched inputs, then the latches are set to a flow-through mode.

One-shot circuits. In some cases, when the device I_{CC} is significant, C_{PD} is not specified. When it is specified, C_{PD} is measured by toggling one trigger input to make the output a squarewave. The timing resistor is tied to a separate supply (equal to V_{CC}) to eliminate its power contribution.

Additional power dissipation in 74HCT devices

When the inputs of a 74HCT device are driven by a TTL device at the specified minimum HIGH output level of V_{OH} = 2.4 V, the input stage p-channel transistor does not completely switch off and there is an additional quiescent supply current (ΔI_{CC}). This current has been considerably reduced by proprietary development of 74HCT input stages, see '74HCT inputs'.

The value of ΔI_{CC} specified in the data sheets is per input and at the worst-case input voltage of V_{CC} -2.1 V for V_{CC} between 4.5 and 5.5 V. The value of 2.1 V is the maximum voltage drop across a TTL output HIGH (minimum V_{CC} and minimum V_{OH}), see Table 9.

The additional power dissipation P is:

P = V_{CC} x ΔI_{CC} x duty factor HIGH x unit load coefficient

The unit load coefficient for an input is a factor by which the value of Δl_{CC} given in the data sheet has to be multiplied. A unit load coefficient is published for each 74HCT device. It is a function of the size of the input p-channel transistor.

Table 9: Worst-case additional quiescent supply current (ΔI_{CC}) for 74HCT devices

	T _{amb} (°C)					TEST CONDITIONS		
	74HCT							
	+25		-40 to +85	-40 to +125	UNIT	V _{CC}	V ₁	OTHER
	typ.	max.	max.	max.		Altrius]	bors spirit	
ΔI _{CC} per input pin for a unit load coefficient of 1*	100	360	450	490	μΑ	4.5 to 5.5	V _{CC} -2.1 V	other inputs at V _{CC} or GND I _O = 0

^{*} The additional quiescent supply current per input is determined by the ΔI_{CC} unit load, which has to be multiplied by the unit load coefficient as given in the individual data sheets. For dual supply systems the theoretical worst-case (V_I = 2.4 V; V_{CC} = 5.5 V) specification is: ΔI_{CC} = 0.65 mA (typical) and 1.8 mA (maximum) across temperature.

Power dissipation due to slow input rise/fall times

When an output stage switches, there is a brief period when both output transistors conduct. The resulting 'through-current' is additional to the normal supply current and causes power dissipation to increase linearly with the input rise or fall time.

As long as the input voltage is less than the n-channel transistor threshold voltage, or is higher than V_{CC} minus the p-channel transistor threshold voltage, one of the input transistors is always off and there is no through-current.

When the input voltage equals the n-channel transistor threshold voltage (typ. 0.7 V), the n-channel transistor starts to conduct and through-current flows, reaching a maximum at V_I = 0.5 V_{CC} for 74HC devices, and V_I = 28%V_{CC} for 74HCT devices, the maximum current being determined by the geometry of the input transistors. The through-current is proportional to V_{CC}ⁿ where n is about 2.2. The supply current for a typical HCMOS input is shown as a function of input voltage transient in Fig.14.

When Schmitt triggers are used to square pulses with long rise/fall times, through-current at the Schmitt-trigger inputs will increase the power dissipation, see Schmitt-trigger data sheets. In the case of RC oscillators, or oscillators constructed with Schmitt triggers this contribution to the power dissipation is frequency-dependent.

Comparison with LSTTL power dissipation

The dynamic power dissipation of a HCMOS device is frequency-dependent; above 1 MHz, that of an LSTTL device is too. Below 1 MHz, the dynamic component of power dissipation of an LSTTL device is negligible compared to the static component. Figure 15 shows the average power dissipation of four HCMOS devices and their LSTTL equivalents. Because all functions in a multi-functional LSTTL device are biased when power is applied, for comparison, the dissipation of whole HCMOS devices besides individual functions are given.

In Fig.15 it can be seen that:

- for SSI gate types, the HCMOS power dissipation is less than LSTTL power dissipation below about 1 MHz
- for more complex types such as a 74HC/HCT138 3-to-8 line decoder HCMOS power dissipation is less than LSTTL power dissipation up to 10 MHz.

In typical microcomputer systems, the operating frequency or the data/address signal rates will usually vary, whereas Fig.15 is for continuous operation at a constant frequency. Average operating frequencies are usually far below the peak frequencies, particularly in the 100 kHz region where the power dissipation of HCMOS is several orders of magnitude less than that of LSTTL.

For further information, see chapter 'Power dissipation'.

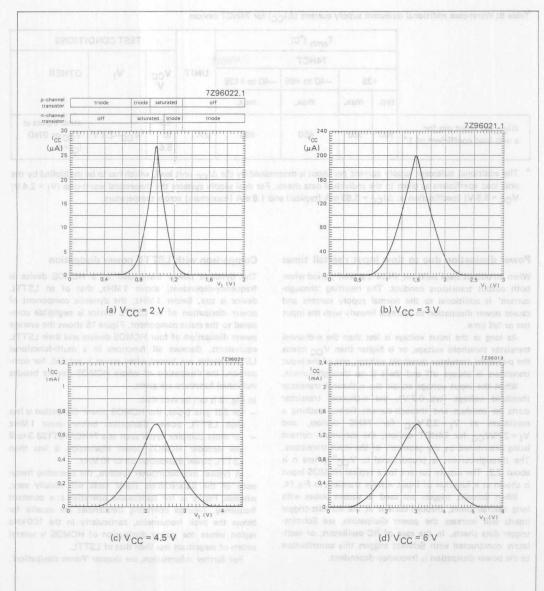
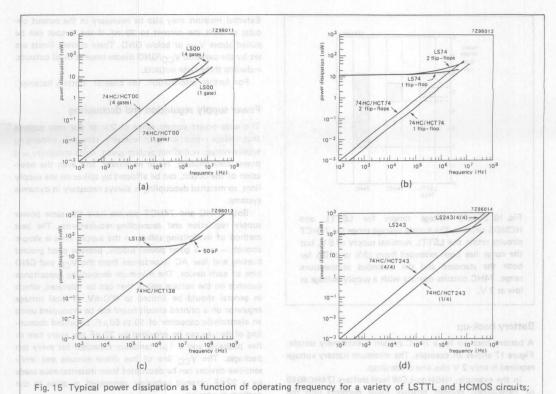


Fig. 14 Typical DC supply current as a function of input voltage for 74HC circuits; normalized curves for a unit load coefficient of 1. The I_{CC} for a specific 74HC circuit can be calculated by multiplying the values of I_{CC} shown by the unit load coefficient for the 74HCT type given in the data sheet.



(a) quad 2-input NAND gate, (b) dual D-type flip-flop, (c) 3-to-8 line decoder/demultiplexer; inverting, (d) quad 3-state bus transceiver.

SUPPLY VOLTAGE

Range

The supply voltage range of 74HC devices is 2 V to 6 V (Fig.16). This ensures continued use of HCMOS with future generations of memory and microcomputer requiring supply voltages of less than 5 V, simplifies the regulation requirements of power supplies, facilitates battery operation and allows lithium battery back-up. When 74HC devices are used in linear applications, for example when they are used as RC oscillators, a supply of at least 3 V is recommended to ensure sufficient margin for operation in the linear region.

74HCT devices are pin-compatible with LSTTL circuits and are intended as power-saving replacements for them. The 74HCT devices will operate from the traditional 5 V LSTTL supply, but the voltage range is extended to $\pm 10\%$ for both LSTTL temperature ranges (-40 to +85°C and

-40 to +125 °C). This allows extended temperature range LSTTL devices to be replaced by 74HCT devices.

The absolute maximum supply or ground current per pin is ± 50 mA for devices with standard output drive, and ± 70 mA for devices with bus driver outputs. These currents are only drawn when the outputs of a device are heavily loaded. The average dynamic current at very high frequencies can be calculated using C_{PD} .

The maximum rated supply voltage of HCMOS devices is 7 V and any voltage above this may destroy the device, even though the on-chip parasitic diode break-down voltage is at least 20 V and the threshold voltage of parasitic thick-field oxide transistors is 15 V.

The $V_{\hbox{\scriptsize CC}}$ and GND potentials must never be reversed as this can cause excessive currents to flow through the input protection diodes.

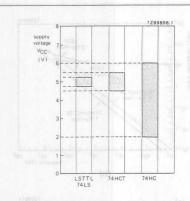
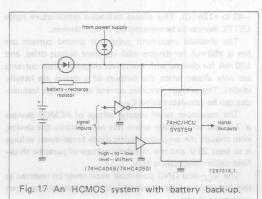


Fig. 16 Supply voltage ranges for LSTTL and HCMOS circuits. The supply voltage range for 74HCT circuits retain the LSTTL nominal supply of 5 V, but the range has been extended from $\pm 5\%$ to $\pm 10\%$ for both the standard and the extended temperature range. 74HC circuits operate with a supply voltage as low as 2 V.

Battery back-up

A battery back-up for a 74HC system is extremely simple. Figure 17 shows an example. The minimum battery voltage required is only 2 V plus one diode drop.

In the example, HIGH-to-LOW level shifters (74HC4049 or 74HC4050) prevent positive input currents into the system due to input signals greater than one diode drop above V_{CC} . If the circuit is such that input voltages can exceed V_{CC} , external resistors should be included to limit the input current to 15 mA for one input (7.5 mA per input for two inputs, 5 mA per input for three inputs, etc.).



External resistors may also be necessary in the output circuits to limit the current to 20 mA if the output can be pulled above V_{CC} or below GND. These current limits are set by the parasitic V_{CC}/GND diodes present in all outputs, including three-state outputs.

For further information, see chapter 'Battery back-up'.

Power supply regulation and decoupling

The wide power supply range of 2 V to 6 V may suggest that voltage regulation is unnecessary. However, a changing supply voltage will affect system speed, noise immunity and power consumption. Noise immunity, and even the operation of the circuit, can be affected by spikes on the supply lines, so matched decoupling is always necessary in dynamic systems.

Both 74HC and 74HCT devices have the same power supply regulation and decoupling requirements. The best method of minimizing spikes on the supply lines is simple enough - use a good power supply, provide good ground bussing and low AC impedances from the Vcc and GND pins of each device. The minimum decoupling capacitance depends on the voltage spikes that can be tolerated, which in general should be limited to 400 mV. A local voltage regulator on a printed circuit board can be decoupled using an electrolytic capacitor of 10 to 50 uF. Localized decoupling of devices can be provided by 22 nF per every two to five packages and a 1 µF tantalum capacitor for every ten packages. The VCC line of bus driver circuits and levelsensitive devices can be decoupled from instantaneous loads by a 22 nF ceramic capacitor connected as close to the package as possible.

For further information, see chapter 'Power supply decoupling'.

INPUT/OUTPUT PROTECTION

The gate input of a MOS transistor acts as a capacitor (<1 pF) with very low leakage current (<1 pA). Without protection, such an input could be electrostatically charged to a high voltage that would breakdown the dielectric and permanently damage the device.

The integration process of the HCMOS family allows polysilicon resistors to be formed at all inputs to slow down fast input transients caused by electrostatic discharge and to dissipate some of their energy. These resistors also ensure that the input impedance of an HCMOS device is typically $100\,\Omega$ under all biasing conditions, even when V_{CC} is short-circuited to GND — an improvement over direct input diode clamps during power-up.

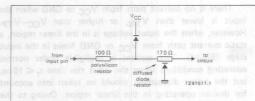


Fig. 18 Standard input protection of 74HC/HCT/HCU inputs against electrostatic discharge.

The standard input protection comprises a series polysilicon resistor and two stages of diode clamping (Fig.18). The typical forward voltage of the diodes is 0.9 V at 2 mA and the reverse breakdown voltage is 20 V. In some applications such as oscillators, the diodes conduct during normal operation, in which case the input current should be limited. The maximum positive input current +I_{1K} per input is 20 mA. For devices with a standard output, the total positive input current is 50 mA; for devices with a busdriver output, the total input current is 70 mA. The maximum negative input current —I_{1K} per pin is:

14 mA for one input

9 mA for two inputs

6 mA for three inputs

5 mA for four inputs

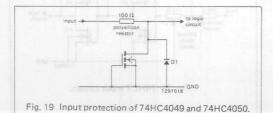
4 mA for five inputs

3 mA for six to eight inputs.

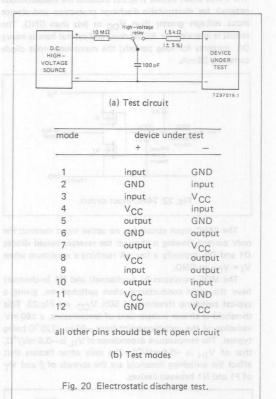
High-to-low level shifters 74HC4049 and 74HC4050 have a single-sided input protection network (Fig.19) which protects against electrostatic input voltages. The diode D1 is the parasitic drain-to-GND diode of the thick field oxide protection device.

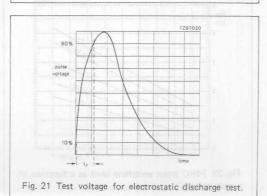
All input pins can withstand discharge voltages up to $2.5\,\mathrm{kV}$ (typ.) when tested according to MIL-STD-883B, method 3015, see Fig.20. The output configurations of standard, bus driver, three-state, open drain and I/O ports can withstand $>3.5\,\mathrm{kV}$ (typ.) because of the large diodes formed by the drain surfaces of the output transistors.

Figure 21 shows the voltage pulse for the discharge test. The rise time t_Γ prescribed by MIL-STD-883B is \leq 15 ns, but in practice it is helpful to adjust the test set-up to give a rise time of 13 ± 2 ns to avoid correlation problems.



Although all inputs and outputs are protected against electrostatic discharge, the standard CMOS handling precautions should be observed (see chapter 'Handling precautions').

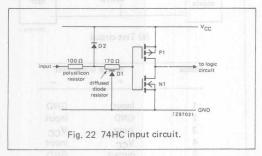




INPUT CIRCUITS and has study lie decortile

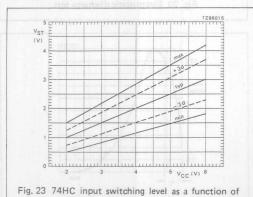
74HC inputs seel havreado ed bluode anomusoarq

The 74HC input circuit (Fig.22) includes the resistor/diode network for electrostatic discharge protection and clamps input voltages greater than $V_{\rm CC}$ or less than GND. The circuit is intended for AC working and cannot handle heavy DC currents for long periods; the maximum input diode current is 20 mA.



The 74HC input circuit has no active input current; the only current flowing is through the reversed-biased diodes D1 and D2, typically a few nA reaching a maximum when $V_1 = V_{CC}$ or GND.

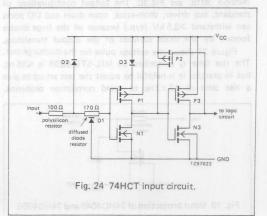
The MOS transistors P1 (p-channel) and N1 (n-channel) have the same conductance when switched on, giving a typical switching threshold of 50% V_{CC} , see Fig.23. This threshold is almost independent of temperature, a $\pm 60~\text{mV}$ variation of the switching point from -40~to +125 °C being typical. The temperature dependence of V_{1L} is $-0.6~\text{mV}/^\circ\text{C}$, that of V_{1H} is $+0.6~\text{mV}/^\circ\text{C}$. The only other factors that affect the switching threshold are the spreads of β and V_T of P1 and N1 between devices.



There is no current path from V_{CC} to GND when the input is lower than V_{TN} , or higher than $V_{CC} - V_{TP}$. However, when the input voltage is in the linear region, a static current path from V_{CC} or GND flows in the input stage (Fig.14). This current is negligible under normal operating conditions when the input rise time $t_r \leqslant 15 \, \text{ns}$, but the power dissipation should be taken into account for devices operating in the linear region. Owing to the voltage gain of the input stage, there is no static flow-through current in the second and subsequent stages. Small currents do flow in these stages during operation when both n-channel and p-channel transistors conduct for brief periods and their effect is included in the C_{PD} value in the data sheets.

74HCT inputs to an analysis and an analysis an

The 74HCT input stage is similar to that of a 74HC device. It has the same characteristics for LSTTL levels as a 74HC input has for CMOS levels, so there is no trade-off in speed or power dissipation. The switching threshold is lower, 1.4 V at $V_{CC}=5\,\rm V$. In addition, the 74HCT input circuit, shown in Fig.24, has an enlarged n-channel transistor (N1) and a level-shift diode (D3) has been added. The natural drain voltage of the p-channel transistor (P1) is approximately V_{CC} —0.6 V, but when the input voltage is LOW, an auxiliary pull-up transistor (P2) raises this to V_{CC} , cutting off p-channel transistor P3 completely. The input stage is well matched to the load presented by the second stage so that symmetrical propagation delays are obtained.



supply voltage.

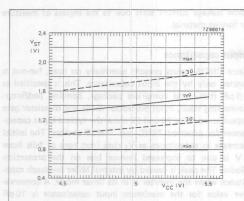


Fig. 25 74HCT input switching level as a function of supply voltage.

Figure 25 shows the switching level as a function of supply voltage.

A TTL HIGH level can be as low as 2.4 V. An input of this order to a HCMOS device would not cut off P1 completely, and additional supply current would flow through the input stage. A level-shift diode D3 and the influence of the back-gate (substrate) connection to P1 minimizes power dissipation caused by this through-current and gives an input switching level compatible with LSTTL. Figure 26 shows the input stage through-current with and without the diode circuit. The peak in the curve occurs at the input switching threshold.

The input stage through-current is virtually zero for a typical TTL HIGH level input of 3.5 V. Thus, this unique 74HCT input structure gives true CMOS low power-consumption when driven by TTL. Typical and maximum through-currents ΔI_{CC} per input are given in the data sheets.

In a system where 74HCT devices are only driven by LSTTL devices, $V_{OH\ min}$ can be 2.7 V except for some bus drivers. With V_{OH} = 2.7 V, ΔI_{CC} is half the published value,

Maximum input rise/fall times

All digital circuits can oscillate or trigger prematurely when input rise and fall times are very long. When the input signal to a device is at or near the switching threshold, noise on the line will be amplified and can cause oscillation which, if the frequency is low enough, can cause subsequent stages to switch and give erroneous results. For this reason, Schmitt-triggers are recommended if rise/fall times are likely to exceed 500 ns at $V_{\rm CC}$ = 4.5 V.

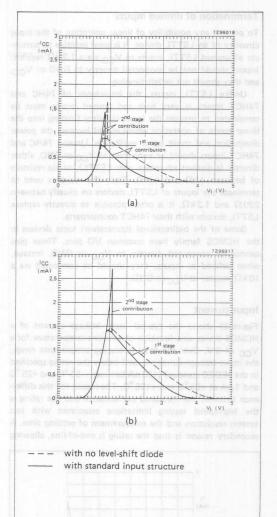


Fig. 26 Additional quiescent supply current ΔI_{CC} (typ.) per input pin of a 74HCT device as a function of supply voltage (unit load coefficient is 1); (a) $V_{CC} = 4.5 \, \text{V}$, (b) $V_{CC} = 5.5 \, \text{V}$.

The flip-flops 74HC/HCT73, 74, 107, 109 and 112 incorporate Schmitt-trigger input circuits and the 74HC/HCT14 and 132 are dedicated Schmitt triggers with specified input levels.

For further information, see chapter 'Schmitt trigger applications'.

Termination of unused inputs

To prevent any possibility of linear operation of the input circuitry of an LSTTL device, it is good practice to terminate all unused LSTTL inputs to V_{CC} via a 1.2 k Ω resistor. Inputs should not be connected directly to GND or V_{CC} , and they should not be left floating.

Unlike LSTTL inputs, the impedance of 74HC and 74HCT inputs is very high and unused inputs must be terminated to prevent the input circuitry floating into the linear mode of operation which would increase the power dissipation and could cause oscillation. Unused 74HC and 74HCT inputs should be connected to V_{CC} or GND, either directly (a distinct advantage over LSTTL), or via resistors of between $1\,\mathrm{k}\Omega$ and $1\,\mathrm{M}\Omega$. Since the resistors used to terminate the inputs of LSTTL devices are usually between $220\,\Omega$ and $1.2\,\mathrm{k}\Omega$, it is often possible to directly replace LSTTL circuits with their 74HCT counterparts.

Some of the bidirectional (transceiver) logic devices in the HCMOS family have common I/O pins. These pins cannot be connected directly to V_{CC} or GND. Instead, when defined as inputs, they should be connected via a 10 k Ω resistor to V_{CC} or GND.

Input current

Figure 27 shows the typical input leakage current of a HCMOS device as a function of ambient temperature for a V_{CC} of 6 V. Over the total operating temperature range, the input leakage current is well below the rating specified in the JEDEC standard (100 nA between $-55\,^{\circ}\mathrm{C}$ and $+25\,^{\circ}\mathrm{C}$ and $1\,\mu\mathrm{A}$ at +85 $^{\circ}\mathrm{C}$ and +125 $^{\circ}\mathrm{C}$. The reason for this difference between the measured performance and the rating is the high-speed testing limitations associated with test system resolution and the measurement of settling time. A secondary reason is that the rating is end-of-line, allowing

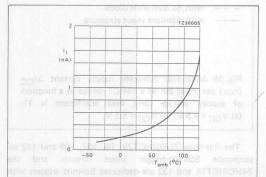


Fig. 27 Typical HCMOS input leakage current I₁ as a function of ambient temperature T_{amb}.

some leakage current shift due to the ingress of moisture or foreign material.

Input capacitance

Since CMOS inputs present essentially no load, fan-out is limited only by the input capacitance. This is specified as $3.5\,\mathrm{pF}$ (typ.) and comprises package, bonding pad/interconnecting track, input protection diode and transistor gate capacitances. Figs 28 and 29 show the typical input capacitances for powered 74HC and 74HCT devices. The initial decrease in capacitance as V_1 rises from zero or falls from 5 V is due to increased reverse bias on the protection diodes. The peak is caused by internal Miller feedback capacitance when the inverter is in its linear mode. A conservative value for the maximum input capacitance is $10\,\mathrm{pF}$ (20 pF for I/O pins owing to the output drain capacitance). Input capacitance is measured with all other inputs tied to ground.

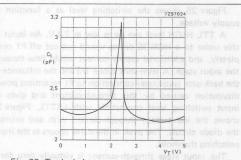


Fig. 28 Typical input capacitance C_1 of a 74HC device as a function of input voltage; V_{CC} = 5 V; T_{amb} = 25 °C.

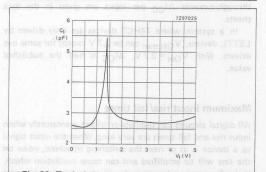


Fig. 29 Typical input capacitance C_{\parallel} of a 74HCT device as a function of input voltage; V_{CC} = 5 V; T_{amb} = 25 °C.

V_{CC} = 5 V

parasitic pnp

HCMOS device

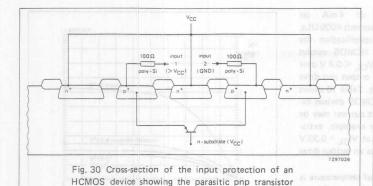


Fig. 31 12 V-to-5 V logic-level conversion at HCMOS inputs using 100 $k\Omega$ series resistors.

V1L(2)

Coupling of adjacent inputs

Parasitic bipolar pnp transistors can be present between adjacent inputs, e.g. between an input protection diode to V_{CC} and the same diode at the adjacent input, as shown in Fig.30. If the recommended operating input voltage is exceeded, perhaps by ringing of more than 0.7 V, current into the terminal (I_1) can cause a current I_2 in the parasitic transistor and in the adjacent input (Fig.31). Because I_2 in the adjacent input has to be drained by the source driving that input, the source resistance (R) must be low. If R is not low enough, the parasitic current can lift the source voltage and cause unwanted switching.

between adjacent inputs.

The ratio of the parasitic adjacent input current (I2) to the forced input current (I1) denoted α :

$$\alpha = \frac{l_2}{l_1}$$
.

 α has been reduced to less than 0.05 (typically 0.001) in the HCMOS family by the use of deep guard rings and optimum bonding pad spacing.

A low α permits proper logic operation in the presence of transients and also allows HIGH-to-LOW voltage translation simply by adding series input resistors. For example, in Fig.31, 12 V system logic is converted to 5 V system logic by adding a 100 k Ω resistor in each input. Since the logic signals are delayed by 1-2 μs , this arrangement is suitable for rather slow 12 V control logic such as that in automotive applications. When the input diodes are used as clamps for logic level translation, the total input current should be limited to 20 mA.

Input voltage and forward diode input current

As a general rule, CMOS logic devices with input clamp diodes (Fig.18) should be operated between the power

supply rails. Neglecting the input series polysilicon resistor shown in Fig.18, this means: $-0.5 \text{ V} \leq \text{V}_1 \leq \text{V}_{CC} + 0.5 \text{ V}$.

100kΩ

This rule is JEDEC Std. No. 7A and is intended to prevent users damaging devices similar to HCMOS that do not have the polysilicon resistor. HCMOS devices however meet the tougher rating: $-1.5\,\text{V} \leqslant \text{V}_1 \leqslant \text{V}_{CC} + 1.5\,\text{V}$. Furthermore, virtually all HCMOS devices can operate reliably up to the rating without logic errors.

The maximum permissible continuous current forced into an input or output of a HCMOS device is ±20 mA (JEDEC rating).

OUTPUT CIRCUITS

Output drive

There are three different output configurations in the HCMOS family:

- push-pull
- three-state
- open-drain n-channel transistor.

Each is available with a standard output or a bus driver output, the latter having 50% more drive capability. All 74HC and 74HCT outputs are buffered for consistent current drives and AC characteristics throughout the HCMOS family. Well-matched output n-channel and p-channel transistors give symmetrical output rise and fall times.

When comparing the output drive capabilities of HCMOS with those of LSTTL, note that LSTTL capability is usually expressed in unit loads (ULs) where the load is specified to be an input of the same family. This guarantees that a system will operate correctly with worst-case LOW and HIGH input signals and that noise immunity margins will be preserved. HCMOS capability is expressed as the source or sink current at a specified output voltage. Since HCMOS requires virtually no input current, the unit load concept is not applicable.

With a specified output drive of 4 mA (at $V_{OLmax} = 0.4 \text{ V}$), the HCMOS capability exceeds 4000 ULs, and with a $20\,\mu\text{A}$ (at $V_{OL} = 0.1 \text{ V}$) specification the HCMOS capability is 20 ULs. A standard HCMOS output can drive ten LSTTL loads and maintain $V_{OL} \le 0.4 \text{ V}$ over the full temperature range. A bus driver output can drive 15 LSTTL loads under the same conditions. Table 10 shows the output drive capabilities of some HCMOS devices expressed in LSTTL unit loads. The output current may be increased for higher output voltages. For example, extrapolating the 6 mA bus driver capability at $V_{OL} = 0.33 \text{ V}$ and $V_{OL} = 0.33 \text{ V}$

Output current derating as a function of temperature is shown in Fig.32 and is valid for all types of output. Output source and sink drives at $V_{\rm CC}$ = 2 V, 4.5 V and 6 V are given in Figs 33 to 36 which show the output current as a function of output voltage; these graphs indicate the typical output currents and the expected minimum output currents. They can serve as a design aid when calculating transmission line effects or when charging highly capacitive loads.

The expected minimum curves are not guaranteed; they are tested only at the values given in the data sheets.

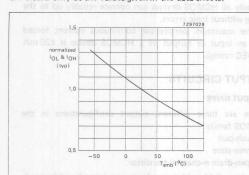


Fig. 32 Derating curve for output drive currents $I_{\mbox{\scriptsize OL}}$ and $I_{\mbox{\scriptsize OH}}$

Table 10: Comparison of the output drive capabilities of LSTTL and HCMOS (V $_{O.1} \le 0.4 \text{ V}$)

LS device	output	drive capacity	HCMOS equiv.	type	output	drive capacity
74LS00	4 mA	10 UL			4 mA	10 UL
74LS138	4 mA	10 UL	75HC138	standard	4 mA	10 UL
74LS245	12 mA	30 UL	74HC245	bus	6 mA	15 UL
74LS374	12 mA	30 UL	74HC374	bus	6 mA	15 UL

UL = unit load.

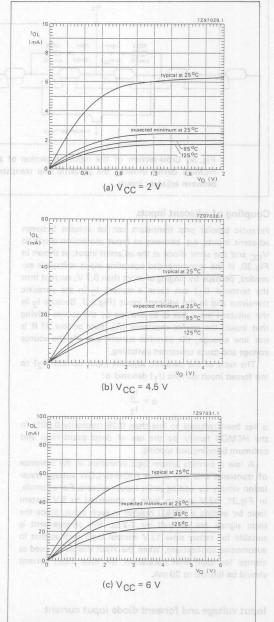
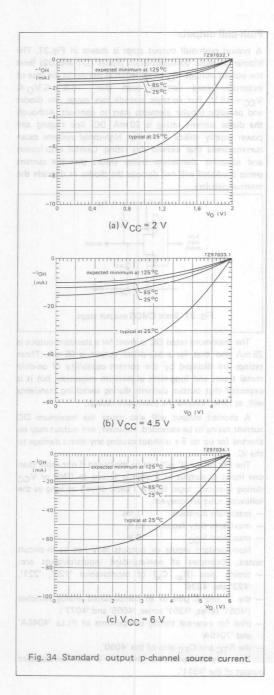
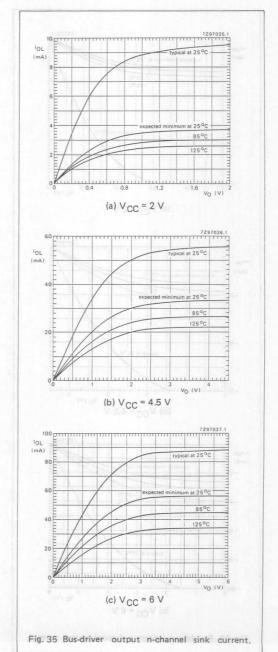
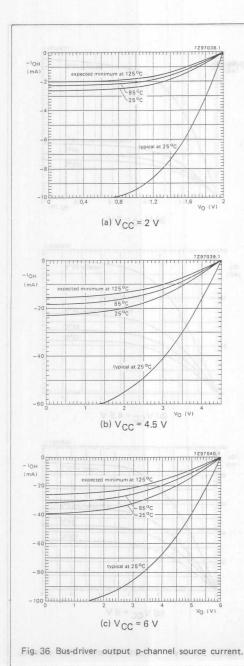


Fig. 33 Standard output n-channel sink current.

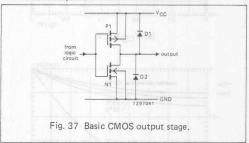






Push-pull outputs

A typical push-pull output stage is shown in Fig.37. The bipolar parasitic transistor-drain diodes (D1 and D2) limit the output voltage $V_{\hbox{\scriptsize O}}$ of all HCMOS devices in the case of externally-forced voltages such that $-0.5~{\rm V} \leqslant V_{\hbox{\scriptsize O}} \leqslant V_{\hbox{\scriptsize CC}} + 0.5~{\rm V}$. For voltages outside this range, the diodes and parasitic bipolar elements start to conduct. Although the diode current rating is 20 mA DC, line ringing and power supply spikes in normal high-speed systems cause current-peaks that exceed this rating. Careful chip-layout and adequate aluminium traces ensure that the current peaks produced will not damage the diodes or degrade the internal circuitry.



The maximum rated DC current for a standard output is 25 mA and that for a bus-driver output is 35 mA. These ratings are dictated by the current capability of on-chip metal traces and long-term aluminium migration, but it is expected that output currents during switching transients will, at times, exceed the maximum ratings.

A shorted output will also cause the maximum DC current rating to be exceeded. However, one output may be shorted for up to 5 s without causing any direct damage to the IC.

The life of the IC will not be shortened if not more than one input or output at a time is forced to GND or $V_{\rm CC}$ during in-circuit logic testing ('back drive') as long as the following rules are obeyed:

- maximum duration : 1 ms
- maximum duty factor: 10 %
- maximum V_{CC} : 6 V

Non-standard inputs or outputs may not be in-circuit tested. Examples of non-standard inputs/outputs are:

- timing pins (R $_{\rm X},$ C $_{\rm X})$ of monostables '123', '221', '423' and '4538'
- the Y and Z pins of all compensated analog switches ('4051' series, '4351' series, '4066' and '4077')
- pins for external timing components of PLLs '4046A' and '7046A'
- the $R_{\mbox{\scriptsize TC}}$ and $C_{\mbox{\scriptsize TC}}$ pins of the '4060'.

The only exception to this rule is the non-standard output of the '4511'.

Three-state outputs

In the typical three-state output circuit shown in Fig.38, when EO is HIGH the output is enabled and transistors P4 and N4 act as a transmission gate connecting the gates of the output transistors. A LOW at EO puts the output in the high-impedance OFF-state and transistors P3 and N3 act as pull-up and pull-down transistors respectively. The logic symbol for a three-state output and its function table is shown in Fig.39.

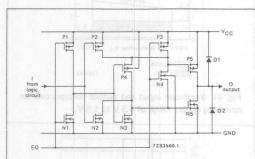
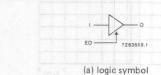


Fig. 38 Typical three-state output circuit.



in	puts	outp	uts
1	EO	0	
X	L	Z	113
L	Н	L	
Н	Н	Н	

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

(b) function table

Fig. 39 Three-state output logic symbol and functions.

Three-state outputs are designed to be tied together but are not intended to be active simultaneously. To minimize noise and to protect outputs from excessive power dissipation, only one three-state output should be active at any time. In general, this requires that the output enable signals should not overlap. When decoders are used to enable three-state outputs, the decoder should be disabled while the address is being changed. This avoids overlapping output-enable signals caused by decoding spikes to which all decoder outputs are prone during address-changing.

When designing with three-state outputs, note that disable propagation delays are measured for an RC load when the output voltage has changed by 10% of the voltage swing. This 10% level is adequate to ensure that a device output has turned off. Although this method provides a standard reference for measuring disable times, it implies that the output is already off for 10% of the RC time. Because all disable times are measured with a load of $1\,\mathrm{k}\Omega$ and $50\,\mathrm{pF}$, subtract the 10% RC time (5 ns) from the values published in the data sheets to obtain the real internal disable propagation delay.

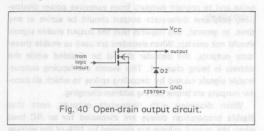
Diodes D1 and D2 are parasitic diodes associated with output transistors P5 and N5 respectively. Diode D1 clamps the output at one V_{BE} above V_{CC} , of importance in large systems where sections of the system may be powered-down (V_{CC} = 0 V), in which case the output diode current has to be limited to 20 mA.

All I/O ports and transceivers have a three-state output as shown in Fig.38. The I/O pin is defined as an input when the output is disabled, but this pin should be regarded as a real input and should not be left floating, because the input to an I/O port can cause V_{CC} current. If necessary, terminate the input with a $10\,\mathrm{k}\Omega$ resistor, see 'Termination of unused inputs',

Open-drain outputs

In TTL families, several functions are offered with opencollector outputs to enhance logic functions by using ORtied logic. The advantage of OR-tied logic is the logic elements saved and hence the lower power dissipation. However, this is countered by power loss and reliance on RC time propagation delays. These disadvantages are not encountered in CMOS and similar applications can be made using devices with 3-state outputs, or simply with the power-saving logic devices. However, the 74HC/HCT03 (quad 2-input NAND gate) has an open-drain n-channel output, see Fig.40. The parasitic diode D1 is not present (there being no p-channel transistor); this allows the output voltage to be pulled above V_{CC} to V_{Omax} making both HIGH-to-LOW and LOW-to-HIGH level-shifting possible. For digital operation, a pull-up resistor is necessary to establish a logic HIGH level.

The open-drain output is protected against electrostatic discharge.



Increased drive capability of gates

To increase output drive, the inputs and outputs of gates in the same package may be connected in parallel. It is advisable to restrict parallel connection to gates within one package to avoid large transient supply currents due to different gate-switching times.

For further information, see chapter 'Interfacing and protection of circuit board inputs'.

Output capacitance

For push-pull outputs, no output capacitance is specified because either the n-channel transistor or the p-channel transistor creates a low-impedance path to the supply rails.

Three-state outputs can be switched to the high impedance OFF-state, and because many of them can be connected to a bus line, the output capacitance is needed to calculate the total capacitive load. For bus-driven 3-state outputs in a DIL package, the output capacitance is 6 pF (typ.) and 20 pF (max.).

STATIC NOISE IMMUNITY

The static noise immunity can be divided into:

- the static noise margin LOW. This is the voltage difference between V_{ILmax} of the driven device and V_{OLmax} of the driver.
- the static noise margin HIGH. This is the difference between V_{OHmin} of the driver and V_{IHmin} of the driven device.

For 74HC devices, both the LOW level noise margin and the HIGH-level noise margin is 28% of $V_{CC}.$ This is a considerable improvement over LSTTL where the LOW-level noise margin is only 8% of V_{CC} and the HIGH level noise margin is just 14% of $V_{CC}.$ The margins are even greater for HCMOS at higher supply voltages as shown in Fig.41. As 74HCT devices have the same switching levels as LSTTL, their noise margins are also the same.

The superior noise immunity of the 74HC input can be clearly seen from the voltage levels of the input-to-output transfer characteristics shown in Figs 42 and 43.

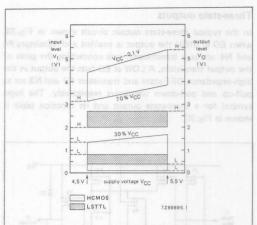


Fig. 41 Worst-case input and output voltages over an operating supply range of 4.5 V to 5.5 V.

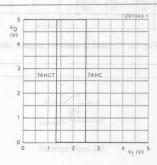


Fig. 42 Typical input-to-output transfer characteristic for 74HC and 74HCT devices.

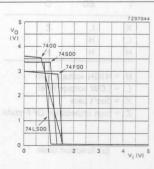


Fig. 43 Input-to-output transfer characteristics for TTL devices.

Table 11 shows the input noise margin of HCMOS devices where like devices are interfaced. Output voltages are also given.

Table 11: Noise immunity and noise margin for HCMOS devices ($V_{CC} = 4.5 \text{ V}$)

			The second secon			
		74HC	74HCT	74HCU		
V _{ILmax}	(V)	1.35	0.8	0.9		
VIHmin	(V)	3.15	2	3.6		
VOLmax	(V)	0.1	0.1	0.5		
VOHmin	(V)	4.4	4.4	4		
Noise margin	low					
VNML	(V)	1.25	0.7	0.4		
Noise margin	high					
VNMH	(V)	1.25	2.4	0.4		

Table 12 shows the input noise margin of 74HCT devices interfacing with LSTTL devices; the 74HCT or LSTTL output is fully-loaded, V_{CC} = 4.5 V and T_{amb} is 0 °C to +70 °C (the only convenient temperature range when using LSTTL characteristics).

Table 12: Noise immunity and noise margin for 74HCT and LSTTL device interfacing

		74HCT	LSTTL			
V _{ILmax}	(V)	0.8	0.8			
V _{IHmin}	(V)	2	2			
V _{OLmax}	(V)	0.33 (note 1) 0.1 (note 2)	0.4			
VOHmin	(V)	3.84 (note 1) 4.4 (note 2)	2.7			
Noise margin	is (V):					
from 74HCT to LS		V _{NML} V _{NMH}	0.47 1.84			
from LS to 74HCT		V _{NML} V _{NMH}	0.4			
from LS to LS		V _{NML} V _{NMH}	0.4			
from 74H to 74HCT		V _{NML}	0.7			

Notes

- 1. 4 mA load (i.e. 10 LSTTL inputs).
- 2. $20 \mu A$ load (i.e. 20 74HCT inputs).

Whenever a 74HCT output drives either an LSTTL or a 74HCT input, the noise margin is better than when an LSTTL device drives an LSTTL or 74HCT input. This improvement is larger for V_{NMH} owing to the superior output sourcing current of the rail-to-rail HCMOS output swing compared with the limited totem-pole pull-up output voltage of LSTTL.

DYNAMIC NOISE IMMUNITY

As for static noise immunity, dynamic noise immunity can be divided into two parts:

- a dynamic noise margin LOW
- a dynamic noise margin HIGH.

For 74HC devices, both margins are similar; for 74HCT devices, the dynamic noise margin LOW is the smaller of the two. To plot it, a pulse of known magnitude, V_p , is applied to the input of a device and its width, t_W , is increased until the device just begins to switch. The input level on which V_p is based is equal to the switching voltage minus the worst-case static noise margin LOW. The pulse width is measured at half pulse height, $V_p/2$. The rise and fall times, t_r and t_f are 0.6 ns.

 V_{p} is then reduced in increments and t_{W} for each new value is ascertained.

The test is repeated for different supply voltages — for 74HC devices between 2 V and 6 V, and at 5 V for 74HCT devices. A range of output currents, I_{O} , are also used. Increasing the DC load reduces the dynamic noise immunity.

Figure 44 shows the amplitude of positive-going pulses that can be withstood in the LOW state for 74HC and 74HCT devices. The curves are worst-case ones with fully-loaded drivers, so a system using only 74HC or 74HCT devices will have $0.23\,\mathrm{V}$ more noise margin for all t_{W} .

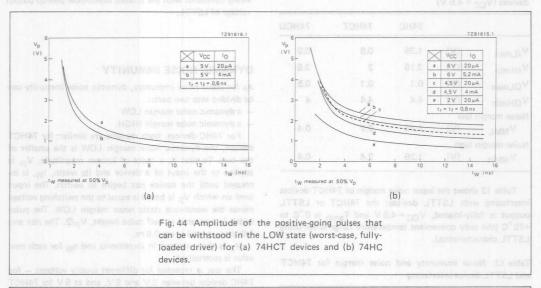
For typical input switching thresholds of 1.4 V and 2.25 V for 74HCT (V_{CC} = 5 V) and 74HC (V_{CC} = 4.5 V) respectively, the noise margins will be 0.83 V [(1.4 – 0.8) + 0.23 V] larger for 74HCT and 1.13 V [(2.25 – 1.35) + 0.23 V] larger for 74HC devices.

The main causes of unwanted input pulses are spikes due to outputs switching, which dumps large currents on the GND lines, or reflections when long lines (longer than about 32 cm) are driven. For more information on the latter, see chapter 'Replacing LSTTL and driving transmission lines'.

The best example of an unwanted pulse generator is an octal device with bus outputs of which seven are switching simultaneously and the eighth, most remote, output is LOW. Figure 45(a) shows the maximum pulse voltage measured on the unswitched output of a 74HC/HCT374 as a function of V_{CC} . Figures 45(b) and 45(c) show this maximum voltage.

age and the pulse width as functions of the number of outputs that are switching. It should be emphasised that any pulses produced by switching outputs won't cause other devices to respond even in worst-case conditions. This is because Fig.44 is based on a worst-case VOL and the

maximum expected pulse height of Fig.45 occurs for a best-case V_{OL}. So, even when a pulse of the maximum expected height shown in Fig.45 occurs, there is still a noise margin. This can be verified by plotting the pulse heights of Fig.45 on the curves of Figs 44(a) and 44(b).



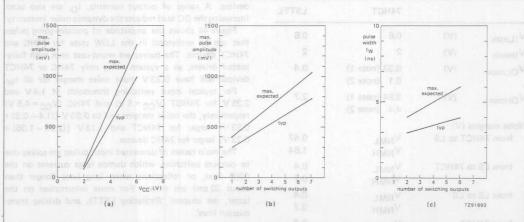


Fig. 45 (a) Amplitude of the voltage pulse (on pin 2, the most remote) due to switching seven of the bus-driver outputs of a 74HC/HCT374 octal flip-flop; $C_L = 150\,\mathrm{pF}$, $T_{amb} = 25\,^{\circ}\mathrm{C}$. (b) Amplitude of the voltage pulse (on pin 2) as a function of the number of outputs switched; $V_{CC} = 5\,\mathrm{V}$, $C_L = 150\,\mathrm{pF}$. (c) Pulse width as a function of the number of outputs switched; $V_{CC} = 4.5\,\mathrm{to}\,6\,\mathrm{V}$, $C_L = 150\,\mathrm{pF}$. For $V_{CC} = 2\,\mathrm{V}$, the maximum expected pulse width is about 10 ns.

BUFFERED DEVICES along quadratal bibs seed on all

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Often the terms 'buffer devices', 'buffered inputs' or 'buffered outputs' are used without qualification and originate from the very first unbuffered CMOS logic family consisting of one-stage logic elements, usually gates. In these devices, both input switching levels and output impedances were not constant, so neither were output rise/fall times or propagation delay times. The Jedec JC40.2 committee define a buffered device to be at least two active stages with the output incependent of the input logic voltage level and independent of the number of inputs that are HIGH or LOW.

A buffer meeting this definition is the AND-function circuit of Fig. 46. The gain between input and output is high enough to consider the output impedance to be independent of the logic level at the input, and the output impedance is not affected by the state of the logic inputs.

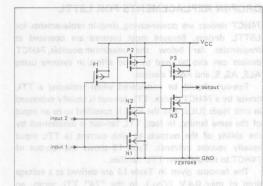


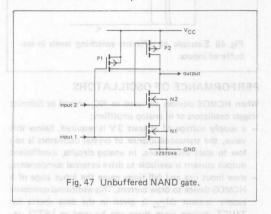
Fig. 46 The minimum number of stages for a buffered device is two. This 2-stage example is an AND function.

All 74HC and 74HCT devices comprise at least two stages to minimize any pattern sensitivity of propagation delay time. Buffering also improves static noise immunity due to increased voltage gain, giving almost ideal transfer characteristics.

The designation 74HCU is used to denote single-stage devices. These have the same specification as 74HC devices but their input and output voltage parameters are relaxed. 74HCU devices don't have the high gain of 74HC/HCT versions, which makes them more suitable for use in RC or crystal oscillators and other feedback circuits operating in the linear mode.

Output buffering

All 74HC and 74HCT devices have buffered outputs for optimum performance. To demonstrate the benefits of output buffering, consider what would happen without it. In the single-stage device shown in Fig.47, the output impedance depends on the DC input voltage. Consequently, the noise margins at the output become a function of the input voltage, even when V_I is a legal HIGH or LOW level.



The steady-state impedance of the circuit of Fig.47 is also affected by the state of the inputs. Given that P1 and P2 have identical performances (same size), there are two values of impedance for output HIGH; one when either input is LOW and P1 or P2 conducts, and another when both inputs are LOW and both P1 and P2 conduct. Therefore, without output buffering, the state of output conduction depends on the number of inputs that are HIGH or LOW.

Input buffering

An input is considered to be buffered when its switching threshold is unaffected by the logic states of other inputs. In the example of Fig.47 that has unbuffered inputs, the switching threshold of input 1 varies with a HIGH level at input 2, and vice versa. This is because the series impedance of transistors N1 and N2 determines the switching threshold of the device. The result can be seen in Fig.48 where curve $1\!+\!2$ occurs when the two inputs are tied together, and curve 1 or 2 is the switching threshold when the accompanying input is at $V_{\rm CC}$.

For true input buffering, an input must have an inverter stage with sufficient gain to ensure that logic levels give independent on-chip levels. Some gates in the 74HC series (usually AND or OR gates) have unbuffered inputs, however all devices meet the family logic level requirements. All 74HCT devices have buffered inputs.

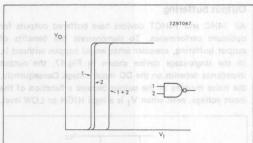


Fig. 48 Example of different switching levels in unbuffered inputs,

PERFORMANCE OF OSCILLATORS

When HCMOS devices are used in RC, crystal or Schmitt trigger oscillators or in analog amplifiers:

- a supply voltage of at least 3 V is required. Below this value, the transconductance of crystal oscillators is too low to start oscillations. In analog circuits, insufficient output current is available to drive external components;
- slow input rise and fall times cause the input stage of a HCMOS device to draw current. This additional quiescent supply current ΔI_{CC} is given in the data sheets for 74HCT devices since these can be used as LSTTL replacements and may be driving a significant load. The total I_{CC} for 74HC devices can be calculated by multiplying the value of I_{CC} read from Fig.14 by the unit load coefficient given in the data sheet for the 74HCT device;
- in general, frequency stability won't be affected by supply voltage, so long as the permissible output currents of the devices are not exceeded.

For further information, see chapters 'Crystal oscillators' and 'Astable multivibrators'.

LATCH-UP FREE metted ad or comedence at Jugat nA

Latch-up is the creation of a low-impedance path between the power supply rails caused by the triggering of parasitic bipolar structures (SCRs) by input, output or supply overvoltages. These overvoltages induce currents that can exceed maximum device ratings. When the low-impedance path remains after removal of the triggering voltage, the device is said to have latch-up.

The JEDEC standard test being developed for latch-up specifies that the input/output current should be equal to the maximum rating (± 20 mA), and that V_{CC} should also be not more than twice V_{CCmax} (14 V) for testing latch-up immunity with excess supply voltage. HCMOS ICs have been extensively subjected to the previously described tests with test parameters far exceeding those quoted by JEDEC.

In no case did latch-up occur. For example, it has been determined that an HCMOS input can typically withstand continuous current (5 s on, 15 s off) of 100 mA to 120 mA, or 1 us pulses of 300 mA with a duty factor of 0.001. An input can also withstand a discharge from a 200 pF capacitor charged to 330 V. An HCMOS output can withstand continuous current (5 s on, 15 s off) of 200 mA to 300 mA, or 1 us pulses of 400 mA with a duty factor of 0.001. However, because there is an internal polysilicon $100\,\Omega$ resistor in series with all HCMOS inputs, the input voltages required to achieve these current levels are so high $(V_1 = V_{CC} + 0.7 V + 100I_1)$ that it is unlikely that they could occur in practice, even in a 6 V system with severe glitches. Moreover, beyond these current levels, excessive heating occurs or aluminium tracks or bond wires breakdown. It is therefore reasonable to conclude that HCMOS logic ICs are completely latch-up free.

For further information, see chapter 'Standardizing latchup immunity tests' in the Designers Guide, High-speed CMOS.

DROP-IN REPLACEMENTS FOR LSTTL

74HCT devices are power-saving, drop-in replacements for LSTTL devices. Because most systems are operated at frequencies far below the maximum possible, 74HCT devices can also be used to good effect in systems using ALS, AS, S, and FAST devices.

Fan-out should be considered when replacing a TTL device by a 74HCT device. TTL fan-out is usually expressed in unit loads (ULs) and the load is specified to be an input of the same family. In fact, TTL fan-out is determined by the ability of the outputs to sink current (a TTL input usually sources current). Table 13 shows the fan-out of 74HCT to the different TTL families.

The fan-outs given in Table 13 are derived at a voltage drop of max. $0.4\,\mathrm{V}$ (V_{OL}). In the "74" TTL series, an extended V_{OL} figure is often seen, e.g. 8 mA at $0.5\,\mathrm{V}$ voltage drop for LSTTL. If this figure is used to determine the fan-out of the TTL device it can result in a higher fanout than is possible with 74HCT. This can be resolved by replacing as many of the driven TTL parts as possible by 74HCT devices to reduce the sink current requirement (the 74HCT input current is negligible). In addition, power dissipation is reduced significantly by using 74HCT.

Table 13: Fan-out of 74HCT to TTL circuits

NUMBER OF STREET	41.34.11.11.11.5.E.	11			SUPPLY SUPPLY
74HCT					
standard output	2	10	20	6	2 2 0 11 1
bus-driver output	3	15	30	10 sbort	3

BUS SYSTEMS

CMOS is being used to an increasing extent in microprocessor bus systems following the introduction of versions of the popular NMOS processors.

There are several constraints imposed on microprocessor systems in industrial applications, such as electrically-noisy environments, battery-standby requirements and sealed, gas-tight enclosures. HCMOS bus systems, e.g. the CMOS STD bus (a non-proprietary CMOS bus standard) provides a solution to all these problems. It offers superior noise immunity, equal operating speed, lower power dissipation, wider supply voltage range, extended temperature range, and enhanced reliability.

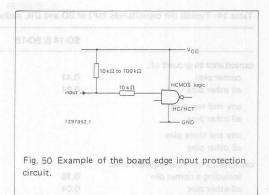
For optimum results, use only 74HC devices in circuits which communicate directly with the bus. This allows a new bus termination to be introduced (see Fig.49(b)) which, unlike the conventional TTL bus termination, draws no heavy DC current and is more suited to HCMOS outputs.

VCC
$$\frac{V_{CC}}{180\Omega}$$
 $\frac{1}{2k\Omega}$ $\frac{1}{390\Omega}$ signal line $\frac{1}{7297051.11}$ $\frac{1}{30\Omega}$ $\frac{1}{30\Omega}$

Fig. 49 Bus terminations. (a) Conventional termination for TTL buses. (b) Proposed termination for CMOS STD bus equivalents.

The wider supply voltage range of HCMOS together with its lower power dissipation virtually eliminates problems caused by voltage drops along power buses between cards in a system. It is possible for a circuit to pick up severe noise spikes or differential voltages via an edge connector. Such pick-up can exceed the CMOS maximum ratings if not limited by a $10\,\mathrm{k}\Omega$ series resistor in the HCMOS logic line. This will limit current to $\pm20\,\mathrm{m}A$ for external voltages of up to $\pm200\,\mathrm{V}$, however, for correct functioning, the DC input current should be kept below those values stated in 'Input/output protection'. The recommended board edge input protection is shown in Fig.50.

In the circuit of Fig.50, if the input diode current exceeds the maximum input current, a HIGH-to-LOW level shifter should be used (e.g. 74HC4049 or 74HC4050).



For further information, see chapter 'Interfacing and protection of circuit board inputs'.

Since HCMOS bus-drivers do not have built-in hysteresis, slowly-rising pulses should be avoided or devices with Schmitt-trigger action should be used, such as the flip-flop series 74HC/HCT73, 74, 107, 109, 112, or the dedicated Schmitt triggers 74HC/HCT14 and 132. The rise and fall times can be derived from the information given in the section 'Propagation delays and transition times' of this User Guide.

PACKAGE PIN CAPACITANCE

In purely digital circuits, the input capacitance or threestate output capacitance is sufficient to determine the dynamic characteristics. However, when a HCMOS device is used in the linear region, it is necessary to take pin capacitance into account, e.g. to prevent crosstalk in analog switches or peaks in the frequency response of PLLs.

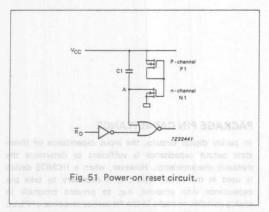
The use of SO packages with their low pin capacitances is recommended for HCMOS analog designs. Table 14 gives the pin-to-pin capacitances for the plastic DIL and SO packages used for HCMOS. Measurements were made using a dummy package with all unused pins connected to ground.

Table 14: Typical pin capacitances (pF) of SO and DIL packages

	SO-14 & SO-16	DIL-16	SO-20	DIL-20	SO-24	DIL-24
capacitance to ground of:		303300030		NMOS proces		
corner pins	0.41	0.07				
all other pins	0.21					
any end two pins				1.12 OMO		
all other pins				0.40		
any end three pins					0.65	1.64
all other pins					0.33	0.65
capacitance between adjacent pin	s: to element 02 pFl					
including a corner pin	0.15	0.40				
all other pins	0.04					
any end three pins			0.28	0.49		
all other pins				0.22		
any end three pins					0.30	0.70
all other pins					0.12	0.28

POWER-ON RESET

The power-on reset (POR) circuit used to automatically set HCMOS ICs in a defined reset state after power-up is shown in Fig.51.



When the IC is powered-up, node A follows the rise of V_{CC} through C1 and the circuit is reset. When the gate voltage of transistor N1 exceeds its threshold level (typically 0.7 V) because it is biased with V_{CC} via transistor P1, capacitor C1 discharges and pulls node A below the

switching level of the NOR gate. The IC cannot be used during the POR release time which is the discharge time of C1 (typically 3 μs at V $_{CC}$ = 4.5 V and 35 μs at V $_{CC}$ = 2 V). The sensitivity of the POR circuit to supply voltage reduction is indicated in Table 15. The typical values of parameters t_W and V $_L$ used in Table 15 are illustrated in Fig.52.

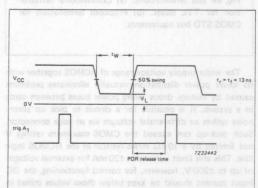


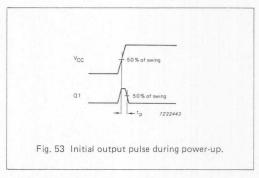
Fig. 52 $\,\rm V_L$ as a function of the duration of a LOW pulse on the supply voltage.

Table 15: Sensitivity of HCMOS POR circuitry to $\ensuremath{\text{V}_{CC}}$ reduction

		V _{CC} (V)	17 - 400
t _w (μs)	2	4.5	6
	V _{Lmax} (V)	V _{Lmax} (V)	V _{Lmax} (V)
8	0.8	2.2	2.8
6	0.75	2.2	2.8
4	0.7	2.2	2.8
2	0.6	2.1	2.8
1	0.5	2.0	2.8
0.5	0.4	1.9	2.8
0.1	0.4	1.9	2.8
0.05	0.4	_	1-
0.02	0.3	- 1	-
0.015	0.15	1.7	2.5

The time taken for a transition to propagate from \overline{R} to Q is about the time taken for the reset action to take effect. Also of course, node A in Fig.51 must rise to a level above the switching level of the NOR gate. Because of this, the

Q output of the IC may initially follow the V $_{\rm CC}$ ramp as indicated in Fig.53. If the V $_{\rm CC}$ ramp is fast (typically less than 100 ns), the amplitude of the Q output pulse can exceed V $_{\rm CC}/2$ and have a duration of about 10 ns.



Normally, the Q output pulse is negligible because the V_{CC} ramp is slow (typically more than 0.5 μ s) due to the charging time of large-value smoothing and decoupling capacitors. With a slow V_{CC} ramp, the amplitude of the Q output pulse remains well below the switching level of the succeeding stage. In any event, it is most unlikely that a system will be triggered by the Q output pulse because it only occurs during power-up.

Table 15: Sensitivity of HCMOS POR circultry to VCR mulucition

The time takes for a transition to propagate from \overline{R} to Q is about the time takes for the reset action to take effect. Also of counts, node A in Fig.51 must rise to a level above the switching level of the NOA cetts. Second of this, the

Douglout of the IC may initially follow the Voc ramp as neighboring in Fig.53. If the Voc ramp is fast (typically ess than 100 ns) the amplitude of the C output pulse an exceed Vocs/2 and have a duration of about 10 ns.



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QUALITY INFORMATION

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QUALITY INFORMATION

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QUALITY ASSURANCE

Our Quality Department is fully involved in all stages of the production cycle of our HCMOS family of logic ICs:

- design and development
- wafer fabrication
- assembly
- inspection and testing
- batch release
- customer liaison.

The result is a continuous feedback of data which enables us to refine design procedure, production conditions and test methods. By adopting this procedure we ensure optimum quality in the final application.

Design and development

Layout rules and designs parameters for our HCMOS family of ICs are specified in our Design Manual, which reflects more than fifteen years' experience in CMOS silicon-gate production.

During the CAD generation of new circuit designs, layouts are automatically checked against the design rules laid down in the Design Manual. Each layout is further checked by the Quality Department against not only the Design Manual requirements, but also against the capabilities of the assembly process and product specifications (this forms part of the product release and qualification procedure). This design check activity supplements our product knowledge and customer support capability.

Wafer fabrication

To realize the full performance potential of our HCMOS technology we have developed an organizational structure for the wafer fabrication process. Production flow is now divided between technology-oriented Process Control Groups that are responsible for:

- process control
- equipment engineering
- calibration
- contamination control
- training.

Activities of these Groups are coordinated by Process Engineering and supported by extensive data-processing facilities. The flow of wafers through the various fabrication stages and the associated process controls are shown in Fig.1. The overall wafer fabrication activity, Fig.2, is monitored by frequent audits by the Quality Department. The audit procedures are defined in our Quality Manual.

Assembly

Quality control is fully integrated into the assembly process, as shown in Fig.3.

Dice are assembled into packages on highly automated assembly lines. Fully automatic die attach and wire bonding ensure a high and consistent assembly quality. Tube-to-tube handling after moulding (or sealing, for cavity devices) ensures excellent mechanical and visual quality.

There is a continuous exchange of information between our assembly centres. All aspects of quality and reliability for these assembly centres are controlled by the HCMOS Quality and Reliability department. These centres are audited twice a year.

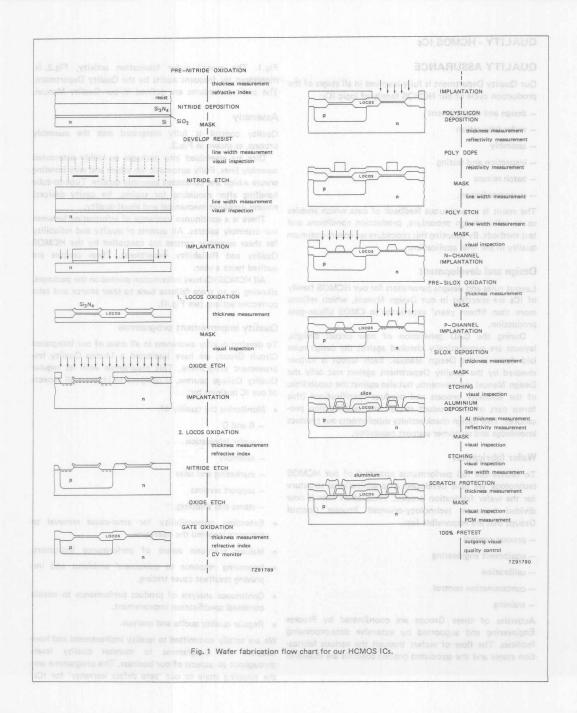
All HCMOS ICs have information printed on the packages, allowing us to trace failures back to their source and take corrective actions (see Fig.4).

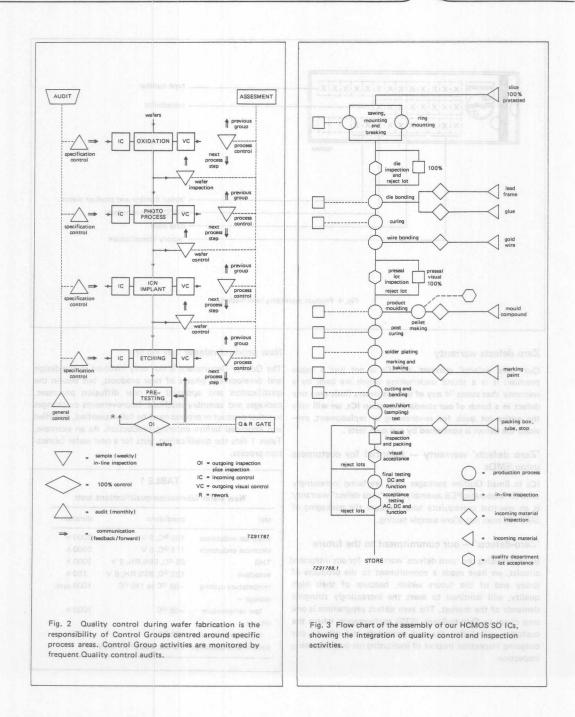
Quality improvement programme

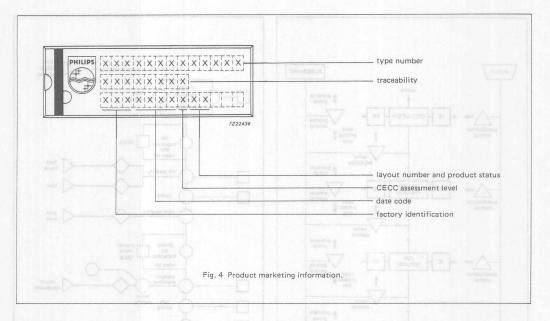
To develop quality awareness in all areas of our Integrated Circuit Group, we have instituted a 14-step Quality Improvement programme. This programme with its regular Quality College courses, is designed to improve all aspects of our IC business by:

- · Monitoring the quality of:
 - R and D
 - wafer fabrication
 - assembly
 - marketing and sales
 - support services
 - stores and shipping.
- Extending responsibility for error-cause removal to everyone involved the operation.
- Making everyone aware of performance indicators.
- Improving response to customers' problems and improving resultant cause tracing.
- Continuous analysis of product performance to enable continual specification improvement,
- · Regular quality audits and analysis.

We are totally committed to quality improvement and have adopted this programme to monitor quality levels throughout all aspects of our business. This programme was the stepping stone to our 'zero defect warranty' for ICs.







Zero defects warranty

Our 'zero defects' standard for ICs is not just a vague promise; it is a sound undertaking which we back by a warranty that states 'If any of our customers finds even one defect in a batch of our standard-function ICs, we will take the entire lot back for re-screening or replacement, provided the defect is confirmed by our own tests'.

'Zero defects' warranty — essential for customers using SMDs

ICs in Small Outline packages (SO) are being increasingly used for automatic PCB assembly. The 'zero defect' warranty is an essential prerequisite here, because the packaging of SMD ICs does not allow sample testing.

'Zero-defects' - our commitment to the future

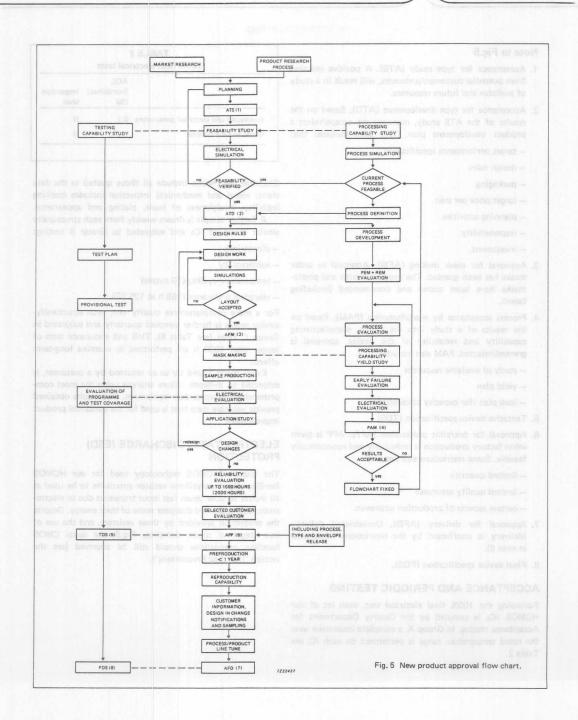
By introducing the 'zero defects' warranty for our integrated circuits, we have made a commitment to the products of today and of the future which, because of their high quality, will continue to meet the increasingly stringent demands of the market. The zero defect programme is one step closer to Ship-to-Stock (STS) performance, where the customer will define the test procedure and rely on our outgoing inspection instead of instituting his own incoming inspection.

New product release (see Fig.5)

The Quality Department is not only involved in the design and development phases of new products, but also in the qualification and approval of new diffusion processes, packages and assembly methods. Improvements or changes in either product or process must be fully specified, qualified and approved before entering production. As an example, Table 1 lists the qualification tests for a new wafer fabrication process.

TABLE 1
New wafer fabrication qualifications tests

test	conditions	duration
electrical endurance	150 °C, 6 V	2000 h
electrical endurance	175 °C, 6 V	2000 h
ТНВ	85 °C, 85% RH, 6 V	2000 h
autoclave	132 °C, 85% RH, 6 V	150 h
temperature cycling	-65 °C to 150 °C	1000 cycl.
storage —		
low temperature	-65 °C	1000 h
storage —		
high temperature	150 °C	
electrostatic discharge	1,5 kΩ, 100 pF,>2 kV	riens in topic



Note to Fig.5

- Acceptance for type study (ATS). A positive reaction from potential customer/customers, will result in a study of available and future resources.
- Acceptance for type development (ATD). Based on the results of the ATS study, management accept/reject a product development plan. This plan includes the:
 - target performance specification
 - design rules
 - packaging
 - target price per unit
 - planning activities
 - responsibility
 - investment.
- Approval for mask making (AFM). Approval to order masks has been granted. The product design and photomasks have been coded and documented (including tapes).
- 4. Process acceptance by manufacturing (PAM). Based on the results of a study into the design, manufacturing capability and reliability of the device, approval is granted/rejected. PAM also includes:
 - study of available resources
 - yield plan
 - load plan (for capacity calculations).
- 5. Tentative device specification (TDS).
- Approval for pre/pilot production (APP). APP is given when factory production is technically and economically feasible. Some restrictions still remain:
 - limited quantity
 - limited quality assurance
 - certain aspects of production unproven.
- Approval for delivery (AFD). Unrestricted delivery (delivery is unaffected by the restrictions mentioned in note 6).
- 8. Final device specification (FDS).

ACCEPTANCE AND PERIODIC TESTING

Following the 100% final electrical test, each lot of our HCMOS ICs is sampled by the Quality Department for Acceptance testing. In Group A, a complete inspection over the rated temperature range is performed on each IC, see Table 2.

TABLE 2		
promotes and a second	AQL (combined) (%)	inspection level
functional and electrical parameters	0.1	П
visual and mechanical	0.1	П

Electrical parameters include all those quoted in the data sheet; visual and mechanical inspection includes marking legibility, straightness of leads, plating and appearance.

A further sample is drawn weekly from each structurally similar group of ICs and subjected to Group B testing:

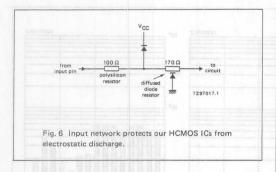
- dimensions
- solderability
- temperature cycling (10 cycles)
- electrical endurance (168 h at 125 °C).

For a more comprehensive quality test, each structurallysimilar group is further sampled quarterly and subjected to Group C Tests (see Table 8). THB and endurance tests of longer than 1000 h are performed to examine long-term effects.

Every reject found by us or returned by a customer, is subjected to in-depth failure analysis using the most comprehensive and up-to-date equipment. The results obtained provide valuable data that is used for the continual product improvement.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

The improved CMOS technology used for our HCMOS families allows polysilicon resistor structures to be used at all inputs to slow down fast input transients due to electrostatic discharges and dissipate some of their energy. Despite the protection provided by these resistors, and the use of two stages of diode clamping, Fig.6, the usual CMOS handling precautions should still be observed (see the section 'Handling Precautions').



ESD resistance of our HCMOS ICs is measured for both positive and negative discharges from a 100 pF capacitor through a 1.5 k resistor. Pulse rise time is 13 ± 2 ns. All input pins can withstand a discharge of 2.5 kV (typ.). The output pins can withstand > 3.5 kV (typ.) due to the large diodes formed by the drain surface of the output transistors.

OUTGOING QUALITY

The results from Quality Department Acceptance testing provide a good indication of the outgoing quality of our HCMOS ICs. Figure 7 shows the reject levels recorded in ppm (parts per million) for the years 1984 to 1986 and the first nine months of 1987.

ENDURANCE AND ENVIRONMENTAL TEST RESULTS

Temperature-humidity-bias

THB testing indicates the moisture resistance of plastic DIL and SO packages. It is performed at 85 °C and 85% relative humidity with $V_{CC}=6~V$. Electrical measurements (against the Device Specification) are made after 168 h, 500 h, 1000 h, and every 1000 h thereafter. Functional failures are subjected to failure analysis.

Results from tests carried out up to September 1987 (Table 3) show the excellent moisture resistance of our packages, even after extended tests durations.

Results of THB testing confirm that there is no significant difference between the results of tests on ICs in DIL and SO packages.

TABLE 3 Temperature-humidity-bias (85 °C/85% RH/6 V)

test	100	failure	(cum.)	cumulative failure (%		
time (h)	sample (N)	parameter	function	parameter	function	
170	2112	0	1	0.0	0.05	
500	2092	0	1	0.00	0.05	
1000	1875	1	1	0.05	0.05	
2000	1275	1	2	0.08	0.16	
4000	575	0	2	0.00	0.35	
6000	159	0	1	0.00	0.63	
8000	60	0	1	0.00	1.67	

Failure analysis of rejects:

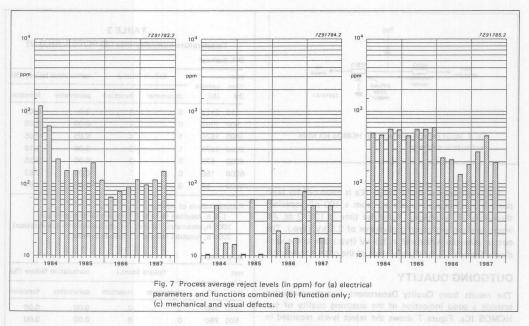
170 h, function failure: 1 x open aluminium track
1000 h, parametric failure: 1 x gate breakdown (oxidization)
2000 h, function failure: 1 x open contact.

SO package

test		failure	(cum.)	cumulative failure (9		
(h)	sample (N)	parameter	function	parameter	function	
170	790	0 000 (0)	0	0.00	0.00	
500	750	0	0	0.00	0.00	
1000	670	0	0	0.00	0.00	
2000	650	0	1	0.00	0.15	
4000	370	1	0	0.27	0.00	
8000	20	0	0	0.00	0.00	

Failure analysis of rejects:

2000 h, function failure: 1 x open contact 4000 h, function failure: 1 x I_{CC} leakage.



Autoclave with bias

This is essentially a THB test with an accelerated factor of 30, this means that 120 hours' autoclave is comparable with 3600 hours' THB. We have extended the conventional autoclave test to include 6 V bias at a temperature of 133 °C in unsaturated steam at a relative humidity of 85% and a pressure of 250 kPa (2.5 atmospheres). The results given in Table 4 attest to the excellence of the siliconnitride/Vapox protection layer and the excellent workmanship of the package.

Accelerated life testing

To obtain data for failure rate predictions quickly, some life tests are performed at elevated temperatures. ICs are powered by their maximum supply voltage; ambient temperature is up to 125/150 °C for ICs in plastic packages and 175/225 °C for ICs in special/ceramic evaluation packages. Function and electrical parameters are tested before the life tests starts, and then after 48 h, 168 h, 1000 h, and every 1000 h thereafter. Every failure found is analysed. A large number of 74HC and 74HCT types were tested and the results are shown in Tables 5 and 6.

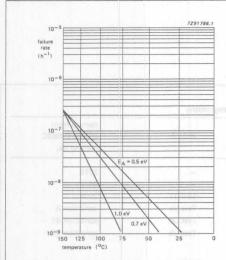
Tables 5 and 6 show the excellent quality level obtained by us over the last few years. Table 6 is a derated (derated to 50 °C version of Table 5.

The effect on failure rates by the use of different activation energies is shown in Fig.8.

						BLE 4						
				Temperatur	e-humidity	-bias: 13	3 °C/85	% RH	/6 V			
DIL	ackage					SO pa	ackages	protes/pe	Ptuliel			
test	sample	failure	(cum.)	cumulative	failure (%)	test time	sample	007	failure	(cum.)	cumulativ	e failure (%
(h)	(N)	parameter	function	parameter	function	(h)	(N)		imeter	function	parameter	function
60	1477	0	1	0.00	0.07	60	1112	0		4	0.00	0.36
120	1147	0	2	0.00	0.17	120	1112	3		4	0.27	0.36
180	922	1 331 x	3	0.11	0.33	180	877	2		4	0.23	0.45
240	822	1	3	0.12	0.36	240	827	2		3	0.24	0.36
300	792	1	4	0.13	0.51	300	792	2		2	0.25	0.25
360	762	1	5	0.13	0.66	360	550	0		0	0.00	0.00
420	702	0	9	0.00	1.28	420	530	0		0	0.00	0.00
480	682	0	4	0.00	0.59	480	500	0		1	0.00	0.20
540	578	O HOUSE	3	0.00	0.52	540	450	7		4	1.56	0.89
600	518	0	1	0.00	0.19	600	450	8		5	1.78	1.11
660	458	0	1	0.00	0.22	720	270	0		1 5017	0.00	0.37
720	458	0	1	0.00	0.22	840	80	0		1	0.00	1.25
840	189	0	2	0.00	1.06	960	30	0		1	0.00	3.33
960	140	0	0	0.00	0.00						0.00	0.00
080	120	0	0	0.00	0.00	Failur	e analysi	s of rei	ects:			
200	120	0	0	0.00		60				2 x bond	pad corrosion	
320	120	0	03 = 000	0.00	0.00					1 x broke	en lead	
440	60	0	0	0.00	0.00	enter oru				1 x ICC		
440	30	0	0	0.00		120	h, param	eter fa	ilure:	1 x 3-stat	e leakage	
EGO										1	alversiations as	a a la
560	50.01			0.00	0.00						aluminium tr	rack
1560 Failur	50 60 10	-	a ligi		0.00	480	h, functi	on fail	ure:	1 x crack	ed die	
ailur	e analysis	of rejects:	00 to	failures	0.00		h, functi			1 x crack 1 x l _{CC} l	ed die eakage	
ailur 60	e analysis h, functio	of rejects:	1 x intern		10		h, param		ilure:	1 x crack 1 x l _{CC} l ₁ 7 x l _{CC} l ₂ 2 x bond	ed die eakage eakage pad corrosior	
ailur 60 120	e analysis h, functio h, functio	of rejects:	1 x intern	al corrosion	8		h, param	eter fa	ilure:	1 x crack 1 x I _{CC} II 7 x I _{CC} II 2 x bond 1 x dama	ed die eakage eakage pad corrosion ged during	
ailur 60 120	e analysis h, functio h, functio	of rejects:	1 x intern 1 x source 1 x param good a	al corrosion dedrain leakage etric failure (e	lectrically	540	h, param functi	eter fa on fail	ilure: ure:	1 x crack 1 x I _{CC} II 7 x I _{CC} II 2 x bond 1 x dama decap	ed die eakage eakage pad corrosion ged during osulation	
Failur 60 120 180	e analysis h, functio h, functio h, parame	of rejects: 25 on failure: 144 on failure: etric failure:	1 x intern 1 x source 1 x param good a 1 x intern	al corrosion dedrain leakage etric failure (e lifter decapsula al corrosion	lectrically	540	h, param functi h, functi	eter fa on failt	ilure: ure: ure:	1 x crack 1 x l _{CC} l ₁ 7 x l _{CC} l ₂ 2 x bond 1 x dama decap 1 x l _{CC} l ₁	ed die eakage eakage pad corrosion ged during isulation eakage	
60 120 180	e analysis h, functio h, functio h, parame	of rejects: for failure: failure: etric failure:	1 x intern 1 x source 1 x param good a 1 x intern 1 x intern	al corrosion drain leakage etric failure (e lifter decapsula al corrosion	lectrically	540	h, param functi h, functi	eter fa on failt	ilure: ure: ure:	1 x crack 1 x I _{CC} II 7 x I _{CC} II 2 x bond 1 x dama decap	ed die eakage eakage pad corrosion ged during isulation eakage	
=ailur 60 120 180 300 360	e analysis h, function h, function h, parame	of rejects: on failure: on failure: etric failure: on failure: on failure:	1 x intern 1 x source 1 x param good a 1 x intern 1 x intern 1 x I _{CC} le	al corrosion c-drain leakage etric failure (e ifter decapsula al corrosion al corrosion akage	lectrically	540	h, param functi h, functi	eter fa on failt	ilure: ure: ure:	1 x crack 1 x l _{CC} l ₁ 7 x l _{CC} l ₂ 2 x bond 1 x dama decap 1 x l _{CC} l ₁	ed die eakage eakage pad corrosion ged during isulation eakage	
=ailur 60 120 180 300 360	e analysis h, function h, function h, parame	of rejects: for failure: failure: etric failure:	1 x intern 1 x source 1 x param good a 1 x intern 1 x intern	al corrosion I-drain leakage etric failure (e ifter decapsula al corrosion al corrosion akage akage	lectrically	600	h, param functi h, functi	eter fa on failt	ilure: ure: ure:	1 x crack 1 x l _{CC} l ₁ 7 x l _{CC} l ₂ 2 x bond 1 x dama decap 1 x l _{CC} l ₁	ed die eakage eakage pad corrosion ged during isulation eakage	
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300 360 420 480	e analysis h, function h, function h, parame h, function h, function h, function h, function h, function	of rejects: on failure: on failure: etric failure: on failure: on failure: on failure: on failure:	1 x intern 1 x source 1 x param good a 1 x intern 1 x lcc le 1 x lcc le 1 x lcc le 1 x lcc le 1 x lcc le	al corrosion -drain leakage etric failure (e ifter decapsula al corrosion al corrosion akage akage akage akage akage	lectrically	540 5 600 5 1385 5 800 5 800	h, param functi h, functi param	eter fa on failt	ilure: ure: ure: ilure:	1 x crack 1 x l cc li 2 x bond 1 x dama decap 1 x l cc li 1 x l cc li 1 x l cc li	ed die eakage eakage pad corrosion ged during ssulation eakage eakage	entreament of the control of the con
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			V 8/F	in magy Li	TABI fe results	LE 5 tests; 6 V	0141836	oms	7			
			failures	/samples tes	t duration							
package types and temperature		170	500	1000	2000	4000	8000		12000	failures		
Plastic DIL 125	0.00	0/220 0/2333	0/104 0/2333	0/27	- 1/1393	_ 1/873	- 1/497	00.0	- 0/80	parametric, 1 x I _{CC} leakage	1477 1147 922	120
Ceramic DIL 175 225	0.25 0.25 0.00	0/386 0/48	1/386 0/48	1/386	2/386 0/24	2/220	1/140	0.12 0.13 0.13 0.13		parametric threshold P-char 2000 h, 1 x I _{CC}		246 360 360
Plastic SO 125 150	00.0 1.56 1.28 1.28		0/77 3/1062	0/77 3/982	3/942	3/606	- 2/296	00.00 00.00 00.00		function 1 x gate oxide b 1 x overstress	reakdow	980 0 0 0 800
85.1	00.0			0 08	848	55,8		00.0		f p	488	120

			device hours	00.0		failure rate	failure rate at 50 °C with
temperature (°C)	Selot 00 X		at 50 °C (10 ⁶)	failu			60% UCL (10 ⁻⁹ /hr)
Plastic DIL	x demaged during december	r and the second	У.	flesimostal en	ulist ohtsemi	exi ts	190 h, parametric failur
125	220	0.09	9.7	0		< 102.63	94.04
150	2333	7.70	2941.4				
			2951.1	1			0.96
Ceramic DIL					pen gate		480 h, function failure:
175	386	1.77	1976.6	4			2.65
225	48	0.06	445.7	0		2.24	2.06
			2951.1	4		1.65	2.16
Plastic SO				I FILL			
125	157	0.09	10.4	0		< 96.53	88.45
150	1102	4.37	1668.1	4		2.40	3.14
			1678.5	4		2.38	3.13
total		I TANK A TOO	7051.9	9		1.28	1.49



MAY

Fig. 8 Projected failure rates for our HCMOS ICs as a function of temperature, with activation energy as parameter.

Temperature cycling

Cycling between —65 °C and +150 °C generates stresses that test the structural integrity of die and packages. We perform this test according to the requirements of the MIL-STD-883C, Method 1010, Condition C. Samples are checked before and after the test for function and electrical parameters against the published values. Two failures have been observed in 1200 cycles, as reported in Table 7.

TABLE 7
Temperature cycling: -65 °C to +150 °C in dry air

	DIL		SO		
no. of cycles (cum.)	samples	failures (cum.)	samples	failures	
200	1686	0	1183	0	
400	1492	0	1118	0	
800	997	0	1038	1 Tunsin	
1200	360	0	616	2	
1600	195	0	310	0	
2000	195	0	288	0	
2400	195	0			

RELIABILITY TEST PROGRAM

Conditions for the endurance tests performed regularly on structural similarity groups of our HCMOS ICs are derived from IEC68 and MIL-STD-883C specifications. These are listed in Table 8.

	TABLE 8 Periodic reliability test pro	ogramme	
subgroup	description	IEC 68	derived from MIL-STD-883C method no.
C1	dimensions	- 107000	2016
C2	marking	==+4	2015
C3	robustness of terminations	68-2-21	2004
	- tensile	Test Ua	condition A
	- bending	Test Ub	condition B1
	— lead fatigue	Test Ub	condition B2
C4	temperature treatment (sequential) — resistance to soldering heat (10 s at 300 °C)		
	- thermal shock (10 x 0 °C to 100 °C)	68-2-27 Test Nc	1011 condition A
	 temperature cycling (10 x -65 °C to 150 °C) storage to 85 °C and 85% RH for 21 days 	68-2-87 Test Na	1011 condition A
C6	THB (85 °C/85% RH/6 V/1000h)	68-2-3 Test Ca	1004
C8	electrical endurance 1000 h at 125 °C		1005
C10	temperature cycling (200 x -65 °C to +150 °C)	68-2-14 Test B	1010 condition C
C11	storage endurance 1000 h at Tamb = 150 °C	68-2-2 Test Ba	1008 condition C
C12	storage endurance 1000 h at Tamb = -65 °C	68-2-1 Test Ab	
C13	transient energy		3015 Of Or Dom
C15	salt mist	68-2-11 Test Ka	1009 condition A
	solderability -do need	68-2-20 Test T	2001
	autoclave 121 °C/100% RH/60 h		

CECC QUALIFIED PRODUCTS

Introduction

The CECC Quality System, which dates from 1973, facilitates international trade by the publication of harmonized specifications and quality assessment procedures for electronic components. CECC approval is issued by independent nationally recognized, National Supervisory Inspectorates (NSI). Our HCMOS quality control programme is based on the rules and procedures laid down by the CECC and our manufacturing activities have received official CECC approval.

Our HCMOS ICs are qualified to the generic specification CECC 90 000 (latest issue) and the family specification CECC 90 109.

CECC - what are customers offered?

- ICs wholly manufactured in CECC approved premises.
- ICs released by an Inspection Organisation which is approved by the National Supervising Inspectorate (NSI).
- ICs released in accordance with CECC adopted specifications.
- · Mandatory sample life tests and environmental tests.
- Delivery in packages which are sealed with the mark of conformity under supervision of the NSI.
- Certified test records compiled every six months and available on request.
- Audits of the production facilities by the NSI.

The CECC scheme

CECC is a scheme for providing electronic components of an assessed quality which is controlled by the NSI. It is set up by the CENELEC (European Committee for Electrotechnical Standardization), Electronic Components Committee (CECC) and the International Electrotechnical Commission (IEC).

The CECC scheme includes two essential features of any Quality Assurance Scheme:

- a specification system
- a certification procedure supported by an independent inspectorate.

CECC IN OPERATION

The CECC scheme operates essentially in three parts:

Part 1; the plant qualification.

Part 2; the device specification.

Part 3; quality conformance inspection of deliveries.

Part 1

Established to the satisfaction of the NSI that the organization has adequate quality systems, procedures and standards to control the manufacturing of electronic components to the minimum standard as defined in the CECC system.

Part 2

Established by demonstration to the NSI that the ICs can meet the requirements of detail specifications which are prepared in accordance with the CECC systems. This is accomplished by performing the qualification activity.

Part 3

Established by lot-by-lot and periodic sampling basis such that the ICs conform to the specification to which they were initially qualified. Data on the results of these tests are provided as Certified Test Records (CTRs), certified by a representative of the NSI and published at six-monthly intervals.

CECC - QUALIFICATION FEATURES

Lot-by-lot testing

Group A inspection

Group A prescribes the visual examination and electrical lot-by-lot measurements to assess the principal electrical properties of a circuit (see CECC 00 107). Group A inspection is divided into appropriate Sub-Groups.

Group B inspection

Group B prescribes the lot-by-lot procedures to be used to assess certain additional properties of the IC. It includes environmental and endurance tests which can be completed in less than a week (see CECC 00 107). Group B inspection is divided into appropriate Sub-Groups.

Periodic tests

Group C inspection

Group C prescribes the procedures to be used on a periodic basis to assess certain additional properties of the IC. It includes environmental and endurance tests which are appropriate for checking at intervals of 3 months. Group C inspection is divided into appropriate Sub-Groups.

Group D inspection

Group D prescribes the procedures to be used on a periodic basis at intervals of 12 months.

CECC - QUALIFICATION PROCEDURE

- · Raise detail specification with appropriate rules.
- Detail specification approved by NSI and NAI (National Authorized Institution).
- Submit 3 separate lots for qualification.
- · Pass all Group A and B tests on each of the 3 lots.
- Pass all Group C test on a combined sample from the 3 lots
- Pass all Group C tests, except Test C8 (endurance).
- Pass C8 endurance test at 2000 hours. Submit test records countersigned by supervising inspector and apply for provisional approval.

CECC - PRODUCTS

Our HCMOS ICs are available up to the highest assessment level P. Products qualified by the CECC are recognized by the symbol (CECC symbol) on the individual data sheets in this handbook and in the Qualificatied Parts List (Q.P.L.) CECC 00 200 (latest issue), which is available at the National Authorized Institutions. The appropriate details specification number is also given.

The CECC scheme

CECC is a scheme for providing electronic components of massessed quality which is controlled by the NSI. It is set up by the CENELEC (European Committee for Electronic Standardization), Electronic Components Committee (CECC) and the International Electrorecinical Committee (CECC).

The CECC scheree Includes two estential features of any Quality Assurance Scherner

- a specification system
- a certification procedure supported by an independent inspectorate.

SECCIM OPERATION

The CECC scheme operates essentially in three parts:

art 1: the plant qualification.

Part 2; the device specification.

Part 3: quality conformance insection of deliveries.

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Established to the satisfaction of the NSI that the organization has adequate quality systems, procedures and standards to control the manufacturing of electronic components to the minimum standard as defined in the CCCC system.

Part

Established by demonstration to the NSI that the ICs can meet the requirements of datal specifications which are prepared in accordance with the CECC systems. This is accomplished by performing the qualification activity.

E tred

Established by lot-by-for and periodic sampling basis such that the ICs conform to the specification to which they were initially qualified. Data on the results of these tests are provided as Certified Test Rodords (CTRs), certified by a representative of the NSI and published as six-monthly intervals.

CECC - QUALIFICATION FEATURES

Lot-by-lot testing

Group A inspection

Group A prescribes the visual examination and electrical lot-by-lot measurements to assess the principal electrical properties of a circuit (see CECC 00 107). Group A inspection is divided into supropriate Sub-Groups.

Group B inspection

From 8 prescripes the lockly-lot procedures to be used to sesses certain additional properties of the IC, it includes neveronmental and endurance tests which can be completed to less than a weak (see CECC 00 107). Group 8 respection is divided into appropriate Sub-Broups.

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Group C prescribes the procedures to be used on a pariodic basis to assess certain additional properties of the IC. It lookudes sovicenmental and andurance tests which are appropriate for the billion of intervals of 3 months, Group C inspection is alwided into appropriate Sub-Broups.

Group D Inspection

Group D prescribes the procedures to be used on a periodic basis at interession 12 months.

CREC ... CHALLETCA TION PROCEOURE

- Raise detail specification with appropriate rules
- Detail specification apployed by NSI and NAI
 (National Authorized Institution),
 - Submit 3 separate fors for qualification.
- a Para all Group A and B tests on each of the 3 lots
- Pass all Group C test on a combined sample from the 3 lers.
- . Park of Group C rests, except Test C8 (endurance).
- Pass C8 endurance test at 2000 hours. Submit test records countersigned by supervising inspector and apply for provisional exproval.

STALIGNER _ abac

Our HCMOS IDs are preliable up to the highest assessment level P. Products qualified by the OECC are incognized by the symbol (CECC symbol) on the individual data sheats in this symbol (CECC 00 200 (letest issue), which is available at the National Authorized Institutions. The appropriate details specification number is also given.

HCMOS FAMILY CHARACTERISTICS

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HOMOS FAMILY CHARACTERISTICS

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Data sheet specification guide

Definitions of symbols

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire HCMOS 74HC/HCT/HCU family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The 74HC/HCT/HCU high-speed Si-gate CMOS logic family combines the low power advantages of the HE4000B family with the high speed and drive capability of the low power Schottky TTL (LSTTL).

The family will have the same pin-out as the 74 series and provide the same circuit functions.

In these families are included several HE4000B family circuits which do not have TTL counterparts, and some special circuits.

The basic family of buffered devices, designated as XX74HCXXXXX, will operate at CMOS input logic levels for high noise immunity, negligible typical quiescent supply and input current. It is operated from a power supply of 2 to 6 V.

A subset of the family, designated as XX74HCTXXXXX, with the same features and functions as the "HC-types", will operate at standard TTL power supply voltage (5 V ± 10%) and logic input levels (0.8 to 2.0 V) for use as pin-to-pin compatible CMOS replacements to reduce power consumption without loss of speed. These types are also suitable for converted switching from TTL to CMOS.

Another subset, the XX74HCUXXXXX, consists of single-stage unbuffered CMOS compatible devices for application in RC or crystal controlled oscillators and other types of feedback circuits which operate in the linear mode.

HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.

However, to be totally safe, it is desirable to take handling precautions into account (see also chapter "HANDLING PRECAUTIONS").

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER		74HC			74HC1	ed House	UNIT	CONDITIONS
STWIBOL	FARAMETER 13° 0 (1- suppl	min.	typ.	max.	min.	typ.	max.	Jid one	Ig CONDITIONS
Vcc	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	K
VI	DC input voltage range	0		Vcc	0		Vcc	V	
V _O	DC output voltage range	0		Vcc	0		Vcc	V	
Tamb	operating ambient temperature range	-40	90000	+85	-40	inne 180	+85	°C	see DC and AC
T _{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	per device
t _r , t _f	input rise and fall times except for Schmitt-trigger inputs		6.0	1000 500 400		6.0	500	ns	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V

Note

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", the specified maximum operating supply voltage is 10 V.

RECOMMENDED OPERATING CONDITIONS FOR 74HCU

SYMBOL	DARAMETER		74HCL	J	LINUT	CONDITIONS
STINBUL	PARAMETER	min.	typ.	max.	UNIT	CONDITIONS
Vcc	DC supply voltage	2.0	5.0	6.0	V	
VI	DC input voltage range	0		Vcc	V	
V _O	DC output voltage range	0		Vcc	V	
T _{amb}	operating ambient temperature range	-40		+85	°C	see DC and AC
T _{amb}	operating ambient temperature range	-40		+125	°C	Per device

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V) as standard summer UDH TOHIOHAY 20M2H entire and to applications

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
Vcc	DC supply voltage	-0.5	+7	V	NEROBOUTION The TAHC/HCT/HCQ high-speed Si-gate CMOS logic fair
±IIK	DC input diode current	berattus	20	mA	for $V_1 < -0.5$ or $V_1 > V_{CC} +0.5$ V
±10K	DC output diode current	irlw arius	20	mA	for V_{O} < -0.5 or V_{O} > V_{CC} +0.5 V
Ol± Dostatic et fe	DC output source or sink current - standard outputs - bus driver outputs	NEPLINE uts and la variet, wever, to	25 35	mA mA	for -0.5 V < V _O < V _{CC} +0.5 V
±I _{CC} ; ±I _{GND}	DC V _{CC} or GND current for types with: — standard outputs — bus driver outputs	ECAUT	50 70	mA mA	CXTANCXXXXX, will uperate at CMDS input Topic limiting noise branchity, and input typical quiescent supply nout pour europhy of 2 and power supply of 2 and 2 an
T _{stg}	storage temperature range	-65	+150	°C	SECONMENDER ORGEN TIMO CONDITIONS CO
P _{tot}	power dissipation per package		750	mW	for temperature range: -40 to +125 °C 74HC/HCT/HCU above +70 °C: derate linearly with 12 mW/K
	plastic Brz	eri	500	mW	above +70 °C: derate linearly with 8 mW/K

Note

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", the specified maximum operating supply voltage is 11 V.

| TAND | PARAMETER | TAND | TA

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

					T _{amb} (°C)					TEST CO	NDITIONS
	PARAMETER V	125	+ or 01	- 88	74H	C			UNIT	N	TEMAS	OTHER
SYMBOL	PARAMETER	+25			-40	to +85	-40 t	o +125	UNII	V _{CC}	VI	OTHER
	4.5	min.	typ.	max.	min.	max.	min.	max.				
VIH	HIGH level input voltage	1.5 3.15 4.2	1.2 2.4 3.2	2	1.5 3.15 4.2		1.5 3.15 4.2	2.0	V	2.0 4.5 6.0	level Hi	TH (H)
VIL	LOW level input voltage	8.0	0.8 2.1 2.8	0.5 1.35 1.8	0	0.5 1.35 1.8	0 5,	0.5 1.35 1.8	V	2.0 4.5 6.0	ni lavel W	Da 71.
VOH	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0	Co-	1.9 4.4 5.9	A	1.9 4.4 5.9	4,4	V	2.0 4.5 6.0	VIH or VIL	$-1_0 = 20 \mu A$ $-1_0 = 20 \mu A$ $-1_0 = 20 \mu A$
Vон	HIGH level output voltage standard outputs	3.98 5.48	4.32 5.81	8	3.84 5.34		3.7 5.2	h 80.6	V	4.5 6.0	VIH or VIL	-1 _O = 4.0 m/ -1 _O = 5.2 m/
V _{OH}	HIGH level output voltage bus driver outputs	3.98 5.48	4.32 5.81	8	3.84 5.34		3.7 5.2	88.8	V	4.5 6.0	VIH or VIL	$-1_0 = 6.0 \text{ m/s}$ $-1_0 = 7.8 \text{ m/s}$
VOL	LOW level output voltage all outputs	1,0	0 0	0.1 0.1 0.1	C	0.1 0.1 0.1	0	0.1 0.1 0.1	V	2.0 4.5 6.0	VIH or VIL	$I_O = 20 \mu A$ $I_O = 20 \mu A$ $I_O = 20 \mu A$
VoL	LOW level output voltage standard outputs	A.0	0.15 0.16			0.33 0.33	0 81.	0.4	V	4.5 6.0	VIH or VIL	I _O = 4.0 mA I _O = 5.2 mA
VOL	LOW level output voltage bus driver outputs	A:0	0.15 0.16	0.26 0.26		0.33	0 81.	0.4 0.4	V	4.5 6.0	VIH or VIL	I _O = 6.0 mA I _O = 7.8 mA
±1 ₁ 0 10 33 V =	input leakage current	0.1		0.1		1.0		1.0	μА	6.0	V _{CC} or GND	in jt
±I _{OZ}	3-state OFF-state current	0.01		0.5		5.0	0	10.0	μА	6.0	VIH or VIL	Vo = Vcc or GND
Icc 0 =	quiescent supply current SSI flip-flops MSI LSI	40.0 80.0 160.0		2.0 4.0 8.0 50.0		20.0 40.0 80.0 500	24 4 20 20	40.0 80.0 160.0 1000	μΑ μΑ μΑ -μΑ	6.0 6.0 6.0 6.0	VCC or GND	1 _O = 0 1 _O = 0 1 _O = 0

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

					T _{amb} (°C)				TEST CONDITIONS			
	TEST CONDIT				74H0	т							
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	VI	OTHER LAS JOHNYS	
	Marie Ma	min.	typ.	max.	min.	max.	min.	max.					
VIH	HIGH level input voltage	2.0	1.6	# .X	2.0	(7) .30E	2.0	min. 1	V	4.5 to 5.5	Isual M	una l	
VIL	LOW level input voltage	3,5	1.2	0.8	.0.	0.8	.8 0	0.8	V	4.5 to 5.5	di Jewal III		
V _{OH} OS = AH OS =	HIGH level output voltage all outputs	4.4	4.5		4.4	8	4.4	9.T	V	4.5	VIH or VIL	-1 _O = 20 μA	
Vон	HIGH level output voltage standard outputs	3.98	4.32	5	3.84		3.7	5.3 I	V	4.5	VIH or VIL	-1 _O = 4.0 mA	
Vон	HIGH level output voltage bus driver outputs	3.98	4.32	8.3	3.84		3.7	89.8	V	4.5	V _{IH} or V _{IL}	-I _O = 6.0 mA	
Vol	LOW level output voltage all outputs	1.0	0	0.1	ô a	0.1	0	0.1	V	4.5	VIH or VIL	Ι _Ο = 20 μΑ	
Vol	LOW level output voltage standard outputs	1.0 0.0	0.15	0.26	0	0.33	e er.	0.4	V	4.5	V _{IH} or V _{IL}	I _O = 4.0 mA	
Vol	LOW level output voltage bus driver outputs	4.0	0.16	0.26	0	0.33	0 81.	0.4	V	4.5	VIH or VIL	I _O = 6.0 mA	
±I ₁	input leakage current	0.1		0.1		1.0		1.0	μА	5.5	V _{CC} or GND		
±loz V	3-state OFF-state current	0.01		0.5	8	5.0	0	10.0	μΑ	5.5	VIH or VIL	V _O =V _{CC} or GND per input pin; other inputs at V _{CC} or GND; I _O = 0	
Icc 0=	quiescent supply current SSI flip-flops MSI LSI	80.0 80.0 180.0		2.0 4.0 8.0 50.0	8 8 8	20.0 40.0 80.0 500		40.0 80.0 160.0 1000	μΑ μΑ μΑ μΑ	5.5 5.5 5.5 5.5 5.5	V _{CC} or GND	1 ₀ = 0 1 ₀ = 0 1 ₀ = 0 1 ₀ = 0	
ΔI _{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μА	4.5 to 5.5	V _{CC} -2.1 V	other inputs at VCC or GND; IO = 0	

Note

^{1.} The additional quiescent supply current per input is determined by the ΔI_{CC} unit load, which has to be multiplied by the unit load coefficient as given in the individual data sheets. For dual supply systems the theoretical worst-case (V_I = 2.4 V; V_{CC} = 5.5 V) specification is: ΔI_{CC} = 0.65 mA (typical) and 1.8 mA (maximum) across temperature.

DC CHARACTERISTICS FOR 74HCU

Voltages are referenced to GND (ground = 0 V)

Genus							T _{amb} (°C)					TEST CO	NDITIONS
214	WAVEFOR						74HC	U			LINUT	, 8	ETEMAR	OTHER
SYMBOL	PARAMET	ER		+25			-40	to +85	-40 t	o +125	UNIT	V _{CC}	VI	OTHER
				min.	typ.	max.	min.	max.	min.	max.				
VIH	HIGH level	input vo	oltage	1.7 3.6 4.8	1.4 2.6 3.4		1.7 3.6 4.8	1	1.7 3.6 4.8		V	2.0 4.5 6.0	enut tuo endard or	
VIL	LOW level i	input vo	Itage	81	0.6 1.9 2.6	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0	out trans a driver	
Vон	HIGH level	output	voltage	1.8 4.0 5.5	2.0 4.5 6.0		1.8 4.0 5.5		1.8 4.0 5.5		Унач	2.0 4.5 6.0	VIH or VIL	$-1_{O} = 20 \mu A$ $-1_{O} = 20 \mu A$ $-1_{O} = 20 \mu A$
Voh	HIGH level	output	voltage	3.98 5.48	4.32 5.81		3.84 5.34	e ^Y	3.7 5.2		V	4.5 6.0	VCC or GND	-I _O = 4.0 m _s -I _O = 5.2 m _s
VOL	LOW level of			851-	0	0.2 0.5 0.5	For 04	0.2 0.5 0.5	125	0.2 0.5 0.5	V	2.0 4.5 6.0	VIH or VIL	$I_{O} = 20 \mu A$ $I_{O} = 20 \mu A$ $I_{O} = 20 \mu A$
VOL	LOW level of	output v	oltage	222 222	0.15 0.16	0.26 0.26		0.33 0.33	1 9 P	0.4	٧	4.5	VCC or GND	1 _O = 4.0 mA 1 _O = 5.2 mA
±1 ₁	input leaka	ge currer		e ₁		0.1		1.0		1.0	μА	6.0	VCC or GND	1 131
¹ cc	quiescent su SSI	upply cu	rrent			2.0		20.0		40.0	μΑ	6.0	VCC or GND	I _O = 0
SNUTT	MINOU 123						a'l dn							

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

	тезт соирг		T _{amb} (°C)							TEST CONDITIONS			
					74H		UNIT	V	WAVEFORMS				
SYMBOL PARAMETER	PARAMETER	+25			-40 to +85 -		-40 to +125		UNIT	V _{CC}	SYMBOL PARAMETE		
		min.	typ.	max.	min.	max.	min.	max.					
t _{THL} / t _{TLH}	output transition time standard outputs		19 7 6	75 15 13	7 1	95 19 16	\$. 8.	110 22 19	ns epsti	2.0 4.5 6.0	Figs 3 and 4		
t _{THL} / t _{TLH}	output transition time bus driver outputs	6.0	14 5 4	60 12 10	0	75 15 13	0 a.c	90 18 15	ns spar	2.0 4.5 6.0	Figs 3 and 4		

AC CHARACTERISTICS FOR 74HCU

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

			2	3	T _{amb} (°C)			session	TEST CONDITIONS			
CVMDOI	Au DC - at Au D CT	74HCU								Vcc	WAVEFORMS	
AR DV = 01		+25			-40	to +85	-40 to	o +125	UNIT	V	o level WOL	
		min.	typ.	max.	min.	max.	min.	max.				
t _{THL} /	output transition time	4.0 4.0	19 7 6	75 15 13	0	95 19 16	0 87.6	110 22 19	ns	2.0 4.5 6.0	Fig. 1	JoY

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V; } t_r = t_f = 6 \text{ ns; } C_L = 50 \text{ pF}$

SYMBOL			E .		T _{amb} (TEST CONDITIONS				
	24244575				74HC	т			LINUT	.,	WALVEFORMS	
	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
tTHL/ tTLH	output transition time standard outputs		7	15		19		22	ns	4.5	Figs 8 and 9	
tTHL/ tTLH	output transition time bus driver outputs		5	12		15		18	ns	4.5	Figs 8 and 9	

HCU TYPES

AC WAVEFORMS 74HCU

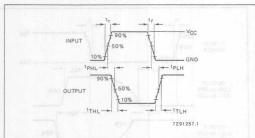


Fig. 1 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

TEST CIRCUIT FOR 74HCU

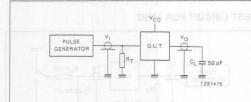


Fig. 2 Test circuit.

Definitions for Fig. 2:

- C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
- $R_T = {}$ termination resistance should be equal to the output impedance Z_O of the pulse generator.

HC TYPES

AC WAVEFORMS 74HC

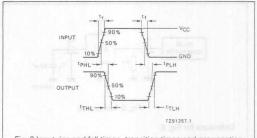


Fig. 3 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

AC WAVEFORMS 74HC

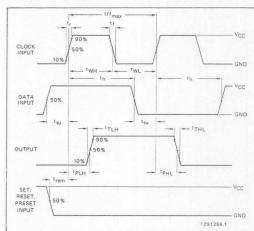


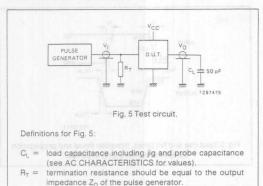
Fig. 4 Set-up times, hold times, removal times, propagation delays and the maximum clock pulse frequency for sequential logic ICs.

Notes to Fig. 4

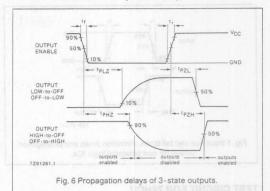
- In Fig. 4 the active transition of the clock is going from LOWto-HIGH and the active level of the forcing signals (SET, RESET and PRESET) is HIGH. The actual direction of the transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.
- 2. For AC measurements: t_r = t_f = 6 ns; when measuring f_{max} , there is no constraint on t_r , t_f with 50% duty factor.

HC TYPES (continued)

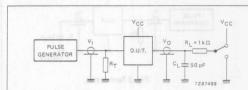
TEST CIRCUIT FOR 74HC



AC WAVEFORMS 74HC (continued)



TEST CIRCUIT FOR 74HC



Switch position

TEST	SWITCH
t _{PZH} t _{PZL} t _{PHZ} t _{PLZ}	GND V _{CC} GND V _{CC}

Note to switch position table

For open-drain N-channel outputs t_{PLZ} and t_{PZL} are applicable.

Fig. 7 Test circuit for 3-state outputs.

Definitions for Fig. 7:

 $C_L = load$ capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

 R_T = termination resistance should be equal to the output impedance Z_0 of the pulse generator.

HCT TYPES

AC WAVEFORMS 74HCT

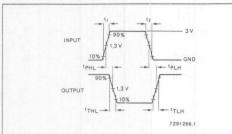
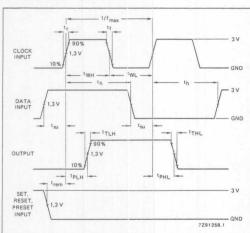


Fig. 8 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

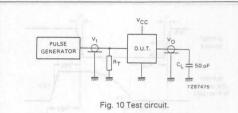
AC WAVEFORMS 74HCT



Notes to Fig. 9

- 1. In Fig. 9 the active transition of the clock is going from LOW-to-HIGH and the active level of the forcing signals (SET, RESET and PRESET) is HIGH. The actual direction of the transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.
- 2. For AC measurements: $t_r = t_f = 6$ ns; when measuring f_{max} , there is no constraint on t_r , t_f with 50% duty factor.

TEST CIRCUIT FOR 74HCT TOHAT SMRO TO YAW DA



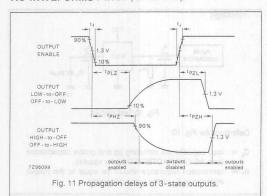
Definitions for Fig. 10:

- C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
- R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.



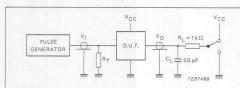
HCT TYPES (continued)

AC WAVEFORMS 74HCT (continued)



Heart file and fall limes, transition times and propagation design (Cs.

TEST CIRCUIT FOR 74HCT



Switch position

TEST	SWITCH
t _{PZH} t _{PZL} t _{PHZ} t _{PLZ}	GND V _{CC} GND V _{CC}

Note to switch position table

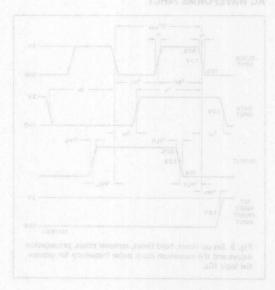
For open-drain N-channel outputs t_{PLZ} and t_{PZL} are applicable.

Fig. 12 Test circuit for 3-state outputs.

Definitions for Fig. 12:

 $C_L = load$ capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

 ${\rm R_T}={\rm termination}$ resistance should be equal to the output impedance ${\rm Z_O}$ of the pulse generator.



INTRODUCTION

The 74HCMOS data sheets have been designed for ease-ofuse. A minimum of cross-referencing for more information is needed

TYPICAL PROPAGATION DELAY AND FREQUENCY

The typical propagation delays listed at the top of the data sheets are the average of t_{PLH} and t_{PHL} for the longest data path through the device with a 15 pF load.

For clocked devices, the maximum frequency of operation is also given. The typical operating frequency is the maximum device operating frequency with a 50% duty factor and no constraints on $t_{\rm r}$ and $t_{\rm f}$.

LOGIC SYMBOLS

Two logic symbols are given for each device — the conventional one (Logic Symbol) which explicitly shows the internal logic (except for complex logic) and the IEC Logic Symbol as developed by the IEC (International Electrotechnical Commission).

The IEC has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic current to each output without explicitly showing the internal logic. Internationally, Working Group 2 of IEC Technical Committee TC-3 has prepared a new document (Publication 617-12) which supersedes Publication 117-15, published in 1972.

RATINGS

The "RATINGS" table (Limiting values in accordance with the Absolute Maximum System — IEC134) lists the maximum limits to which the device can be subjected without damage. This doesn't imply that the device will function at these extreme conditions, only that, when these conditions are removed and the device operated within the Recommended Operating Conditions, it will still be functional and its useful life won't have been shortened

The maximum rated supply voltage of 7 V is well below the typical breakdown voltage of 18 V.

RECOMMENDED OPERATING CONDITIONS

The "RECOMMENDED OPERATING CONDITIONS" table lists the operating ambient temperature and the conditions under which the limits in the "DC CHARACTERISTICS" and "AC CHARACTERISTICS" tables will be met. The table should not be seen as a set of limits guaranteed by the manufacturer, but as the conditions used to test the devices and guarantee that they will then meet the limits in the DC and AC CHARACTERISTICS tables.

DC CHARACTERISTICS

The "DC CHARACTERISTICS" table reflects the DC limits used during testing. The values published are quaranteed.

The threshold values of VIH and VII can be tested by the user. If VIH and VII are applied to the inputs, the output voltages will be those published in the "DC CHARACTER-ISTICS" table. There is a tendency, by some, to use the published VIH and VII thresholds to test a device for functionality in a "function-table exercizer" mode. This frequently causes problems because of the noise present at the test head of automated test equipment with cables up to 1 metre. Parametric tests, such as those used for the output levels under the VIH and VII conditions are done fairly slowly, in the order of milliseconds, so that there is no noise at the inputs when the outputs are measured. But in functionality testing, the outputs are measured much faster, so there can be noise on the inputs, before the device has assumed its final and correct output state. Thus, never use VIH and VII to test the functionality of any HCMOS device type; instead, use input voltages of VCC (for the HIGH state) and 0 V (for the LOW state). In no way does this imply that the devices are noise-sensitive in the final system.

In the data sheets, it may appear strange that the typical V_{1L} is higher than the maximum V_{1L} . However, this is because $V_{1L\max}$ is the maximum V_{1L} (guaranteed) for all devices that will be recognized as a logic LOW. However, typically a higher V_{1L} will also be recognized as a logic LOW. Conversely, the typical V_{1H} is lower than its minimum guaranteed level.

For 74HCMOS, unlike TTL, no output HIGH short-circuit current is specified. The use of this current, for example, to calculate propagation delays with capacitive loads, is covered by the HCMOS graphs showing the output drive capability and those showing the dependence of propagation delay on load capacitance.

The quiescent supply current I_{CC} is the leakage current of all the reversed-biased diodes and the OFF-state MOS transistors. It is measured with the inputs at V_{CC} or GND and is typically a few nA.

AC CHARACTERISTICS

The "AC CHARACTERISTICS" table lists the guaranteed limits when a device is tested under the conditions given in the AC Test Circuits and Waveforms section.

TEST CIRCUITS

Good high-frequency wiring practices should be used in test circuits. Capacitor leads should be as short as possible to minimize ripples on the output waveform transitions and undershoot. Generous ground metal (preferably a groundplane) should be used for the same reasons. A VCC decoupling capacitor should be provided at the test socket, also with short leads. Input signals should have rise and fall times of 6 ns, a signal swing of 0 V to V_{CC} for 74HC and OV to 3V for 74HCT; a 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must be increased for testing fmax. Two pulse generators are usually required for testing such parameters as set-up time, hold time and removal time. f_{max} is also tested with 6ns input rise and fall times, with a 50% duty factor, but for typical f_{max} as high as 60 MHz, there are no constraints on rise and fall times.

The array have use VIE and VIE to test the functionality of the VIEW of the second of the VIEW of the

For 74NCMOS unitles TTL, no output HIGH short-circuit outreat. Is specified. The use of this current, for assemble, to calculate propagation delays with capacitive loads, is covered by the HQMOS graphs showing the dependence of propagation daily on load choose showing the dependence of propagation.

the reversed-blasted diodes and the OFF state MOS translators. It is measured with the incurs at VOC or GND and is synjonly a few nA.

The "AC CHARACTERISTICS" table lists the guaranteed limits when a device it rested under the conditions given in the AC Test Circuits and Waysforms section.

MIRODUCTION

The 74HCMOS data sheet; have been designed for egge-ofuse. A minimum of cross-reterencing for more information is needed.

TYPICAL PROPAGATION DELAY AND PRECIDENCY The typical propagation delays listed of the top of the data theorem are the everage of telly and topy, for the longest tata path through the device with a 18 pF load.

The relicked devices, the maximum frequency of operation a slee sleet. The typical operating frequency is the maximum device operating frequency with a 50% cuty factor and no constraints on t_e and t_e.

Two logic symbols are given for each device — the conventional lone (Logic Symbol) which explicitly shown the internal logic (except for complex logic) and the IEC Logic formions as developed by the IEC (International Electro

The IEC has been developing a very powerful symbolic flanguage that cen show the relationship of each hour of a flanguage that cen show the relationship of each original logic current to each output without explicitly showing the internal logic Internationally, Working Group about IEC Technical Committee TC-3 has prepared a new document Publication 817-121 which supersedes Publication 117-15, published in 1972.

SOUNTA

The "RATINGS" table (Limiting values in accordance with the Absolute Maximum System — IEC134) lists the maximum limits to which the device can be subjected without damage. This desen't imply that this device will function at these excitence conditions, only that when these conditions are removed and the device operated within the Recommended Operating Conditions, it will still be functional and its useful life won't have been shortened.

The maximum rated supply voltage of 7 V is well below the typical breakdown voltage of 18 V.

RECOMMENDED OPERATING CONDITIONS

The "RECOMMENDED OPERATING GONDITIONS" lable lists the operating ambient temperature and the conditions under which the limits in the "DC CHARAC-TERISTICS" and "AC CHARAC-TERISTICS" tables will be met. The stalle should not be seen as a set of limits guaranteed by the manufacturer, but as the conditions used to set the devices and guarantees that they will train meet.

DEFINITIONS OF SYMBOLS AND TERMS USED IN HCMOS DATA SHEETS

Currents

Positive current is defined as conventional current flow into a device.

Negative current is defined as conventional current flow out of a device.

loc	Quiescent power supply current; the current flowing into
	the Voc supply terminal.

ΔI_{CC}	Additional	quiescent	supply	current	per	input	pin	at	а
	specified input voltage and V _{CC} .								

I _{GND}	Quiescent power	supply	current:	the	current	flowing	into
	the GND terminal	- 50-11-3					

ad Hite	Input leakage current; the current flowing into a device at a
	specified input voltage and V _{CC} .

I _{IK}	Input diode current; the current flowing into a device at a
	specified input voltage.

$$I_{\rm OK}$$
 . Output diode current; the current flowing into a device at a specified output voltage.

loz	OFF-state output current; the leakage current flowing into
	the output of a 3-state device in the OFF-state, when the
	output is connected to V _{CC} or GND.

Is Analog switch leakage current; the current flowing into an analog switch at a specified voltage across the switch and V_{CC}.

Voltages

All voltages are referenced to GND (ground), which is typically 0 V.

GND	Supply voltage; for a device with a single negative power					
	supply, the most negative power supply, used as the					
	reference level for other voltages; typically ground.					

V_{CC} Supply voltage; the most positive potential on the device.

V_{EE} Supply voltage; one of two (GND and V_{EE}) negative power

V_H Hysteresis voltage; difference between the trigger levels, when applying a positive and a negative - going input signal.

V_{IH} HIGH level input voltage; the range of input voltages that represents a logic HIGH level in the system.

V_{IL} LOW level input voltage; the range of input voltages that represents a logic LOW level in the system.

V_{OH} HIGH level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.

V_{OL} LOW level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.

 V_{T+} Trigger threshold voltage; positive-going signal.

V_T- Trigger threshold voltage; negative-going signal.

Analog terms

R_{ON} ON-resistance; the effective ON-state resistance of an analog switch, at a specified voltage across the switch and output load

 ΔR_{ON} ΔON -resistance; the difference in ON-resistance between any two switches of an analog device at a specified voltage across the switch and output load.

Capacitances JOHAT bas OHAT our and strategy

C_t Input capacitance; the capacitance measured at a terminal connected to an input of a device.

C_{I/O} Input/Output capacitance; the capacitance measured at a terminal connected to an I/O-pin (e.g. a transceiver).

C_L Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.

C_{PO} Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function, when no extra load is provided to the device.

 $C_{\widehat{S}}$. Switch capacitance; the capacitance of a terminal to a switch of an analog device.

AC switching parameters

fi Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device function table. For sequential logic devices the clock frequency using alternate HIGH and LOW for data input or using the toggle mode, whichever is applicable.

fo Output frequency; each output.

f_{max} Maximum clock frequency; clock input waveforms should have a 50% duty factor and be such as to cause the outputs to be switching from 10%V_{CC} to 90%V_{CC} in accordance with the device function table.

Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

Clock input rise and fall times; 10% and 90% values.

- tpHL Propagation delay; the time between the specified reference points, normally the 50% points for 74HC and 74HCU devices on the input and output waveforms and the 1.3 V points for the 74HCT devices, with the output changing from the defined HIGH level to the defined LOW level.
- tplh Propagation delay; the time between the specified reference points, normally the 50% points for 74HC and 74HCU devices on the input and output waveforms and the 1.3 V point for the 74HCT devices, with the output changing from the defined LOW level to the defined HIGH level.
- tpHZ 3-state output disable time; the time between the specified reference points, normally the 50% points for the 74HC and 74HCU devices and the 1.3 V points for the 74HCT devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a HIGH level (V_{OH}) to a high impedance OFF-state (Z).
- tpLZ 3-state output disable time; the time between the specified reference points, normally the 50% points for the 74HC devices and the 1.3 V points for the 74HCT devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a LOW level (VOL) to a high impedance OFF-state (Z).
- tpZH 3-state output enable time; the time between the specified reference points, normally the 50% points for the 74HC devices and 1.3 V points for the 74HCT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a HIGH level (VOH).
- tpzl 3-state output enable time; the time between the specified reference points, normally the 50% points for the 74HC devices and the 1.3 V points for the 74HCT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a LOW level (VOL).

- trem Removal time; the time between the end of an overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at the 50% points for 74HC devices and the 1.3 V points for the 74HCT devices on both input voltage waveforms.
- t_{su}

 Set-up time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the coltrol input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.
- thl Output transition time; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from HIGH-to-LOW.
- the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW-to-HIGH.
- t_W Pulse width; the time between the 50% amplitude points on the leading and trailing edges of a pulse for 74HC and 74HCU devices and at the 1.3 V points for 74HCT devices.



QUAD 2-INPUT NAND GATE

FEATURES

Output capability: standard

• I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT00 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT00 provide the 2-input NAND function.

		CONDITIONS	TYPI	UNIT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
tPHL/ tPLH	propagation delay nA, nB to nY	C _L = 15 pF V _{CC} = 5 V	7	10	ns
CI	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per gate	notes 1 and 2	22	22	pF

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD \times VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

f; = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

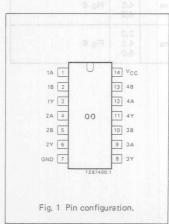
2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

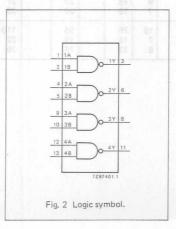
PACKAGE OUTLINES

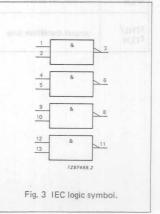
14-lead DIL; plastic (SOT27)

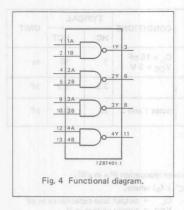
14-lead mini pack; plastic (SO14; SOT108A)

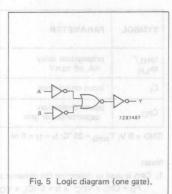
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs 9973MA9A9 JOBMY3
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	Vcc	positive supply voltage











FUNCTION TABLE 23RUTA24

INP	UTS	OUTPUT					
nA	nB	nY					
	iesch-doid in	е потт Н том					
		H					
Hotm	night saward	wol da Holdis					
H	H	LTTS					

H = HIGH voltage level L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: SSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \ V: t_r = t_f = 6 \ ns: C_1 = 50 \ pF$

	UNICTION		MAM		10	T _{amb} (°C)				TEST CONDITIONS			
OVIMBO!	040445750	sindi			Ah	74	нс	9, 12	.1	UNIT	V	MANE	OPMS
SYMBOL	PARAMETER		o halo	+25	Ya	-40	to +85	-40 to	+125	UNIT	V _{CC}	WAVEFORMS	
	(V 0)		min.	typ.	max.	min.	max.	min.	max.				
tPHL/	propagation delay nA, nB to nY			25 9 7	90 18 15	331	115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 6	
^t THL/ ^t TLH	output transition t	me		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6	
						d	m/s		71		207 [8]	U	1) 41
						5							

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: SSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

		T _{amb} (°C)							TEST CONDITIONS			
SYMBOL	PARAMETER				741	HCT			UNIT	Vcc	WAVEFORMS	
STIMBOL	PARAMETER		+25		-40	to +85	-40 to	0 +125	Olvii	V		
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay nA, nB to nY		12	19		24		29	ns	4.5	Fig. 6	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 6	

AC WAVEFORMS

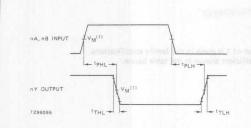


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

For the OC characteristics are chapter "HCMC

CC strugery: set
Vote to NCT sypa:
The value of additional quiescent supply current (SICC) for a life value of additional quiescent supply current (SICC) for a life value by the unit is

INPUT UNIT LOAD
AN AS 1.50

Note to AC waveforms M ROA SOITSIRBTDARAND OA

(1) HC: $V_M = 50\%$; $V_I = GND$ to V_{CC} .

EST CONDITIONS	Ţ	ME		(0)	des	CI: V	M = 1.3	V; V ₁ = GND to 3 V.	

QUAD 2-INPUT NOR GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT02 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT02 provide the 2-input NOR function.

01/14001		CONDITIONS	TYP	UNIT	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
tPHL/ tPLH	propagation delay nA, nB to nY	C _L = 15 pF V _{CC} = 5 V	7	9	ns
Cl	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	22	24	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

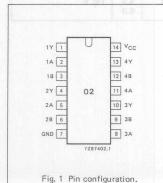
- 1. CPD is used to determine the dynamic power dissipation (P_D in μ W); PD = CPD × VCC² × f₁ + Σ (CL × VCC² × f₀) where:
 - f_i = input frequency in MHz f_O = output frequency in MHz
- C_L = output load capacitance in pF V_{CC} = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

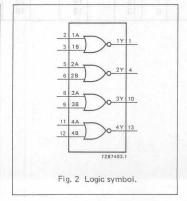
PACKAGE OUTLINES

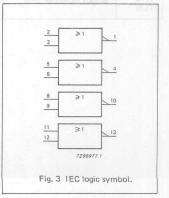
14-lead DIL; plastic (SOT27)

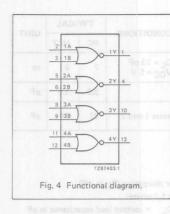
14-lead mini pack; plastic (SO14; SOT108A)

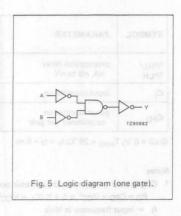
PIN NO.	SYMBOL	NAME AND FUNCTION MARKET JOHNY
1, 4, 10, 13	1Y to 4Y	data outputs
2, 5, 8, 11	1A to 4A	data inputs
3, 6, 9, 12	1B to 4B	data inputs
7	GND	ground (0 V)
14	Vcc	positive supply voltage











FUNCTION TABLE

INP	UTS	OUTPUT
nA	nB	nY
L	HOLTSIR	ENERAL DESC
L bes	GETH HE	NO TAHISANGTOS
H oig	enallane sec	gate CINOS devin
Hillori	2 HVOOV	ol miw dditerm

H = HIGH voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V; } t_r = t_f = 6 \text{ ns; } C_1 = 50 \text{ pF}$

			T _{amb} (°C)							TEST CONDITIONS		
SYMBOL	PARAMETER	74HC							UNIT	\/	WAVEFORMS	
STIVIBUL	PARAMETER	res estat	+25		-40 t	o +85	-40 t	o +125	OWIT	V _{CC}	WAVEFORMS	
	and	min.	typ.	max.	min.	max.	min.	max.				
tPHL/	propagation delay	lata idi bouot round	25 9 7	90 18 15	B to A SHD VCC	115 23 20	9, 12	135 27 23	ns	2.0 4.5 6.0	Fig. 6	
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: SSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	VENEGUE V										TEST CONDITIONS		
SYMBOL PARAMETER	74HCT								V/	WAVEFORMS			
	+25		-40 to +85		-40 to +125		UNIT	VCC	WAVEI OHMS				
		min.	typ.	max.	min.	max.	min.	max.					
tPHL/ tPLH	propagation delay nA, nB to nY		11	19		24		29	ns	4.5	Fig. 6		
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 6		

AC WAVEFORMS

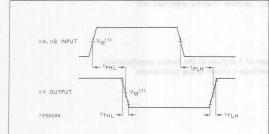


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

DC CHARACTERISTICS POR TARCT

Output oxpability: standar

movt TOH of stold

The value of midliforal quiescent supply current (Alogs). To determine a log per input, multiply this value by the

IMPUT UNIT LOAD
COEFFICIENT

AC CHARACTERISTICS FOR 74HCT

Note to AC waveforms 39 Da = 10 an a = 11 = 17 W D = 014a

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} .

HCT: $V_M = 1.3 \text{ V}$; $V_1 = \text{GND to 3 V}$.

CL = output load capacitance in pF

V_{CC} = supply voltage in V

 $R_L = pull-up resistor in M\Omega$

QUAD 2-INPUT NAND GATE

FEATURES

- · Level shift capability
- Output capability: standard (open drain)
- · ICC category: SSI

GENERAL DESCRIPTION

The 74HC/HCT03 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT03 provide the 2-input NAND function.

The 74HC/HCT03 have open-drain Ntransistor outputs, which are not clamped by a diode connected to VCC. In the OFF-state, i.e. when one input is LOW, the output may be pulled to any voltage between GND and V_{Omax}. This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

SYMBOL	PARAMETER	CONDITIONS	TYF	UNIT	
STWIBOL	PANAMETER	CONDITIONS	НС	нст	UNIT
t _{PZL} /	propagation delay	C _L = 15 pF R _L = 1 kΩ V _{CC} = 5 V	8	10	ns
CI	input capacitance	g lyn	3.5	3.5	pF
C _{PD}	power dissipation capacitance per gate	notes 1, 2 and 3	4.0	4.0	pF

GND = 0 V;
$$T_{amb} = 25 \, ^{\circ}C$$
; $t_r = t_f = 6 \, \text{ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$P_{D} = C_{PD} \times V_{CC}^{2} \times f_{i} + \Sigma (C_{L} \times V_{CC}^{2} \times f_{o}) +$$

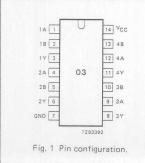
- + Σ (V_O²/R_L) x duty factor LOW, where:
- f; = input frequency in MHz
- fo = output frequency in MHz
- V_O = output voltage in V Σ ($C_L \times V_{CC}^2 \times f_O$) = sum of outputs Σ (V_O^2/R_L) = sum of outputs
- 2. For HC the condition is V_1 = GND to V_{CC} For HCT the condition is V_1 = GND to V_{CC}
- 3. The given value of CPD is obtained with:
- CL = 0 pF and RL = ∞

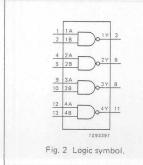
PACKAGE OUTLINES

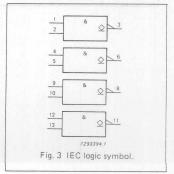
14-lead DIL; plastic (SOT27)

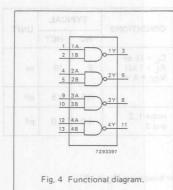
14-lead mini pack; plastic (SO14; SOT108A)

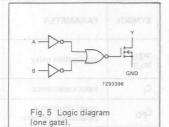
PIN NO.	SYMBOL	NAME AND FUNCTION	
1, 4, 9, 12	1A to 4A	data inputs	GMBIS
2, 5, 10, 13	1B to 4B	data inputs	
3, 6, 8, 11	1Y to 4Y	data outputs of some in rawage	
7 25 45	GND	ground (0 V)	
14	Vcc	positive supply voltage	











FUNCTION TABLE

INP	UTS	OUTPUT
nA	nB	nY ⁽¹⁰⁾
L	L	Z 7
Н	H	DTAN LUNC ME

H = HIGH voltage level

L = LOW voltage level

Z = high impedance OFF-state

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134) Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS Lavel HOLH signs a drillage of
Vcc	DC supply voltage	-0.5	+7	V	3. The give
Vo	DC output voltage	-0.5	+7	V	
IK	DC input diode current		20	mA	for $V_1 < -0.5 \text{ V}$ or $V_1 > V_{CC} + 0.5 \text{ V}$
-1ок	DC output diode current	1108 (4	20	mA	for $V_0 < -0.5 \text{ V}$
-10	DC output sink current		25	mA	for -0.5 V < V _O
±I _{CC} ; ±I _{GND}	DC VCC or GND current		50	mA	ON MIS
T _{stg}	storage temperature range	-65	+150	°C	2.5.10.1
P _{tot}	power dissipation per package		750	mW	for temperature range; —40 to +125 °C 74HC/HCT above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", except that the V_{OH} values are not valid for open drain. They are replaced by I_{OZ} as given below.

Output capability: standard (open drain), excepting $V_{\mbox{OH}}$ $I_{\mbox{CC}}$ category: SSI

Voltages are refereced to GND (ground = 0 V)

	TEST CONDITIONS		T _{amb} (°C)								TEST CONDITIONS		
OVERDOL DARAMETER			74HC							UNIT	V	Vi	OTHER
SYMBOL PARAMETER		+25			-40	to +85	-40 to +125		ONT	V _{CC}	PLANA	OTHER	
			min.	typ.	max.	min.	max.	min.	max.				
loz o	HIGH level output leakage current	Au	10.0		0:5		5.0		10.0	μА	2.0 to 6.0	VIL	V _O = V _O (max) or GND

^{*} The maximum operating output voltage (VO(max)) is 6.0 V.

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_1 = 50 pf$

		T _{amb} (°C)								TEST CONDITIONS		
SYMBOL	YMBOL PARAMETER	74HC						UNIT	Vcc	WAVEFORMS		
STWIDOL		+25			-40 to +85		-40 to +125		OIVII	V CC	WAVEFOR	TIVIS
		min.	typ.	max.	min.	max.	min.	max.	A TANCE	15 FO		
tPZL/	propagation delay nA, nB to nY		28 10 8	95 19 16	on	120 24 20		145 29 25	ns ns	2.0 4.5 6.0	Fig. 6	N 0 = QVI
tTHL ZM	output transition time	+125	19 7 6	75 15 13	MARIC -	95 19 16	+25	110 22 19	ns	2.0 4.5 6.0	Fig. 6	SYMBOL

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", except that the V_{OH} values are not valid for open drain. They are replaced by I_{OZ} as given below.

Output capability: standard (open drain), excepting $V_{\mbox{OH}}$ I $_{\mbox{CC}}$ category: SSI

Voltages are refereced to GND (ground = 0 V)

	YEST COND				T _{amb} (°C)					TEST CO	NDITIONS
SYMBOL PARAMETER		74HCT						LINUT	V-89	VI	OTHER	
	+125	+25		-40 to +85		-40 to +125		UNIT	V _{CC}	VI	OTHER	
		min.	typ.	max.	min.	max.	min.	max.				
I _{OZ}	HIGH level output leakage current	40, 9.01		0.5	3	5.0		10.0	μА	4.5 to 5.5	Isval HE	V _O = V _O (max) or GND

^{*} The maximum operating output voltage (VO(max)) is 6.0 V.

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

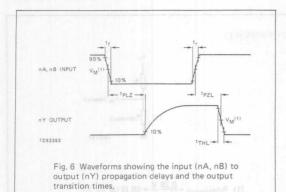
INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.0

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

	AS A.5 Fig. 6	29		T	amb (C)				T	EST CONDITIONS	
SYMBOL	YMBOL PARAMETER		74HCT									
STMBOL PARAMETER		+25		-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.				
tPZL/ tPLZ	propagation delay nA, nB, to nY		12	24		30		36	ns	4.5	Fig. 6	
^t THL	output transition time		7	15		19		22	ns	4.5	Fig. 6	

AC WAVEFORMS



200722 10) 20, 4, 9,02.7,03 10) 20, 4, 9,02.7,03

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

TEST CIRCUIT AND WAVEFORMS

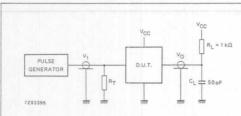


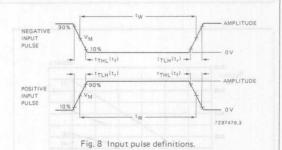
Fig. 7 Test circuit (open drain)

Definitions for Figs. 7 and 8:

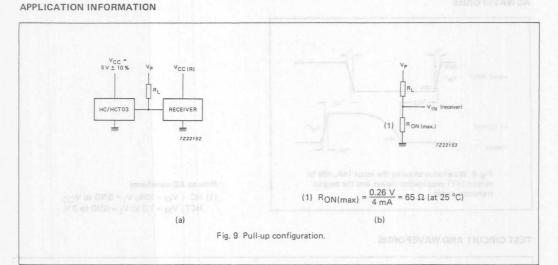
C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

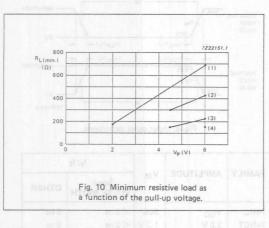
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

 $t_r = t_f = 6$ ns; when measuring f_{max} , there is no constraint on t_r , t_f with 50% duty factor.



			t _r ; t _f	
FAMILY	AMPLITUDE	VM	f _{max} ; PULSE WIDTH	OTHER
74HC	Vcc	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns





Notes to Figs 9 and 10

If $V_P - V_{CC}(R) > 0.5 V$ a positive current will flow into the receiver (as described in the USER GUIDE; input/output protection), this will not affect the receiver provided the current does not exceeds 20 mA. At $V_{CC} < 4.5 \text{ V}$, $R_{ON(max)}$ is not guaranteed; RON(max) can be estimated using Figs 33 and 34 in the USER GUIDE.

Notes to Fig. 10

- 1. V_{CC} (R) = 2.0 V; V_{IL} = 0.5 V. 2. V_{CC} (R) = 5.0 V; V_{IL} = 0.8 V. 3. V_{CC} (R) = 4.5 V; V_{IL} = 1.35 V. 4. V_{CC} (R) = 6.0 V; V_{IL} = 1.8 V.

Note to Application information

All values given are typical unless otherwise specified.

HEX INVERTER

FEATURES BLEAT MOITOMUR

- · Output capability: standard
- · Icc category: SSI

GENERAL DESCRIPTION

The 74HC/HCT04 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT04 provide six inverting buffers.

		CONDITIONS	TYF	LIALLT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
tPHL/ tPLH	propagation delay nA to nY	C _L = 15 pF V _{CC} = 5 V	7	8	ns
Claravii a	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	21	24	pF

GND = 0 V;
$$T_{amb} = 25 \,^{\circ}\text{C}$$
; $t_r = t_f = 6 \, \text{ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

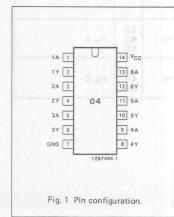
- f; = input frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V

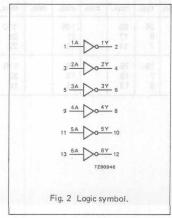
- f_0 = output frequency in MHz Σ (C_L × V_{CC}² × f_0) = sum of outputs
- 2. For HC the condition is VI = GND to VCC For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 V$

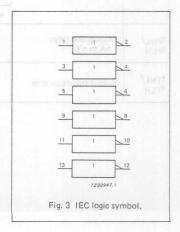
PACKAGE OUTLINES 14-lead DIL; plastic (SOT27)

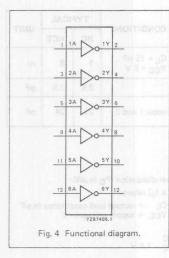
14-lead mini pack; plastic (SO14; SOT108A)

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs a 08 = 10 km 8 = 11 = 12 M 0 = 0.4
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7 (5)	GND	ground (0 V)
14	Vcc	positive supply voltage









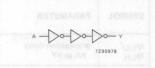


Fig. 5 Logic diagram (one inverter).

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	Н
eHads-ubit o	to POTUPLEMEN an

H = HIGH voltage level L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}_{\text{Nught of the }}$

	TV 01	T _{amb} (°C)								TEST CONDITIONS	
SYMBOL	PARAMETER										WAVEFORMS
		+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
^t PHL/ ^t PLH	propagation delay nA to nY		25 9 7	85 17 14	204	105 21 18		130 26 22	ns	2.0 4.5 6.0	Fig. 6
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD
nA	1.20

AC CHARACTERISTICS FOR 74HCT $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

SYMBOL	PARAMETER	T _{amb} (°C)								TEST CONDITIONS	
											WANEEO DAG
		+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/ tPLH	propagation delay nA to nY		10	19		24		29	ns	4.5	Fig. 6
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

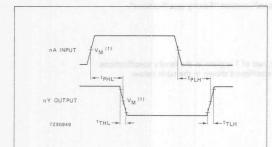


Fig. 6 Waveforms showing the data input (nA) to data output (nY) propagation delays and the output transition times.

DC CHARACTERISTIES FOR MHCT

bacteria extilidades ruquel

social TOM or sould

The value of additional quiescent supply current (AICC) for a or To determine AICC per input, multiply this value by the unit to

Note to AC waveforms

(1) HC: $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

HEX INVERTER

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HCU04 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.

The 74HCU04 is a general purpose hex inverter. Each of the six inverters is a single stage.

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	Н
Н	L

H = HIGH voltage level L = LOW voltage level

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
tPHL/ tPLH	propagation delay nA to nY	C _L = 15 pF V _{CC} = 5 V	5	ns
CI	input capacitance		3.5	pF
CPD	power dissipation capacitance per inverter	note 1	10	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

fi = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

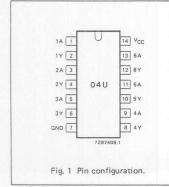
 f_0 = output frequency in MHz Σ (C_L x V_{CC}² x f_0) = sum of outputs

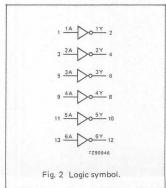
PACKAGE OUTLINES

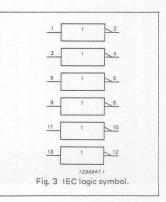
14-lead DIL; plastic (SOT27)

14-lead mini pack; plastic (SO14; SOT108A)

PIN NO.	SYMBOL	NAME AND FUNCTION	
1, 3, 5, 9, 11, 13	1A to 6A	data inputs	
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs	
7	GND	ground (0 V)	
14	Vcc	positive supply voltage	







HEX INVERTER

PEATURES

Output capability: standard
 Icin catagory: SSI

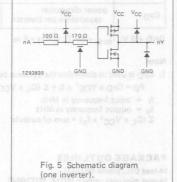
GENERAL DESCRIPTION

The TAHCUOM is a high-speed Si-care CMOS device and is pin compatible with low power Schottley THE (LSTTL), it is specified in compliance with JEDEC standard no. 7A. The 74HCUOM is a general purpose hes inverter. Each of the six inverters is

FUNCTION TABLE

FI = HIGH voltage level L = LOW voltage level

1 1A 0 1Y 2 3 2A 0 2Y 4 5 3A 0 3Y 6 9 4A 0 4Y 8 11 5A 5Y 10 7287408.1 Fig. 4 Functional diagram.



25% DESCRIPTION







DC CHARACTERISTICS FOR 74HCU

Voltages are referenced to GND (ground = 0 V)

					T _{amb} (°C)					TEST CC	NDITIONS
SYMBOL	PARAMETER	74HCU							UNIT	Vcc	VI	OTHER
STINIBUL	PARAMETER	8514	252+ +25		-40 to +85		-40 to +125		UNIT	V CE	VIAB	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
V _{IH}	HIGH level input voltage	1,7 3.6 4.8	1.4 2.6 3.4	0100	1.7 3.6 4.8	0 4 2	1.7 3.6 4.8		V	2.0 4.5 6.0	noiregeq Yn or A	
VIL	LOW level input voltage	110 22 18	0.6 1.9 2.6	0.3 0.9 1,2		0.3 0.9 1.2	19 7	0.3 0.9 1.2	V	2.0 4.5 6.0	nusi Juqi	ue UHT
V _{OH}	HIGH level output voltage	1.8 4.0 5.5	2.0 4.5 6.0		1.8 4.0 5.5		1.8 4.0 5.5		٧	2.0 4.5 6.0	VIH or VIL	-I _O = 20 μA -I _O = 20 μA -I _O = 20 μA
Vон	HIGH level output voltage		4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	VCC or GND	-I _O = 4.0 mA -I _O = 5.2 mA
VoL	LOW level output voltage		0 0 0	0.2 0.5 0.5		0.2 0.5 0.5		0.2 0.5 0.5	V	2.0 4.5 6.0	VIH or VIL	I _O = 20 μA I _O = 20 μA I _O = 20 μA
VOL	LOW level output voltage		0.15 0.16	0.26 0.26		0.33 0.33	417-4	0.4	V	4.5 6.0	VCC or GND	I _O = 4.0 mA I _O = 5.2 mA
±ΙΙ	input leakage current	arrest of	August 1	0.1	100	1.0			μА	6.0	V _{CC} or GND	V/ B giP == c step or
^I CC	quiescent supply current	MD = 1	V : NEÓ	2.0	(1)	20.0		40.0	μА	6.0	V _{CC} or GND	IO = 0

AC CHARACTERISTICS FOR 74HCU

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

SHOUL			T _{amb} (°C)						TEST CONDITIONS			
	PARAMETER		74HCU							V	WAVEFORMS	
SYMBOL P	PARAMETER	+25		- 88	-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORING	
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/ tPLH	propagation delay nA to nY		19 7 6	70 14 12	5.0 6.1 8.1	90 18 15	6.5 6.5 A.1	105 21 18	ns	2.0 4.5 6.0	Fig. 601H	
tTHL/ tTLH	output transition time	0.3 0.9 1.2	19 7 6	75 15 13		95 19 16	0 8 0 8 0 8	110 22 19	ns seat	2.0 4.5 6.0	Fig. 6.01	

AC WAVEFORMS

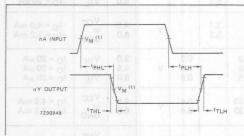
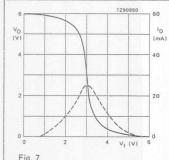


Fig. 6 Waveforms showing the data input (nA) to data output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) $V_M = 50\%$; $V_I = GND$ to V_{CC} .

TYPICAL TRANSFER CHARACTERISTICS



 $\frac{1}{10} = 0$; $\frac{1}{10} = 0$

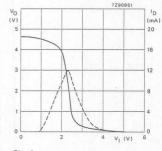


Fig. 8 \sim V_O; $- - - I_D$ (drain current) $I_O = 0$; V_{CC} = 4.5 V.

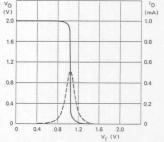


Fig. 9 V_0 ; ----I_D (drain current) V_0 = 0; V_{CC} = 2.0 V.

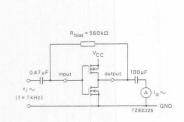


Fig. 10 Test set-up for measuring forward transconductance $g_{fs} = di_0/dv_i$ at vo is constant (see also graph Fig. 11).

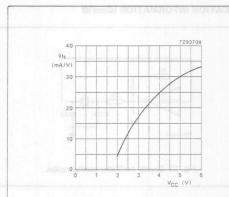


Fig. 11 Typical forward transconductance gfs as a function of the supply voltage VCC at T_{amb} = 25 °C.

APPLICATION INFORMATION

Some applications for the "HCU04" are:

- Linear amplifier (see Fig. 12)
- In crystal oscillator designs (see Fig. 13)
- Astable multivibrator (see Fig. 14)

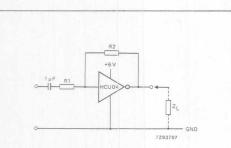


Fig. 12 HCU04 used as a linear amplifier.

Note to Fig. 12

$$Z_L > 10 \text{ k}\Omega$$
; $A_{OL} = 20 \text{ (typ.)}$

Note to Fig. 12
$$Z_{L} > 10 \text{ k}\Omega; A_{OL} = 20 \text{ (typ.)}$$

$$A_{u} = -\frac{A_{OL}}{1 + \frac{R1}{R2} (1 + A_{OL})}; \quad \text{Vo max (p-p)}$$

$$\approx \text{V}_{CC} - 2 \text{ V centered at } \% \text{ V}_{CC}$$

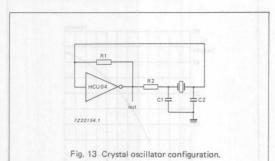
 $3 \text{ k}\Omega \leq \text{R1, R2} \leq 1 \text{ M}\Omega$

Typical unity gain bandwidth product is 5 MHz. C₁ (see Fig. 15)

AOL = open loop amplification Au = voltage amplification

	(GM)	

APPLICATION INFORMATION (Cont'd)



Note to Fig. 13

C₁ = 47 pF (typ.) V species viscus set to solbout set C₂ = 33 pF (typ.)

 $C_2 = 33 \text{ pF (typ.)}$ $R_1 = 1 \text{ to } 10 \text{ M}\Omega \text{ (typ.)}$

R₂ optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} is typically 5 mA at V_{CC} = 5 V and f = 10 MHz).

OPTIMUM VALUE FOR R2

FREQUENCY (MHz)	R ₂ (kΩ)	OPTIMUM FOR minimum required I _{CC} minimum influence due to change in V _{CC}					
3	2 8						
6	1 4.7	minimum I _{CC} minimum I _{CC} minimum I _{CC} minimum I _{CC}					
10	0.5						
14	0.5	minimum I _{CC}					
> 14	replace R ₂ by C ₃ with a typical value of 35 pF						

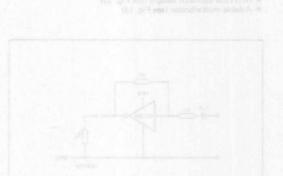
EXTERNAL COMPONENTS FOR RESONATOR (f < 1 MHz)

FREQUENCY (kHz)	R ₁ (MΩ)	R ₂ (kΩ)	C ₁ (pF)	C ₂ (pF)	
10 to 15.9	22	220	56	20	
16 to 24.9	22	220	56	10	
25 to 54.9	22	100	56	10 5 5	
55 to 129.9	22	100	47		
130 to 199.9	22	47	47		
200 to 349.9	10	47	47	5	
350 to 600	10	47	47	5	

Where:

All values given are typical and must be used as an initial set-up.





· Linear amplifier (see Fig. 12)

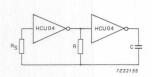


Fig. 14 HCU04 used as an astable multivibrator

Note to Fig. 14

$$f = \frac{1}{T} \approx \frac{1}{2.2 \text{ RC}}$$

 $R_{\text{S}}\approx 2\times R.$

The average I $_{CC}$ (mA) is approximately 3.5 + 0.05 x f (MHz) x C (pF) at V $_{CC}$ = 5.0 V (for more information refer to DESIGNERS GUIDE).

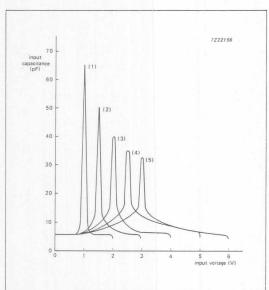


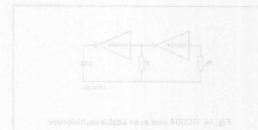
Fig. 15 Typical input capacitance as a function of input voltage.

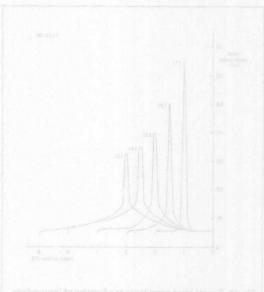
Note to Fig. 15

1. V_{CC} = 2.0 V. 2. V_{CC} = 3.0 V. 3. V_{CC} = 4.0 V. 4. V_{CC} = 5.0 V. 5. V_{CC} = 6.0 V.

Note to Application information

All values given are typical unless otherwise specified.





QUAD 2-INPUT AND GATE

FEATURES

- Output capability: standard
- ICC category: SSI

GENERAL DESCRIPTION

The 74HC/HCT08 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT08 provide the 2-input AND function.

SYMBOL	242445752	CONDITIONS	TYF	UNIT		
	PARAMETER	CONDITIONS	нс	нст	UNIT	
^t PHL [/]	propagation delay nA, nB to nY	C _L = 15 pF V _{CC} = 5 V	7	11	ns	
C _I	input capacitance	e trace	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	10	20	pF	

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

- f; = input frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V
- fo = output frequency in MHz
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

PACKAGE OUTLINES

14-lead DIL; plastic (SOT27)

14-lead mini pack; plastic (SO14; SOT108A)

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs and the south account of 20 and 197
3, 6, 8, 11	1Y to 4Y	data outputs business systill deges sugred
7	GND	ground (0 V)
14	Vcc	positive supply voltage

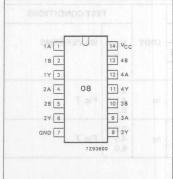
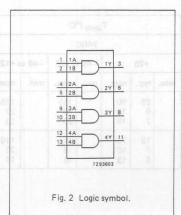
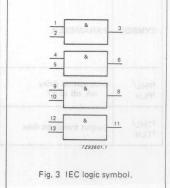
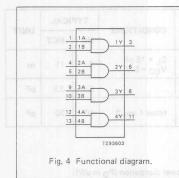


Fig. 1 Pin configuration.







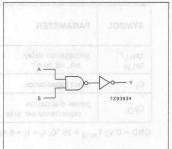
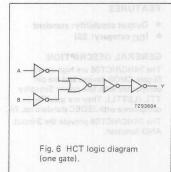


Fig. 5 HC logic diagram (one gate).



FUNCTION TABLE

INP	UTS	OUTPUT		
nA	nB	nY		
L	L	L		
L	Н	L		
H	L	L		
Н	Н	Н		

H = HIGH voltage level L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: SSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

			T _{amb} (°C)							TEST CONDITIONS		
CYMPOL	DADAMETED		иE	74HC						Vcc	WAVEFORMS	
SYMBOL	PARAMETER	+25		-40 to +85		-40 to +125		UNIT	V	WAVEFORMO		
		min.	typ.	max.	min.	max.	min.	max.		A& 20	571	
tPHL/	propagation delay nA, nB to nY		25 9 7	90 18 15	9	115 23 20		135 27 23	ns	2.0 4.5 6.0	80 Fig. 7	E AS
tTHL/ M	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7	Ti ano

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	0.6

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		T _{amb} (°C) 74HCT								TEST CONDITIONS		
CVMPOL	PARAMETER									V	WAVEFORMS	
SYMBOL		+25			-40 to +85 -		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay nA, nB to nY		14	24		30		36	ns	4.5	Fig. 7	
t _{THL} /	output transition time		7	15		19		22	ns	4.5	Fig. 7	

AC WAVEFORMS

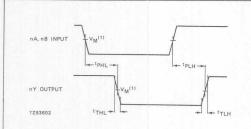


Fig. 7 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

DC CHARACTERISTICS FOR 249CT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications",

Output capability: standard

LCC category: SSI

Note to HCT types

he value of additional quiescent supply current ($\Delta l g g$) for a unit load of 1 is given in the case partitioning of general above in the case palow.

AC CHARACTERISTICS FOR JAHOT

GND = 0 W; ty = 1r = 6 ns; Ct = 50 pl

AC WAVEFORMS

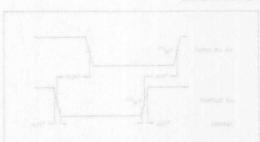


Fig. 7 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output stansisten times.



1) HC : V_M = 503; V₁ = GND to V_{CC}: HCC: V_M = 1.3 V₁ V₂ = GND to 3 V₂

TRIPLE 3-INPUT NAND GATE

FEATURES A MALT MOITOMUS

Output capability: standard

Icc category: SSI

GENERAL DESCRIPTION

The 74HC/HCT10 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT10 provide the 3-input NAND function.

SYMBOL PARAMETER		CONDITIONS	TY	LIMIT	
STWIBOL	PANAMETER	CONDITIONS	нс	нст	UNIT
tPHL/ tPLH	propagation delay nA, nB, nC to nY	C _L = 15 pF V _{CC} = 5 V	9	11	ns
CI	input capacitance	8 42	3.5	3.5	pF
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	12	14	pF

GND = 0 V; $T_{amb} = 25 \,^{\circ}C$; $t_r = t_f = 6 \, \text{ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x VCC^2 x f_i + Σ (CL x VCC^2 x f_o) where:

fi = input frequency in MHz f_O = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

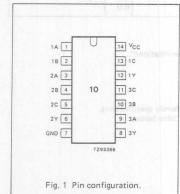
2. For HC the condition is VI = GND to VCC For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 V$

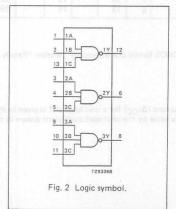
PACKAGE OUTLINES

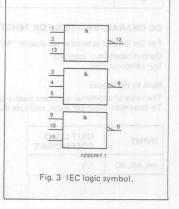
14-lead DIL; plastic (SOT27)

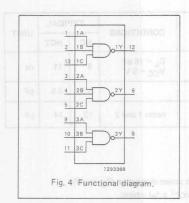
14-lead mini pack; plastic (SO14; SOT108A)

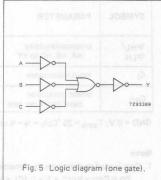
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
13, 5, 11	1C to 3C	data inputs
12, 6, 8	1Y to 3Y	data outputs velsb neiseasgong velsuses
7 05	GND	ground (0 V)
14	Vcc	positive supply voltage











FUNCTION TABLE SERUTAER

	INPUTS	SE : Viola	OUTPUT
nA	nB	nC	nY
Laid	L	so Lab a	OMO Has is
vL:ton	Sowal St	w H daile	slon H mos
L boll	Н	volt /	TLH
C. La long	an Hara	Hariy	reamilH mas
Н	oring the	L	Н
Н	L	H	Н
Н	Н	L	Н
Н	Н	Н	L

H = HIGH voltage level L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: SSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

			T _{amb} (°C)						TEST CONDITIONS				
	AND FUNCTION ON	NAME OF		108	74HC		CARE DITO	7	UNIT	Vcc	WAVEFORMS		
SYMBOL	PARAMETER	gni strib	+25		-40	to +85	-40 t	-40 to +125				V	W. C. C.
			typ.	max.	min.	max.	min.	max.					
tPHL/		oni susti rubizteto foruceg	30 11 9	95 19 16	10 Yr	120 24 20	2.6,1	145 29 25	ns	2.0 4.5 6.0	Fig. 6		
tTHL/ tTLH	output transition time	avillano.	19 7 6	75 15 13	gV]	95 19 16	4.	110 22 19	ns	2.0 4.5 6.0	Fig. 6		

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Output capability: standard

ICC category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

		T _{amb} (°C)								TEST CONDITIONS	
OVIMBOL											WAVEFORMS
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	-40 to +125		V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/ tPLH	propagation delay nA, nB, nC to nY		14	24		30		36	ns	4.5	Fig. 6
t _{THL} /	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

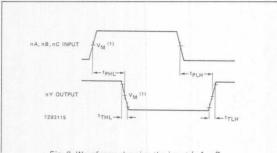


Fig. 6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

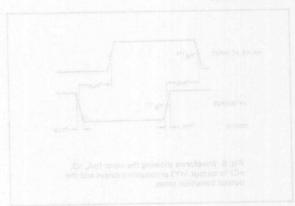
Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

AC CHARACTERISTICS FOR TAHOT

GND = 0 V; ti = 1; = 6 ns; Ci = 60 of

AC WAVEFORMS



lote to AC yeavatorms

BCT1 VM = 1.3 V; VI = GND to V CO.

TRIPLE 3-INPUT AND GATE

FEATURES

Output capability: standard

· ICC category: SSI

GENERAL DESCRIPTION

The 74HC/HCT11 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT11 provide the 3-input AND function.

		ACMIDITIONS.	TYF	UNIT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNII
tPHL/ tPLH	propagation delay nA, nB, nC to nY	C _L = 15 pF V _{CC} = 5 V	10	11	ns
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	18	20	pF

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x VCC^2 x f₁ + Σ (CL x VCC^2 x f₀) where:

f; = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

 f_0 = output frequency in MHz Σ (C_L × V_{CC}² × f_0) = sum of outputs

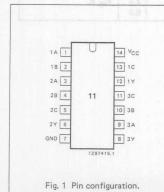
2. For HCT the condition is VI = GND to VCC
For HCT the condition is VI = GND to VCC - 1.5 V

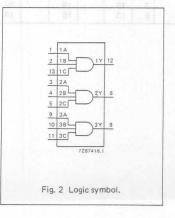
PACKAGE OUTLINES

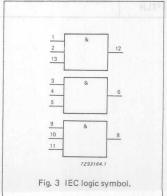
14-lead DIL; plastic (SOT27)

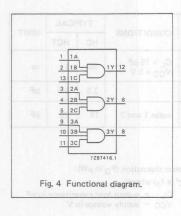
14-lead mini pack; plastic (SO14; SOT108A)

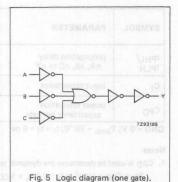
	PIN NO.	SYMBOL	NAME AND FUNCTION
	1, 3, 9 2, 4, 10	1A to 3A 1B to 3B	data inputs data inputs
	7	GND	ground (0 V)
30	12, 6, 8	1Y to 3Y	data outputs
-	13, 5, 11	1C to 3C	data inputs
1	14	Vcc	positive supply voltage











FUNCTION TABLE

	INPUTS		OUTPUT
nA	nB	nC	nY
L	1	1	GENERALLI
L			The TANCINCT
L			School State
LAbla			comparight with
			riw sortal times
H	skit sit	WOH IT	The 74LC/HC
Н	Н	nLitoni	t GM/Lrugal-S
H	Н	Н	Н

H = HIGH voltage level L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications"

Output capability: standard I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

SYMBOL	AND ERNOTION	BIMAN	Tamb (°C)						TEST CONDITIONS		
	PARAMETER (V 0)	A& 74HC 8,8,1						UNIT	\/	WAVEFORMS	
		+25			-40 to +85		-40 to +125		UNII	V _{CC}	WAVEFORING
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/ tPLH	propagation delay nA, nB, nC to nY		32 12 10	100 20 17	0a ⁹	125 25 21	5, 11	150 30 26	ns	2.0 4.5 6.0	Fig. 6
t _{THL} /	output transition times		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD
nA, nB, nC	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

SYMBOL 4	V ₁ = GND to V _{GD}		12mh (C)								TEST CONDITIONS	
	PARAMETER										WAVEFORMS	
	PARAMETER	+25		-40 to +85		-40 to +125		UNIT	V CC	WAVEIONWS		
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/ tPLH	propagation delay nA, nB, nC to nY		16	24		30		36	ns	4.5	Fig. 6	
tTHL/ tTLH	output transition times		7	15		19		22	ns	4.5	Fig. 6	

AC WAVEFORMS

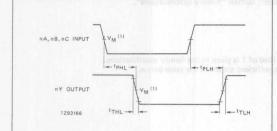


Fig. 6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

CORP. HOT GOLLSING COMMANU JU

Output capability: standard for category: SSI. Note to HCT types The value of additional quascent supply

INPUT UNIT LOAD

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX INVERTING SCHMITT TRIGGER

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT14 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT14 provide six inverting buffers with Schmitt-trigger action. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

SYMBOL	PARAMETER	CONDITIONS	TYF	UNIT	
		CONDITIONS	НС	нст	ONT
tPHL/	propagation delay nA to nY	C _L = 15 pF V _{CC} = 5 V	12	17	ns
CI	input capacitance	The state of	3.5	3.5	pF
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	7	8	pF

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

PD = CPD x VCC² x f_i +
$$\Sigma$$
 (CL x VCC² x f_o) where:

f; = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

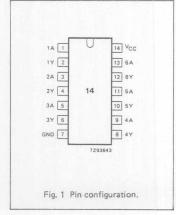
PACKAGE OUTLINES

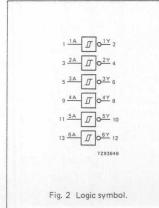
14-lead DIL; plastic (SOT27)

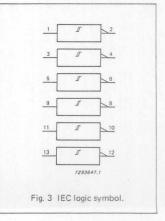
14-lead mini pack; plastic (SO14; SOT108A)



PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13 2, 4, 6, 8, 10, 12		data inputs data outputs strengt (0.00)
14	VCC	ground (0 V) positive supply voltage







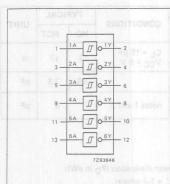


Fig. 4 Functional diagram.

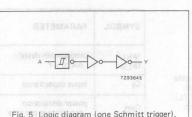
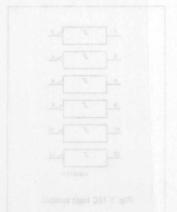


Fig. 5 Logic diagram (one Schmitt trigger).

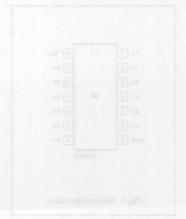
INPUT	OUTPUT
nA	nY
L	Н
Н	L

H = HIGH voltage level L = LOW voltage level

APPLICATIONS		11 0 0 5 1
Wave and pulse shapers		
 Astable multivibrators Monostable multivibrators 		







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard I_{CC} category: SSI

Transfer characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

					T _{amb} (°C)				TEST CONDITIONS		
SYMBOL	PARAMETER				74H	С	UNIT	V				
STINIBUL FA	PANAMETER	+25				UNIT	VCC	WAVEFORMS				
		min.	typ.	max.	min.	max.	min.	max.	- 10	HAPE 1		
V _{T+} _{avoi}	positive-going threshold	0.7 1.7 2.1	1.18 2.38 3.14	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	V bnuc	2.0 4.5 6.0	Figs 6 and 7	
V _T _	negative-going threshold	0.3 0.9 1.2	0.52 1.40 1.89	0,90 2.00 2.60	0.3 0.90 1.20	0.90 2.00 2.60	0.30 0.90 1.2	0.90 2.00 2.60	V	2.0 4.5 6.0	Figs 6 and 7	
VH	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.4 0.6	0.66 0.98 1.25	1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	٧	2.0 4.5 6.0	Figs 6 and 7	

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	6.5 Figs 6 and 7			0.4	T _{amb} (°C)	- 08	0,4 0.		TEST CONDITIONS		
SYMBOL	PARAMETER		74HC									
	PLOTE OF THE STATE	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.	1.41			
tPHL/	propagation delay nA to nY	10	41 15 12	125 25 21	TOP	155 31 26	20	190 38 32	ns	2.0 4.5 6.0	Fig. 8	
tTHL/ tTLH	output transition time	330	19 7 6	75 15 13	on .ni	95 19 16	un Lq	110 22 19	ns	2.0 4.5 6.0	Fig. 8	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard ICC category: SSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA	0.3 EVAIN -

Transfer characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

	6.0	2		2	T _{amb} (°C)			Di	TEST CONDITIONS		
	2.0		000 00.0 0074HCT 000 02.0 8.0									
SYMBOL	PARAMETER 3.A	+25		-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS		
	2.0 Figs 5 and 7	min.	typ.	max.	min.	max.	min.	max.		V	V) Standard LV	
V _{T+}	positive-going threshold	1.2	1.41 1.59	1.9 2.1	1.2 1.4	1.9	1.2 1.4	1.9	V	4.5 5.5	Figs 6 and 7	
V _T _	negative-going threshold	0.5 0.6	0.85 0.99	1.2 1.4	0.5 0.6	1.2 1.4	0.5	1.2	V	4.5 5.5	Figs 6 and 7	
AH SMOH	hysteresis (V _{T+} - V _{T-})	0.4	0.56 0.60	-	0.4		0.4 0.4	_	V	4.5 5.5	Figs 6 and 7	

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

		1 -500	- 20	11 08	T _{amb} (°C)	100	23 - 28500			TEST CONDITIONS
SYMBOL	PARAMETER	74HCT	WAVEFORMS								
STIVIBUL	+25 -40 to +85 -40 to +13	o +125	UNIT		WAVEFORMS						
		min.	typ.	max.	min.	max.	min.	max.	9	nit noit	
t _{PHL} /	propagation delay nA to nY		20	34		43		51	ns	4.5	Fig. 8
t _{THL} /	output transition time		7	15		19		22	ns	4.5	Fig. 8

TRANSFER CHARACTERISTIC WAVEFORMS

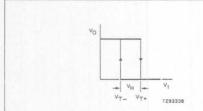


Fig. 6 Transfer characteristic.

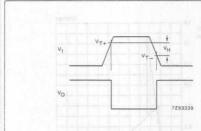


Fig. 7 Waveforms showing the definition of V_{T+}, V_T $_{-}$ and V_H; where V_{T+} and V_T $_{-}$ are between limits of 20% and 70%.

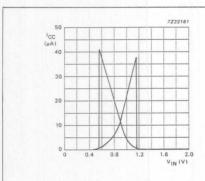


Fig. 8 Typical HC transfer characteristics; V_{CC} = 2 V.

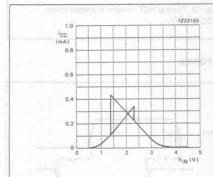


Fig. 9 Typical HC transfer characteristics; V_{CC} = 4.5 V.

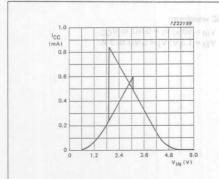


Fig. 10 Typical HC transfer characteristics; $V_{CC} = 6 \text{ V}$.

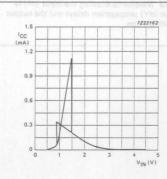


Fig. 11 Typical HCT transfer characteristics; $V_{CC} = 4.5 \text{ V}.$

TRANSFER CHARACTERISTIC WAVEFORMS (Cont'd)

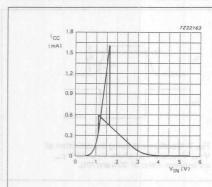


Fig. 12 Typical HCT transfer characteristics; $V_{CC} = 5.5 \text{ V}$.

AC WAVEFORMS

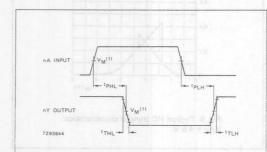
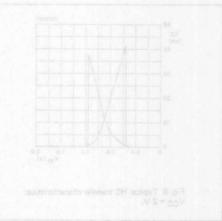
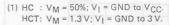


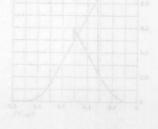
Fig. 13 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.











APPLICATION INFORMATION

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

 P_{ad} = additional power dissipation (μ W) f_1 = input frequency (MHz)

= input rise time (µs); 10% - 90%

= input fall time (μs); 10% — 90%

ICCa = average additional supply current (μA)

Average $I_{\mbox{\scriptsize CCa}}$ differs with positive or negative input transitions, as shown in Figs 14 and 15.

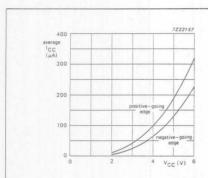


Fig. 14 Average I $_{\rm CC}$ for HC Schmitt trigger devices; linear change of V $_{\rm i}$ between 0.1 V $_{\rm CC}$ to 0.9 V $_{\rm CC}.$

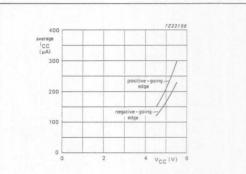


Fig. 15 Average I $_{\rm CC}$ for HCT Schmitt trigger devices; linear change of V $_{\rm i}$ between 0.1 V $_{\rm CC}$ to 0.9 V $_{\rm CC}$.

HC/HCT14 used in a relaxation oscillator circuit, see Fig. 16.

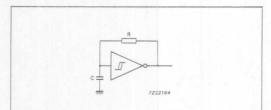


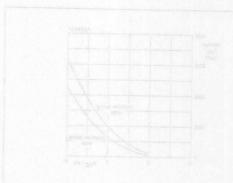
Fig. 16 Relaxation oscillator using HC/HCT14.

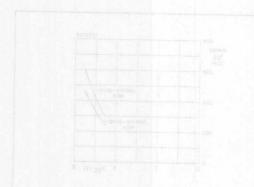
$$HC : f = \frac{1}{T} \approx \frac{1}{0.8 RC}$$

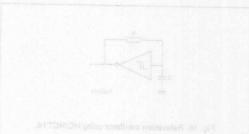
HCT:
$$f = \frac{1}{T} \approx \frac{1}{0.67 \text{ BC}}$$

Note to Application information

All values given are typical unless otherwise specified.







DUAL 4-INPUT NAND GATE

FEATURES

- Output capability: standard
- Icc category: SSI

GENERAL DESCRIPTION

The 74HC/HCT20 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT20 provide the 4-input NAND function.

			TYF	LINUT	
SYMBOL	PARAMETER	CONDITIONS	нс	НСТ	UNIT
tPHL/	propagation delay nA, nB, nC, nD to nY	C _L = 15 pF V _{CC} = 5 V	8	13	ns
C ₁	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	22	17	pF

$$GND = 0 \text{ V; } T_{amb} = 25 \,^{\circ}\text{C; } t_r = t_f = 6 \text{ ns}$$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

fi = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

 f_0 = output frequency in MHz $\Sigma (C_L \times V_{CC}^2 \times f_0)$ = sum of outputs

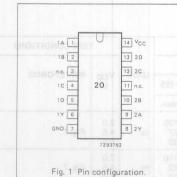
2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

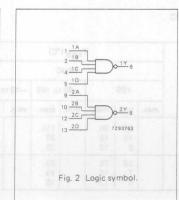
PACKAGE OUTLINES

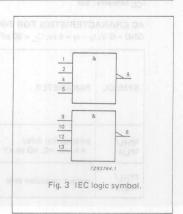
14-lead DIL; plastic (SOT27)

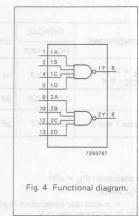
14-lead mini pack; plastic (SO14; SOT108A)

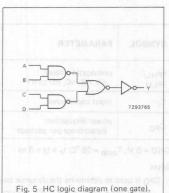
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1A, 2A	data inputs
2, 10	1B, 2B	data inputs
3, 11	n.c.	not connected
4, 12	1C, 2C	data inputs
5, 13	1D, 2D	data inputs
6, 8	1Y, 2Y	data outputs
7	GND	ground (0 V)
14	Vcc	positive supply voltage

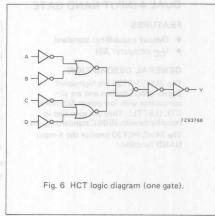












		INP	UTS		OUTPUT
	nA	nB	nC	nD	nY
	L	X	X	X	Н
	X	L	X	X	Н
1	X	X	L	X	Н
1	X	X	X	0.413	Haraus
1	Н	Н	Н	Н	L

H = HIGH voltage level

L = LOW voltage level

X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

			T _{amb} (°C)							TEST CONDITIONS	
CYMPOL	DADAMETED									.,	
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			8 01
tPHL/	propagation delay nA, nB, nC, nD to nY		28 10 8	90 18 15	05 p	115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 7
t _{THL} /	output transition time		19 7 6	75 15 13	S .gii	95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC, nD	0.3

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		T _{amb} (°C)								TEST CONDITIONS	
SYMBOL	242445752		74HCT								WAVEFORMS
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORWS
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} /	propagation delay nA, nB, nC, nD to nY		16	28		35		42	ns	4.5	Fig. 7
t _{THL} /	output transition time		7	15		19		22	ns	4.5	Fig. 7

AC WAVEFORMS

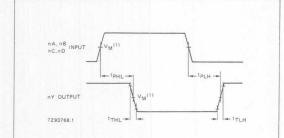


Fig. 7 Waveforms showing the enable input (nA, nB, nC, nD) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

DC CHARACTERISTICS FOR 74HC7

For the DC characteristics see chaoter "HDMOS family characteristics", section "Family specifications"

Output capability: standard for category: \$51

Note to HCT type

The value of additional quiescent supply current (AICC) for a unit load of 1 is given in the family specifications. Fo determine AICC per input, multiply this value by the unit load quafficient shown in the table below.

AC CHARACTERISTICS FOR 74HCT

GND = 0 VI t. # 14 = 6 ns: CI = 50 pF

ACTRIAVEFORMS

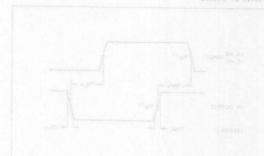


Fig. 7. Waveforms showing the enable input InA, nB, nC, nD) to output In(Y) propagation delays and the output resisting times.

emitorewe JA or ero

HCT: VM = 1.3 V; VI = GND to 3 V.

DUAL 4-INPUT AND GATE

FEATURES

- · Output capability: standard
- ICC category: SSI

GENERAL DESCRIPTION

The 74HC/HCT21 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT21 provide the 4-input AND function.

averana.	DADAMETER	CONDITIONS	TYF	UNIT	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
tPHL/ tPLH	propagation delay nA, nB, nC, nD to nY	C _L = 15 pF V _{CC} = 5 V	10	12	ns
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	15	16	pF

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

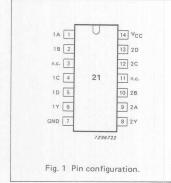
PD = CPD x
$$VCC^2$$
 x f; + Σ (CL x VCC^2 x f₀) where:

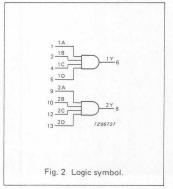
- fi = input frequency in MHz
- CL = output load capacitance in pF VCC · = supply voltage in V
- f_0 = output frequency in MHz Σ (C_L × V_{CC}² × f_0) = sum of outputs
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

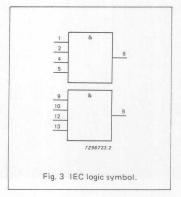
PACKAGE OUTLINES

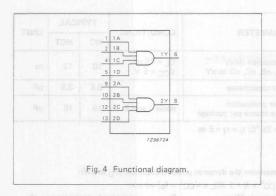
- 14-lead DIL; plastic (SOT27)
- 14-lead mini pack; plastic (SO14; SOT108A)

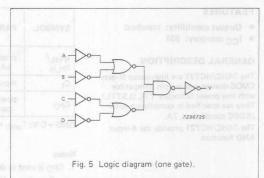
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9 2, 10	1A, 2A 1B, 2B	data inputs data inputs data inputs
3, 11	n.c.	not connected
4, 12	1C, 2C	data inputs
5, 13	1D, 2D	data inputs
6, 8	1Y, 2Y	data outputs
7	GND	ground (0 V)
14	Vcc	positive supply voltage







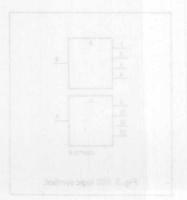




	INP	UTS		OUTPUT
nA	nB	nC	nD	nY
L	X	X	X	L
X X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
Н	Н	Н	Н	Н

ACKAGE OD FERRES Fleet mini peck; plenic (8014; 807108A)

H = HIGH voltage level	NAME AND FUNCTED	
L = LOW voltage level X = don't care		
A - don t care		







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: SSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	PARAMETER DOV of QND = N				T _{amb} (°C)				TEST CONDITIONS	
SYMBOL			74HC or (dn. On. 8n. A								- We sounded W. 8 SP
		208 = +25 OH (-40 to +85 -		-40 to +125		UNIT	VCC	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		en pure bilar	
tPHL/	propagation delay nA, nB, nC, nD to nY		33 12 10	110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 6
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB,	1.50
nC, nD	1.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	PARAMETER				T _{amb} (TEST CONDITIONS					
SYMBOL					74HC	т	UNIT	V	WAVEFORMS			
SYMBOL		+25			-40 to +85		-40 to +125		ONT	V _{CC}	WAVEFORIUS	
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay nA, nB, nC, nD to nY		15	27		34		41	ns	4.5	Fig. 6	
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6	



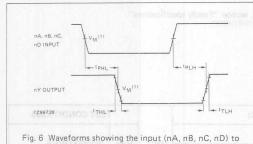


Fig. 6 Waveforms showing the input (nA, nB, nC, nD) to output (nY) propagation delays and the output transition times.

OCCUPATION FOR YANG

Output espainity: standard

AC CHARACTERISTICS FOR 74HC

GND = 0 V; q = tr = 6 ns: Ct = 60 pF

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

DC CHARACTERISTICS FOR TANCT

Dutput capability: srandard

most TOH of stoll

The value of additional quiedcent supply current (A (cg) for a unit load of it is given in the family specifications. To determine A (cm are input, multiply this value by the unit load coefficient shown in the table below.

AC CHARACTERISTICS FOR 741CT

TRIPLE 3-INPUT NOR GATE

Output capability: standard

I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT27 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT27 provide the 3-input NOR function.

SYMBOL	DADAMETED	CONDITIONS	TYF	UNIT	
	PARAMETER	CONDITIONS	НС	нст	OIAII
t _{PHL} /	propagation delay nA, nB, nC to nY	C _L = 15 pF V _{CC} = 5 V	8	10	ns
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	24	30	pF

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

 $PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$ where:

f; = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

 f_0 = output frequency in MHz Σ (C_L × V_{CC}² × f_0) = sum of outputs

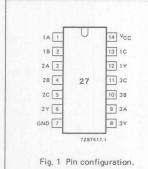
2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

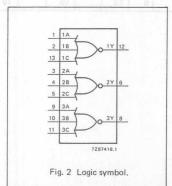
PACKAGE OUTLINES

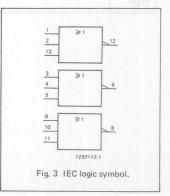
14-lead DIL; plastic (SOT27).

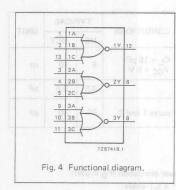
14-lead mini-pack; plastic (SO14; SOT108A).

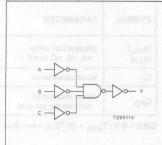
PIN NO.	SYMBOL	NAME AND FUNCTION	
1, 3, 9	1A to 3A	data inputs	CSINAS
2, 4, 10	1B to 3B	data inputs	
13, 5, 11	1C to 3C	data inputs	
7 an.	GND 98	ground (0 V)	
12, 6, 8	1Y to 3Y	data outputs	
14	Vcc	positive supply voltage	











	INPUTS	ory: SS	OUTPUT
nA	nB	nC	nY
L 18	ngstrigiri	T2Z]are	пе инсин
X	X	Hubb	BORTO Ling-R
X	oweHSet	X	w sidist gmps
Hilbri	X	X	TTL LISTTE

H = HIGH voltage level

L = LOW voltage level X = don't care

Fig. 5 Logic diagram (one gate).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: SSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)	N DES	19		TEST CONDITIONS		
SYMBOL	AND PUNCTION	A 3MAW	JOSE 74HC .OM MIS						UNIT	V	WAVEFORMS	
		qni ibab	+25 AT		-40 to +85		-40 to +125		OWIT	V _{CC}	WAVEFORIVIS	
	434	min.	typ.	max.	min.	max.	min.	max.				
tPHL/ tPLH	propagation delay	ground i cara loud orginae	28 10 8	90 18 15		115 23 20	2 8 8	135 27 23	ns	2.0 4.5 6.0	Fig. 6	
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD
nA, nB, nC	1.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

					T _{amb} (°C)		TEST CONDITIONS			
SYMBOL	PARAMETER				74HC	т	UNIT	Vcc	WAVEFORMS		
		+25			-40 to +85		-40 to +125		ONT	V	WAVELORWIS
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/	propagation delay nA, nB, nC to nY		12	21		26		32	ns	4.5	Fig. 6
tTHL/	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

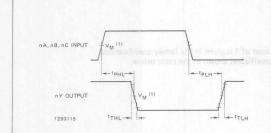


Fig. 6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

The value of additional quiescent supply current $(\Delta \log_C)$ for a unit To determine $\Delta \log_C$ per input, multiply this value by the unit load

Note to AC waveforms

(1) HC : $V_{M} = 50\%$; $V_{I} = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to 3 V}$.

8-INPUT NAND GATE

FEATURES

- · Output capability: standard
- Icc category: SSI

GENERAL DESCRIPTION

The 74HC/HCT30 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT30 provide the 8-input NAND function.

SYMBOL	DADAMETER	CONDITIONS	TYF	UNIT		
SAMBOL	PARAMETER	CONDITIONS	нс	нст	OWIT	
t _{PHL} /	propagation delay A, B, C, D, E, F, G, H to Y	C _L = 15 pF V _{CC} = 5 V	12	12	ns	
CI	input capacitance		3.5	3.5	pF	
CPD	power dissipation capacitance per gate	notes 1 and 2	15	15	pF	

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

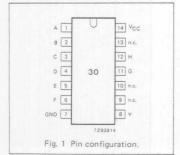
- 1. CPD is used to determine the dynamic power dissipation (PD in μ W):
 - $PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$ where:
 - CL = output load capacitance in pF VCC = supply voltage in V f; = input frequency in MHz
 - fo = output frequency in MHz
 - $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} -1.5 V -1.5 V

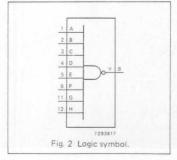
PACKAGE OUTLINES

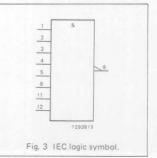
14-lead DIL: plastic (SOT27).

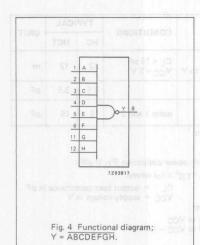
14-lead mini-pack; plastic (SO14; SOT108A).

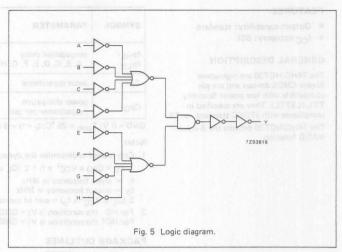
PIN NO.	SYMBOL	NAME AND FU	NC.	ПО	N					
1	A	data input	X	X	X	X	×	X	×	X
2	В	data input								
3	С	data input								
4	D	data input								
5	E	data input								
6	F	data input								
7	GND	ground (0 V)								
8	Y	data output								
9, 10, 13	n.c.	not connected								
11	G	data input								
12	Н	data input								
14	Vcc	positive supply v	olta	ge						









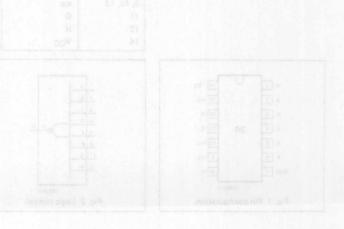


		- 1	NP	JTS				OUTPUT
А	В	С	D	E	F	G	н	Υ
L	X	X	X	X	X	X	X	Н
X	L	X	X	X	X	X	X	Н
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	Н
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	Н
Н	н	Н	Н	н	Н	Н	Н	FIL DIS

H = HIGH voltage level

L = LOW voltage level

X = don't care



DC CHARACTERISTICS FOR 74 HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_{\Gamma} = t_{f} = 6 \text{ ns}$; $C_{L} = 50 \text{ pF}$

					T _{amb} (°C)		The same	TEST CONDITIONS			
SYMBOL	DADAMETED	74HC										
STIVIBUL	MBOL PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/ tPLH	propagation delay A, B, C, D, E, F, G, H to Y		41 15 12	130 26 22		165 33 28	B G ,S tine our	195 39 33	ab mais ns	2.0 4.5 6.0	Fig. 6	
t _{THL} /	output transition time	en:	19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: SSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

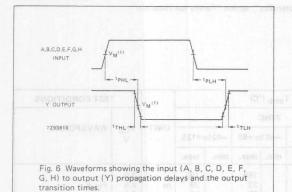
-	INPUT	UNIT LOAD COEFFICIENT
	A, B, C, D, E, F, G, H	0.60

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

			T _{amb} (°C)							TEST CONDITIONS		
CVMDOL	DADAMETER	74HCT								Van	WAVEFORMS	
SYMBOL PARAMETER	+25			-40 to +85 -40		-40 to +125		UNIT	VCC	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay A, B, C, D, E, F, G, H to Y		16	28		35		42	ns	4.5	Fig. 6	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 6	

AC WAVEFORMS



OC CHARACTERISTICS FOR 74 HC

Output depolitry: standard LCC category: 881

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $x_i = x_i = 6$ ns; $C_{i,j} = 60$ pF

85+ KBM UV7 JOHAN

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

poil transition rime

CHARACTERISTICS FOR TANCT

Disposes synilidades rugard

Mate to HCT types

The value of additional quiescent supply coment (A Ipp.) for a unit load of 1 is given in the family specificated.

To extermine other than multiply this value by the unit load coefficient shown in the fable celow.

	TURNI

AC CHARACTERISTICS FOR 74HCT

GND = 0 V: T = T = 6 m; CL = 50 pF

QUAD 2-INPUT OR GATE

FEATURES

- Output capability: standard
- · ICC category: SSI

GENERAL DESCRIPTION

The 74HC/HCT32 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT32 provide the 2-input OR function.

CVMDOI	FUNCTION TABLE	CONDITIONS	TYF	UNIT	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	
tPHL/ tPLH	propagation delay nA, nB to nY	C _L = 15 pF V _{CC} = 5 V	6	9	ns
CI	input capacitance	THE C	3.5	3.5	pF
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	16	28	pF

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

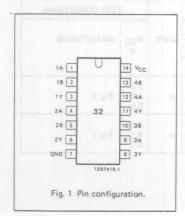
$$P_D = C_{PD} \times V_{CC}^2 \times f_1 + \Sigma (C_L \times V_{CC}^2 \times f_0)$$
 where:

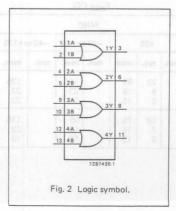
- fi = input frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V
- fo = output frequency in MHz
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

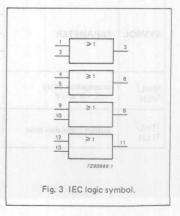
PACKAGE OUTLINES

- 14-lead DIL; plastic (SOT27).
- 14-lead mini-pack; plastic (SO14; SOT108A).

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	Vcc	positive supply voltage







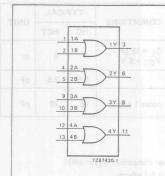


Fig. 4 Functional diagram.

INP	UTS	OUTPUT
100000000000000000000000000000000000000	nB	nY
Timo	Pan An	14 145
Long	Here	H
H	L	Н
Н	Н	H

H = HIGH voltage level L = LOW voltage level

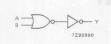


Fig. 5 Logic diagram 74HC (one gate).

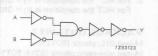


Fig. 6 Logic diagram 74HCT (one gate).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: SSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

		1	T _{amb} (°C)								TEST CONDITIONS			
SYMBOL	PARAMETER				74H	UNIT	\/	WAVEFORMS						
STIVIBOL			+25		-40	to +85	-40 t	o +125	DIVIT	V _{CC}	WAVE	ORIVIS		
	min.	typ.	max.	min.	max.	min.	max.		14 Yes					
^t PHL [/] ^t PLH	propagation delay nA, nB to nY		22 8 6	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 7	S 87 E VI		
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7	2 85		

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: SSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD
nA, nB	1.20

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	= GND to SV.	V;VE	VIVER H MV TON Tamb (°C)								TEST CONDITIONS	
SYMBOL	PARAMETER		74НСТ									
TANAMETER	+25			-40 to +85 -		-40 to +125		UNIT	Vcc	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/ tPLH	propagation delay nA, nB to nY		11	24		30		36	ns	4.5	Fig. 7	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 7	

AC WAVEFORMS

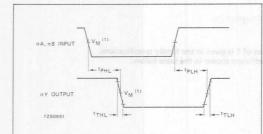


Fig. 7 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_1 = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_1 = GND$ to 3 V.

BCD TO DECIMAL DECODER (1-OF-10)

FEATURES

- Mutually exclusive outputs
- 1-of-8 demultiplexing capability
- Outputs disabled for input codes above nine
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT42 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT42 decoders accept four active HIGH BCD inputs and provide 10 mutually exclusive active LOW outputs. The active LOW outputs facilitate addressing other MSI circuits with active LOW input enables.

The logic design of the "42" ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input (A₃) produces a useful inhibit function when the "42" is used as a 1-of-8 decoder. The A3 input can also be used as the data input in an 8-output demultiplexer application.

01/140		BARAT WORLDWOG	CONDITIONS	TYF	LIBILT	
SYMB	OL	PARAMETER	CONDITIONS	нс	нст	UNIT
tPHL/	OY 1	propagation delay A _n to \overline{Y}_n	C _L = 15 pF V _{CC} = 5 V	14	17	ns
CI	185	input capacitance	1-1-0	3.5	3.5	pF
CPD	H	power dissipation capacitance per package	notes 1 and 2	37	37	pF

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

Notes

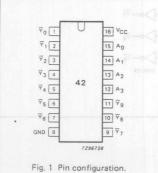
- 1. CPD is used to determine the dynamic power dissipation (PD in μ W):
 - PD = CPD x VCC^2 x f_i + Σ (CL x VCC^2 x f_o) where:
 - f; = input frequency in MHz fo = output frequency in MHz
- CL = output load capacitance in pF
- VCC = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is VI = GND to VCC
- For HCT the condition is $V_I = GND$ to $V_{CC} 1.5 V$

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 9, 10, 11	\overline{Y}_0 to \overline{Y}_9	multiplexer outputs
8	GND	ground (0 V)
15, 14, 13, 12	A ₀ to A ₃	data inputs
16	Vcc	positive supply voltage



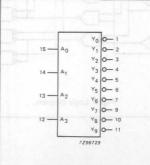
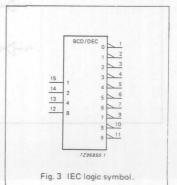
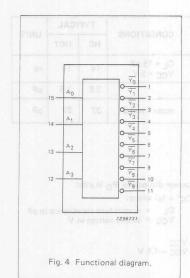


Fig. 2 Logic symbol.



SCD TO DECIMAL DECODER (1-05-10)



FUNCTION TABLE

	INP	UTS						OUT	PUTS				
А3	A ₂	A ₁	A ₀	₹0	₹1	₹2	₹3	₹4	₹5	₹6	₹7	₹8	Y
L	L	nL o	oB.	L	H	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	H
L	L	Н	L	Н	H	L	Н	Н	Н	H	H	HOO	H
L	ahse	Н	Н	Н	H	Н	L	Н	Н	Н	Н	Н	Н
L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
[] =	H	PLAS	H	H	H	Н	Н	Н	L	Н	Н	Н	Н
L	H	Н	L	Н	Н	Н	Н	Н	H	L	Н	Н	H
L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н
Н	L	L	L	Н	Histor	ИН	н	Н	Н	Н	Н	opailo	Н
Н	L	L	H	Н	-Ho	H	Н	H	Н	H	HH	CHAN	L
Н	L	Н	L	Н	Н	Н	Hivo	Hins	Hadi	CHD8	HHH	H	H
Н	L	Н	Н	Н	Н	Н	al H qm	OHO.	H	Н	Н	Н	Н
Н	Н	AFiliah		Н	Н	Н	HWID	Н	Hus	Н	Н	Н	Н
Н	H	EE lo	Ho	H×	H	Н	Н	Н	Н	H -86	H	Н	H
H	-HV	Н	oLo e	HO	Н	SH	H	Н	H	Н	H	H	Н
H	H	H	пНа в	H	H	Н	H	Н	Н	H	Н	Н	Н

H = HIGH voltage level
L = LOW voltage level

MOITOMA SMAA

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_1 = 50 pF$

					T _{amb} (°C)	- 1		100	TEST CONDITIONS		
	DADAMETER	74HC								1	WAVEFORMS	
SYMBOL	SYMBOL PARAMETER	+25			-40	-40 to +85 -40 to		0 to +125		V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.	AT Jugai	arts print	Fig. If Wavetoms snow	
tPHL/	propagation delay A_n to \overline{Y}_n	WE.I =	47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6	
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
An	1.0

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		T _{amb} (°C) 74HCT								Т	EST CONDITIONS
SYMBOL	PARAMETER									Vac	WAVEFORMS
STINBUL	IBOL PARAMETER	+25			-40 to +85 -40 to		10 to +125		V _{CC}	WAVEFORWS	
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/ tPLH	propagation delay A_n to \overline{Y}_n		20	35		44		53	ns	4.5	Fig. 6
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

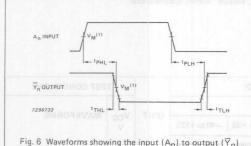


Fig. 6 Waveforms showing the input (A_n) to output $(\overline{\mathsf{Y}}_n)$ propagation delays and the output transition times.

Note to AC waveforms

(1) HC : VM = 50%; VI = GND to VCC. HCT: $V_M = 1.3 V$; $V_I = GND to 3 V$.

DUAL AND-OR GATE

FEATURES

gate.

- Output capability: standard
- ICC category: SSI

GENERAL DESCRIPTION

The 74HC58 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A. The "58" provides two sections of AND-OR gates. One section contains a 2-wide, 3-input (1A to 1F) AND-OR gate and the second section contains a 2-wide, 2-input (2A to 2D) AND-OR

		001101710110	TYPICAL	LIBILT
SYMBOL	PARAMETER	CONDITIONS	НС	- UNIT
^t PHL [/] ^t PLH	propagation delay 1n to 1Y 2n to 2Y	C _L = 15 pF V _{CC} = 5 V	11 9	ns ns
CI	input capacitance	1 20161	3.5	pF
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	18	pF

GND = 0 V; T_{amb} = 15 °C; t_r = t_f = 6 ns

Notes.

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

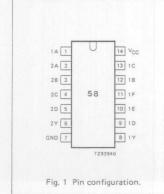
- fi = input frequency in MHz CL = output load capacitance in pF
- VCC = supply voltage in V fo = output frequency in MHz
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is VI = GND to VCC

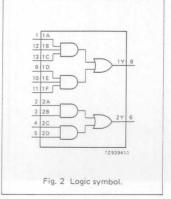
PACKAGE OUTLINES

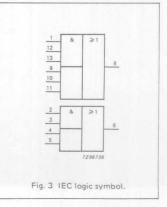
14-lead DIL; plastic (SOT27).

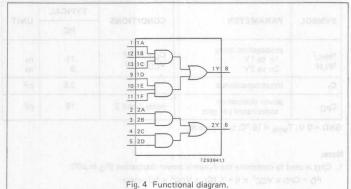
14-lead mini-pack; plastic (SO14; SOT108A).

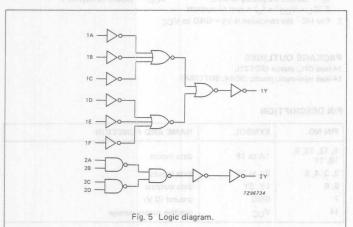
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 12, 13, 9, 10, 11	1A to 1F	data inputs
2, 3, 4, 5	2A to 2D	data inputs
8, 6	1Y, 2Y	data outputs
7	GND	ground (0 V)
14	VCC	positive supply voltage









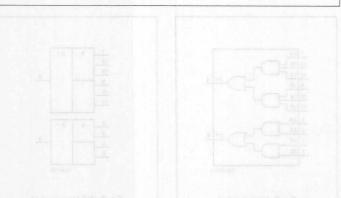


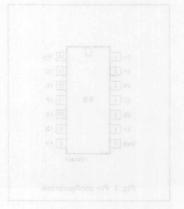
	GIL	OUTPUT				
1A	1B	1C	1D	1E	1F	1Y
L	X	X	L	X	X	CENERA
L	X	X	X	L	X	ough am
L	X	X	X	X	L	L
X	L	X	L	X	X	L
X	L	X	X	L	X	L
X	L	X	X	X	L	complianc
X.	X	Fire	FON	X	X	1,89 au
X	X	Line	X	LO	X	ROLGINA
X	X	L	X	X	L	a Z-mgde, a
X	X	X	H	H	H	A DAH STREET
H	H	H	X	X	X	H

	INP	OUTPUT		
2A	2B	2C	2D	2Y
L	X	L	X	L
L	X	X	L	L
X	L	L	X	L
X	L	X	L	L
X	X	Н	Н	Н
H	Н	X	X	Н

H = HIGH voltage level L = LOW voltage level

X = don't care





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: SSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

SYMBOL					r _{amb} (°C)				TEST CONDITIONS	
	242445772	74HC								.,	WAVEFORMS
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORINS
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} /	propagation delay 1A,1B,1C,1D,1E,1F to 1Y		36 13 10	115 23 20		145 29 25		175 35 30	ns	2.0 4.5 6.0	Fig. 6
t _{PHL} /	propagation delay 2A,2B,2C,2D to 2Y		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC WAVEFORMS

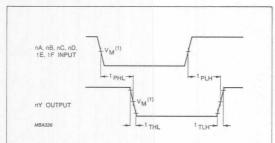


Fig. 6 Waveforms showing the input (nA, nB, nC, nD, 1E, 1F) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} .

For the DC characteristics are chapter "HOMOS family characteristics", section "Family specifications"

Output capability; standard Inc. datesory: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t, = t; = 8 ns; C; = 50 pF

AC WAVEFORMS

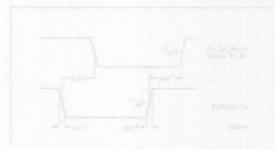


Fig. 6 Waveforms showing the input (nA. nB. nC. nD. 1E 1F) to curput (nY) propagation delays and the output (nY) propagation delays and the output specified times.

lote to AC waveforms

DUAL JK FLIP-FLOP WITH RESET; NEGATIVE-EDGE TRIGGER

FEATURES

Output capability: standard

I_{CC} category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT73 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL), They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT73 are dual negativeedge triggered JK-type flip-flops featuring individual J, K, clock (nCP) and reset (nR) inputs; also complementary Q and \overline{Q} outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset (nR) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the Q output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

		COMPUTIONS	TYF	LIBUT		
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT	
^t PHL [/] ^t PLH	propagation delay n <u>CP</u> to n <u>Q</u> n <u>CP</u> to n <u>Q</u> n <u>R</u> to n <u>Q</u>	C _L = 15 pF V _{CC} = 5 V	16 16 15	15 18 15	ns ns ns	
fmax	maximum clock frequency		77	79	MHz	
Cl	input capacitance	0 01	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	30	30	pF	

 $GND = 0 \text{ V}; T_{amb} = 25 \, ^{\circ}\text{C}; t_r = t_f = 6 \text{ ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

 $PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$ where:

fi = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

fo = output frequency in MHz

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is VI = GND to VCC For HCT the condition is VI = GND to VCC - 1.5 V

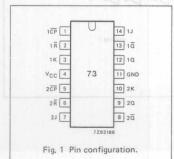
PACKAGE OUTLINES

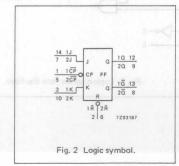
14-lead DIL; plastic (SOT27)

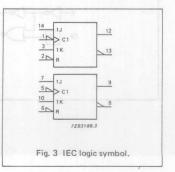
14-lead mini pack; plastic (SO14; SOT108A)

PIN DESCRIPTION

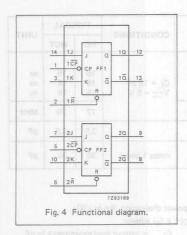
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	PIN NO.	SYMBOL	NAME AND FUNCTION
$\begin{array}{cccccccccccccccccccccccccccccccccccc$			clock input (HIGH-to-LOW, edge-triggered) asynchronous reset inputs (active LOW)
13, 8 $1\overline{Q}$, $2\overline{Q}$ complement flip-flop outputs			
	12, 9	10, 20	true flip-flop outputs
14 7 3 10 1J 2J 1K 2K synchronous inputs: flip-flops 1 and 2	13, 8	10, 20	complement flip-flop outputs
	14, 7, 3, 10	1J, 2J, 1K, 2K	synchronous inputs; flip-flops 1 and 2







. Ourput capability: standard



FUNCTION TABLE

		INPU	OUTPUTS			
OPERATING MODE	ηR	nCP	ooy o	K	Q	ā
asynchronous reset	L	X	X	X	L	Н
toggle	н	+	h	h	q	q
load "O" (reset)	Н	1	1	h	S SE	H
load "1" (set)	Н	1	h	1	Н	L
hold "no change"	Н	1	- 1	1	q	q

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition

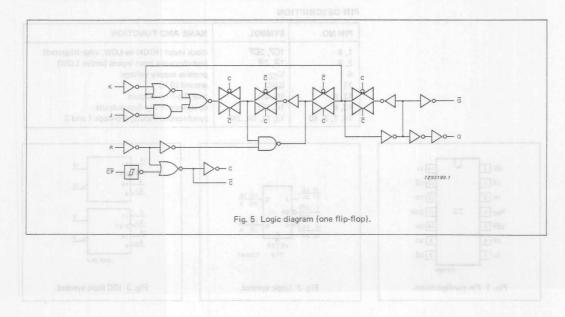
L = LOW voltage level

I = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition

X = don't care

↓ = HIGH-to-LOW CP transition



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: flip-flops

AC CHARACTERISTICS FOR 74HC at any manager at the book manager to be a second and a

GND =0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

					T _{amb} (°C)				TV	TEST CONDITIONS	
		17.75			74H	С						
SYMBOL	PARAMETER		+25		-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
^t PHL [/]	propagation delay		52 19 15	160 32 27		200 40 34		240 48 41	ns _{Rg O}	2.0 4.5 6.0	Fig. 6 , = ,t.iV 0 = QM	
t _{PHL} /	propagation delay		52 19 15	160 32 27	OT em	200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} /	propagation delay	+128 max.	50 18 14	145 29 25	of Ob-	180 36 31	-25 typ.	220 44 38	ns	2.0 4.5 6.0	Fig. 7	
tTHL/ tTLH	output transition time	57 n	19 7 6	75 15 13		95 19 16	87	110 22 19	ns	2.0 4.5 6.0	Fig. 6	
tW	clock pulse width HIGH or LOW	80 16 14	22 8 6	5	100 20 17	20	120 24 20		ns	2.0 4.5 6.0	Fig. 6	
tw	reset pulse width HIGH or LOW	80 16 14	22 8 6	6	100 20 17	8	120 24 20		ns am	2.0 4.5 6.0	Fig. 7	
^t rem	removal time nR to nCP	80 16 14	22 8 6		100 20 17		120 24 20	ar	ns	2.0 4.5 6.0	Fig. 7	
^t su	set-up time nJ, nK to nCP	80 16 14	22 8 6		100 20 17		120 24 20	ar ar	ns	2.0 4.5 6.0	Fig. 6	
^t h	hold time nJ, nK to nCP	3 3 3	-8 -3 -2		3 3 3		3 3 3	12	ns	2.0 4.5 6.0	Fig. 6	
f _{max}	maximum clock pulse frequency	6.0 30 35	23 70 83		4.8 24 28		4.0 20 24	3	MHz	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: flip-flops

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD
nK	0.60
nR	0.65
nCP, nJ	1.00

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

	1 0.6		10										13-217
			240		00	T _{amb} (°C)	53				TEST CONDITIO	NS
SYMBOL	PARAMETER		15h		0	74 H	СТ	re er		UNIT	VCC	WAVEFORMS	
OTWIDOL			220	+25	08	-40	to +85	-40 t	o +125		V		
	4,5 Fig. 7 8.0	ns 4,5 Fig. 7	min.	typ.	max.	min.	max.	min.	max.			propagation ,Ωn to nΩ,	HJF
t _{PHL} /	propagation delay	2ft	110	18	38	9	48	19	57	ns	4.5	Fig. 6	UHT
tPHL/	propagation delay		81	21	36		45	22	54	ns	4.5	Fig. 6	
tPHL/ tPLH	propagation delay			20	34	7	43	8	51	ns	4.5	Fig. 7	18
t _{THL} /	output transition	time an		7	15	00	19	9	22	ns	4.5	Fig. 6	W
tw	clock pulse width HIGH or LOW	30	16	8 115		20		24	80 16	ns	4.5	Fig. 6	Other
tW	reset pulse width HIGH or LOW		18	9		23		27	68	ns	4.5	Fig. 7	
t _{rem}	removal time	1023	14	8		18		21	14	ns	4.5	Fig. 7	- 10
t _{su}	set-up time nJ, nK to nCP	an an	12	6		15		18	8 6	ns	4.5	Fig. 6	
th	hold time nJ, nK to nCP	sHM	3	-2		3 8		3 50	0:0	ns	4.5	Fig. 6	***
f _{max}	maximum clock p	ulse	30	72		24		20] 86	MHz	4.5	Fig. 6	

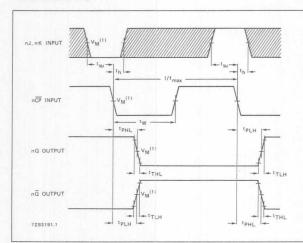


Fig. 6 Waveforms showing the clock ($n\overline{CP}$) to output (nQ, $n\overline{Q}$) propagation delays, the clock pulse width, the J and K to $n\overline{CP}$ set-up and hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

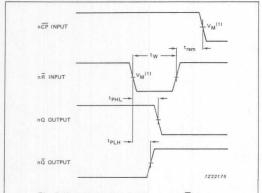


Fig. 7 Waveforms showing the reset $(n\overline{R})$ input to output $(nQ, n\overline{Q})$ propagation delays and the reset pulse width and the $n\overline{R}$ to $n\overline{CP}$ removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

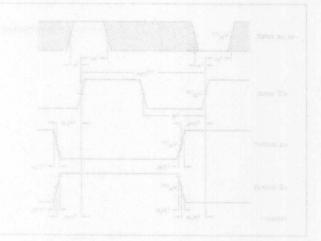
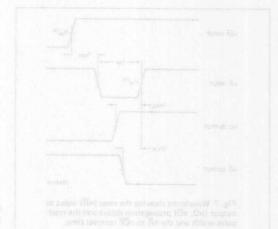


Fig. 5 Viewforms showing the clieck (nCP) to output (nC, nC) propagation delays, the clieck pulse width, the J and K to nCP server and pulse width, the proper terminal and the property of the continue of the clieck pulse of the continue of the clieck pulse of the continue of the clieck pulse of the continue of the continue of the clieck pulse of the clieck

e property

The shaded areas indicate when the input is permitted to change for predictable output conformance.



Vote to AC weveroring (1) HC : V_M = 50%; V₁ = 5WD to V_{CC} HCT: V_M = 1.2 V; V₁ = 5WD to 3 V;

DUAL D-TYPE FLIP-FLOP WITH SET AND RESET; POSITIVE-EDGE TRIGGER

FEATURES

- Output capability: standard
- · ICC category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT74 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT74 are dual positiveedge triggered, D-type flip-flops with individual data (D) inputs, clock (CP) inputs, set (\overline{S}_D) and reset (\overline{R}_D) inputs; also complementary Ω and $\overline{\Omega}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOWto-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

ABBAT	NUNDAUA	CONDITIONS	TYF			
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT	
tPHL/ H	propagation delay nCP to nQ, nQ nSp to nQ, nQ nRp to nQ, nQ	C _L = 15 pF V _{CC} = 5 V	14 15 16	15 18 18	ns ns ns	
f _{max}	maximum clock frequency		76	59	MHz	
CITURNI	input capacitance	e los 08	3.5	3.5	pF	
CPD	power dissipation capacitance per flip-flop	notes 1 and 2	24	29	pF	

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes Hotel

- 1. CPD is used to determine the dynamic power dissipation (PD in μ W):
- PD = CPD x VCC² x f₁ + Σ (CL x VCC² x f₀) where:
- f; = input frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V fo = output frequency in MHz
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is VI = GND to VCC For HCT the condition is $V_1 = GND$ to $V_{CC} - 1.5 V$

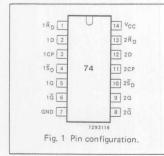
PACKAGE OUTLINES

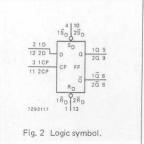
14-lead DIL; plastic (SOT27).

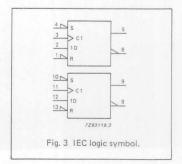
14-lead mini-pack; plastic (SO14; SOT108A).

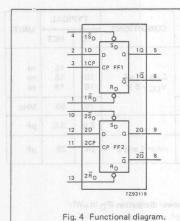
PIN DESCRIPTION

SYMBOL	NAME AND FUNCTION
1RD, 2RD	asynchronous reset-direct input (active LOW)
1D, 2D 1CP, 2CP	data inputs clock input (LOW-to-HIGH, edge-triggered)
1\$D, 2\$D	asynchronous set-direct input (active LOW)
10, 20	true flip-flop outputs
	complement flip-flop outputs
	ground (0 V) positive supply voltage
	1R _D , 2R _D 1D, 2D 1CP, 2CP 1SD, 2SD









FUNCTION TABLE

ARAMETER	INPU	ard .	OUTPUTS				
₹D	RD	СР	D	Q	ā		
On of 90a	H JI	X	X	Н	но Суч в		
on Loan	L	×	×	н	H		

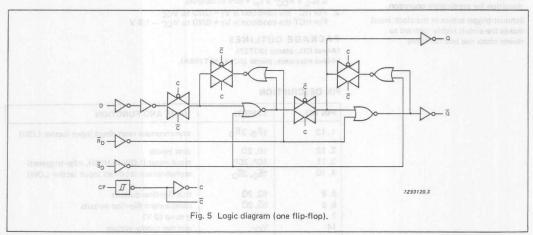
OND THE	INPL	OUTPUTS			
\overline{s}_D	RD	СР	D	Q _{n+1}	Ō _{n+1}
Н	Н	1	Lizza	oni (glif) res	n bH (a
H	H	1	Н	and CHurps	D vogane

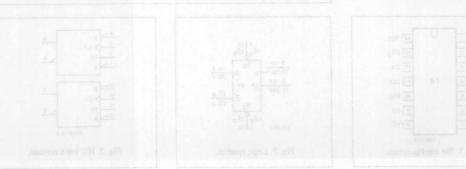
= HIGH voltage level

= LOW voltage level = don't care

= LOW-to-HIGH CP transition

 Q_{n+1} = state after the next LOW-to-HIGH CP transition







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". See additional and the section of the DC characteristics are chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: flip-flops

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF slott and it mode installation and yet unavaily vigitud, graph sea 30 (A snitmests) of

					T _{amb} (°C)		1	le u		TEST CONDIT	
					74H	С			UNIT	V	WAVEFORMS	
SYMBOL	PARAMETER	+25			-40 to +85 -40 to			o +125	UNIT	V _{CC}	WAVEFORW	On mAn
		min.	typ.	max.	min.	max.	min.	max.			08.0	
tPHL/	propagation delay nCP to nQ, nQ		47 17 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6	
^t PHL [/]	propagation delay n\$\overline{S}_D\$ to nQ, n\$\overline{Q}\$		50 18 14	200 40 34		250 50 43		300 60 51	ns and	2.0 4.5 6.0	Fig. 7	
tPHL/	propagation delay nRD to nQ, nQ		52 19 15	200 40 34	TOH	250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 7	JOBMY
tTHL/ tTLH	output transition time	3650	19 7 6	75 15 13	or an	95 19 16	1.09	110 22 19	ns	2.0 4.5 6.0	Fig. 6	
tW	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6	ATH6
tW	set or reset pulse width	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	ATH6 HIR
^t rem	removal time	30 6 5	3 1 1		40 8 7		45 9 8		ns ⁶¹	2.0 4.5 6.0	Fig. 7 2 40	TUH!
^t su	set-up time nD to nCP	60 12 10	6 2 2	2	75 15 13		90 18 15	81	ns	2.0 4.5 6.0	Fig. 6	W
[†] h	hold time nD to nCP	3 3 3	-6 -2 -2	8	3 3 3	8	3 3 3	a	ns	2.0 4.5 6.0	Fig. 6	mer
fmax	maximum clock pulse frequency	6.0 30 35	23 69 82		4.8 24 28	ir .	4.0 20 24	12	MHz	2.0 4.5 6.0	Fig. 6	US

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: flip-flops

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD
nD	0.70
nRD	0.70
nSD	0.80
nCP	0.80

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	9.0				T _{amb} (°C)					TEST CONDITION	S
	2.0 ns 4.5 Fig.7	(1)			74HC	т	01 E		UNIT	visiati v Do	WAVEFORMS	PHU
SYMBOL	PARAMETER 0.8	+25		-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORING		
	2:0 ns - 4.5 Fig. 6	min.	typ.	max.	min.	max.	min.	max.		nis nois		LIT
tPHL/ tPLH	propagation delay nCP to nQ, nQ		18	35	66	44	0	53	ns	4.5	Fig. 6	
t _{PHL} /	propagation delay nSD to nQ, nQ		23	40		50		60	ns	4.5	Fig. 7	
tPHL/ tPLH	propagation delay nRD to nQ, nQ		24	40		50		60	ns	4.5	Fig. 7	VV
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 6	men
tW	clock pulse width HIGH or LOW	18	9	9	23	V.	27	9 08	ns	4.5	Fig. 6	
tW	set or reset pulse width LOW	16	9	T	20		24	0	ns	4.5	Fig. 7	Lie
^t rem	removal time set or reset	6	1	833	8	W 600 FG	9	- E	ns	4.5	Fig. 7	19
t _{su}	set-up time nD to nCP	12	5	20	15	2	18	0.0	ns	4.5	Fig. 6	жел
th	hold time nD to nCP	3	-3		3		3		ns	4.5	Fig. 6	
f _{max}	maximum clock pulse frequency	27	54		22		18		MHz	4.5	Fig. 6	

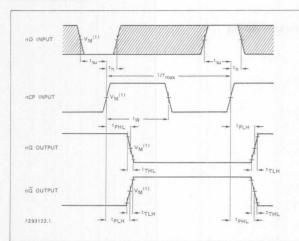


Fig. 6 Waveforms showing the clock (nCP) to output (nQ, $n\bar{\Omega}$) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

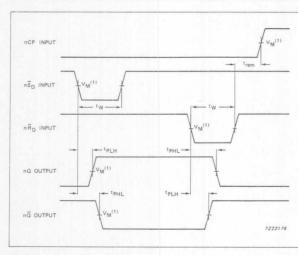


Fig. 7 Waveforms showing the set $(n\overline{\mathbb{S}}_D)$ and reset $(n\overline{\mathbb{R}}_D)$ input to output $(nQ, n\overline{Q})$ propagation delays, the set and reset pulse widths and the $n\overline{\mathbb{R}}_D$ to nCP removal time.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_1 = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_1 = GND$ to 3 V.

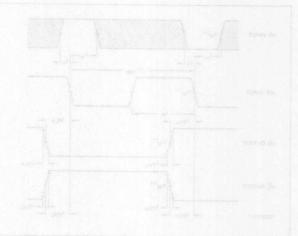
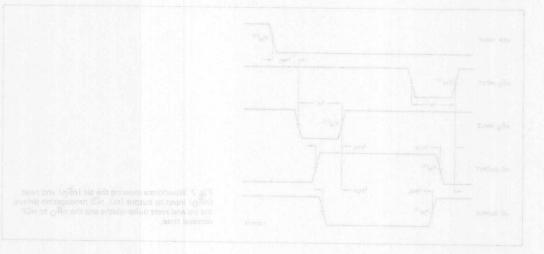


Fig. 6 Waveforms showing the clock (nCPI to output (nC), nO), propagation delays, the clock pursue width, the nD to nCP set-up, the nCP to nD hold times the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

Fire shaded areas indicate when the input is sentimed to change for predictable output,



Note to AC waveforms

(1) HC : VM = 50%, VI = 6ND to VCC HCT: Ver = 1.3 V: VI = 6ND to 3 V

QUAD BISTABLE TRANSPARENT LATCH

FEATURES

- Complementary Q and Q outputs
- VCC and GND on the centre pins
- Output capability: standard
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT75 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT75 have four bistable latches. The two latches are simultaneously controlled by one of two active HIGH enable inputs (LE $_{1-2}$ and LE $_{3-4}$). When LE $_{n-n}$ is HIGH, the data enters the latches and appears at the nQ outputs. The nQ outputs follow the data inputs (nD) as long as LE $_{n-n}$ is HIGH (transparent). The data on the nD inputs one set-up time prior to the HIGH-to-LOW transition of the LE $_{n-n}$ will be stored in the latches. The latched outputs remain stable as long as the LE $_{n-n}$ is LOW.

0.44004	DADAMETED.	CONDITIONS	TYF	UNIT	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
^t PHL/ ^t PLH	propagation delay nD to nQ, nQ LE _{n-n} to nQ, nQ	C _L = 15 pF V _{CC} = 5 V	11	12 11	ns ns
CI	input capacitance	w bt	3.5	3.5	pF
C _{PD}	power dissipation capacitance per latch	notes 1 and 2	42	42	pF

GND = 0 V; $T_{amb} = 25 \,^{\circ}C$; $t_r = t_f = 6 \, \text{ns}$

Note

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD
$$\times$$
 VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

- fi = input frequency in MHz
- CL = output load capacitance in pF
- fo = output frequency in MHz
- VCC = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

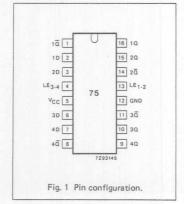
PACKAGE OUTLINES

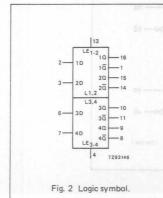
16-lead DIL; plastic (SOT38Z).

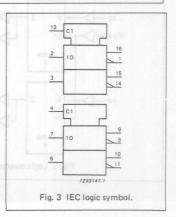
16-lead mini-pack; plastic (SO16; SOT109A).

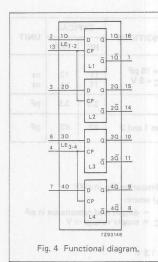
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 14, 11, 8	10 to 40	complementary latch outputs
2, 3, 6, 7	1D to 4D	data inputs
4	LE3-4	latch enable input, latches 3 and 4 (active HIGH)
5	Vcc	positive supply voltage
12	GND	ground (0 V)
13	LE ₁₋₂	latch enable input, latches 1 and 2 (active HIGH)
16, 15, 10, 9	1Q to 4Q	latch outputs





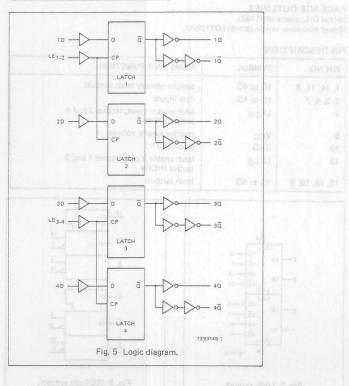




FUNCTION TABLE

OPERATING MODES	INPU	TS	OUTPUTS		
OPERATING MODES	LE _{n-n}	nD	nQ	nQ	
data enabled	Н	L	L	H	
data latched	L	X	q	q	

- H = HIGH voltage level
- L = LOW voltage level
- q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW LE_{n-n} transition
- X = don't care



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", see apparent and a section of the DC characteristics are chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

					Tamb (°C)		Г	TEST CONDIT	ONS		
					74HC	:				7	COEFFICIEN	10/168
SYMBOL	PARAMETER		+25		-401	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORM	S LEnen
		min.	typ.	max.	min.	max.	min.	max.				
^t PHL/ ^t PLH	propagation delay nD to nQ		33 12 10	110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} /2//0 t _{PLH}	propagation delay		39 14 11	120 24 20	(O°) d	150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 7	
t _{PHL} / t _{PLH}	propagation delay LE _{n-n} to nQ	125 25	33 12 10	120 24 20	3+ cr O	150 30 26	ios sets la	180 36 31	ns	2.0 4.5 6.0	Fig. 8	MBOL
t _{PHL} /	propagation delay LE _{n-n} to nQ	2 5	39 14 11	125 25 21	35	155 31 26	28	190 38 32	ns	2.0 4.5 6.0	Fig. 8	\underset
tTHL/ tTLH	output transition time	se S	19 7 6	75 15 13	38	95 19 16	28	110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7	HT/
tW	enable pulse width	80 16 14	17 6 5		100 20 17		120 24 20	81	ns	2.0 4.5 6.0	Fig. 8	NH.
t _{su}	set-up time nD to LE _{n-n}	60 12 10	14 5 4		75 15 13		90 18 15	7	ns	2.0 4.5 6.0	Fig. 9	HT/ HT/
th	hold time nD to LE _{n-n}	3 3	-8 -3 -2	24	3 3 3	20	3 3 3	6 4	ns	2.0 4.5 6.0	Fig. 9	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD
nD	0.75
LE _{n-n}	1.00

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V; } t_r = t_f = 6 \text{ ns; } C_L = 50 \text{ pF}$

		es (25	E S		T _{amb} (°C)	129	39		Vsle	TEST CONDITION	
		1 1 1	0		74HC	т	09.				Em or un	
SYMBOL	PARAMETER	+25			-40 to +85 -40 to			o +125	UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				HTd
^t PHL/ ^t PLH	propagation delay nD to nQ	20 E	15	28	151 31 28	35	125 26 21	42	ns	4.5	Fig. 6	
tPHL/ tPLH	propagation delay nD to nŌ	03	15	28	36	35	76	42	ns	4.5	Fig. 7	инт
tPHL/ tPLH	propagation delay LE _{n-n} to nQ	-	13	28	ar c	35	13	42	ns	4.5	Fig. 8	17,41
tPHL/ tPLH	propagation delay LE _{n-n} to nŌ	all	15	30		38		45	ns	4.5	Fig. 8	V
tTHL/ tTLH	output transition time	4	7	15		19		22	ns	4.5	Figs 6 and 7	131
tw	enable pulse width HIGH	16	4	2 2	20	200	24		ns	4.5	Fig. 8	
t _{su}	set-up time nD to LE _{n-n}	12	4	6	15	£	18		ns	4.5	Fig. 9	
th	hold time nD to LE _{n-n}	3	-2		3		3		ns	4.5	Fig. 9	

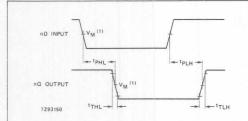


Fig. 6 Waveforms showing the data input (nD) to output (nQ) propagation delays and the output transition times.

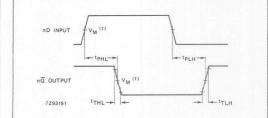


Fig. 7 Waveforms showing the data input (nD) to output (nQ) propagation delays and the output transition times.

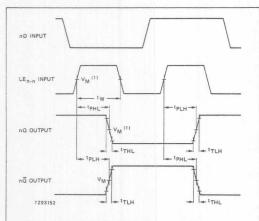
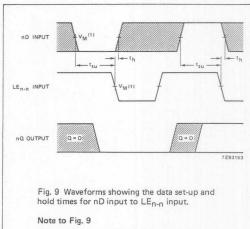


Fig. 8 Waveforms showing the latch enable input (LEn,n) pulse width, the latch enable input to outputs (nQ, $n\overline{Q}$) propagation delays and the output transition times.



The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.



Fig. 6 Waveforms showing the deta input (nD) to output (nO) propagation delays and the output transition times.

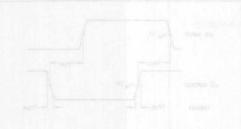


Fig. 7 Waveforms showing the data input (nD) to currout (nD) propagation delays and the purput transition times.

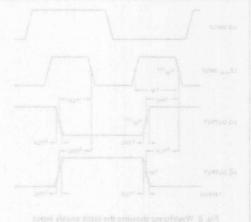


Fig. 8. Waveforms showing the latch enable input to $(LE_{\rm Per})$ pulse width, the latch enable input to outputs (nO, n $\overline{\rm O}$) propagation delays and that output transition times.



Fig. 9 Waveforms showing the data set-up an hold timus for nO logalt to $LE_{0:\rm cl}$ input.

Note to Flac

The sheded areas indicate when the input is permitted to clistics for predictable output performance.

Note to AC waveforms

1) RC : V_M = 80%; V₁ = GND to V_{CC}. HOT: V_M = 1.3 V; V₁ = GND to 3 V.

4-BIT MAGNITUDE COMPARATOR

FEATURES

- Serial or parallel expansion without extra gating
- Magnitude comparison of any binary words
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT85 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT85 are 4-bit magnitude comparators that can be expanded to almost any length. They perform comparison of two 4-bit binary, BCD or other monotonic codes and present the three possible magnitude results at the outputs (QA>B, QA=B and QA<B). The 4-bit inputs are weighted (A0 to A3 and B0 to B3), where A3 and B3 are the most significant bits.

The operation of the "85" is described in the function table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed forward conditions that exist in the parallel expansion scheme.

For proper compare operation the expander inputs ($I_A>_B$, $I_A=_B$ and $I_A<_B$) to the least significant position must be connected as follows: $I_A<_B=I_A>_B=$ = LOW and $I_A=_B=HIGH$. For words greater than 4-bits, units can be cascaded by connecting outputs $Q_A<_B$, $Q_A>_B$ and $Q_A=_B$ to the corresponding inputs of the significant comparator.

OVAROL	APPLICATIONS	CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT	
t _{PHL} /	propagation delay A_n , B_n to $Q_A > B$, $Q_A < B$ A_n , B_n to $Q_{A=B}$	C ₁ = 15 pF	20 18	22 20	ns ns	
^t PLH	1A <b, 1a="">B to QA<b, qa="">B 1A=B to QA=B</b,></b,>	C _L = 15 pF V _{CC} = 5 V	15	15 15	ns ns	
Cl	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	18	20	pF	

GND = 0 V; $T_{amb} = 25 \,^{\circ}C$; $t_r = t_f = 6 \, \text{ns}$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x VCC^2 x f_i + Σ (CL x VCC^2 x f_o) where:

fi = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

 f_0 = output frequency in MHz $\Sigma (C_L \times V_{CC}^2 \times f_0)$ = sum of outputs

2. For HC the condition is V $_{\rm I}$ = GND to V_{CC} For HCT the condition is V $_{\rm I}$ = GND to V_{CC} - 1.5 V

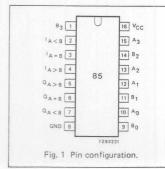
PACKAGE OUTLINES

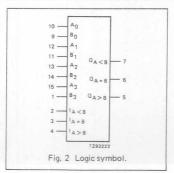
16-lead DIL; plastic (SOT38Z).

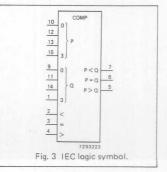
16-lead mini-pack; plastic (SO16; SOT109A).

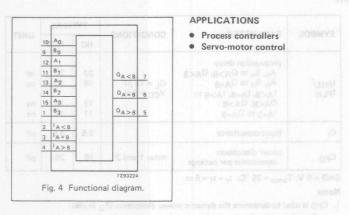
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	e8=eA	Egety Egety
2	IA <b< td=""><td>A < B expansion input</td><td></td><td></td></b<>	A < B expansion input		
3 H	IA=B	A = B expansion input		
4	IA>B	A > B expansion input		
5	QA>B	A > B output		
6	QA=B	A = B output		
7	QA <b< td=""><td>A < B output</td><td></td><td></td></b<>	A < B output		
8	GND	ground (0 V)		
9, 11, 14, 1,	Bo to B3	word B inputs		
10, 12, 13, 15	An to A3	word A inputs		
16	VCC	positive supply voltage		



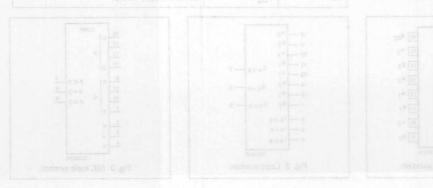


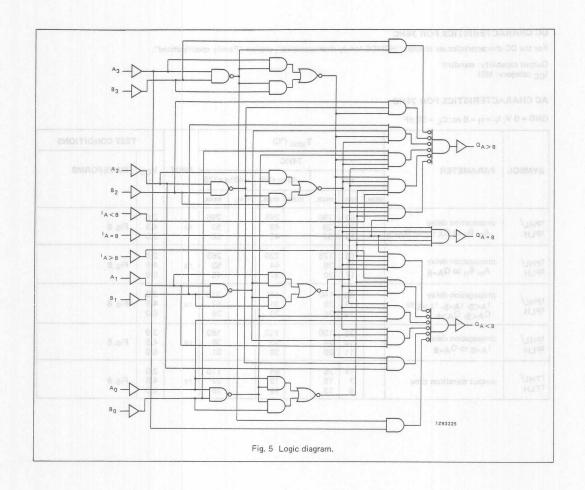




FUNCTION TABLE

CC	OMPARIN	G INPUTS	- DOV	CASCA	ADING IN	NPUTS	TOURNE	OUTPUTS	S EA	us 4-bit inputs are weighted (Ap to d Sh to Ro), where An and Ro an
A ₃ , B ₃	A ₂ , B ₂	A ₁ , B ₁	A ₀ , B ₀	I _{A>B}	I _A <b< th=""><th>I_{A=B}</th><th>Q_{A>B}</th><th>Q_{A<b< sub=""></b<>}</th><th>Q_{A=B}</th><th>erid musikingis sas</th></b<>	I _{A=B}	Q _{A>B}	Q _{A<b< sub=""></b<>}	Q _{A=B}	erid musikingis sas
A 3 > B 3 A 3 < B 3 A 3 = B 3	X X A ₂ >B ₂ A ₂ <b<sub>2 A₂=B₂ A₂=B₂ A₂=B₂ A₂=B₂</b<sub>	X X X X X A ₁ >B ₁ A ₁ <b<sub>1 A₁=B₁</b<sub>	X X X X X A ₀ >B ₀ A ₀ <8 ₀	X X X X X	X X X X X X X X	X X X X X X	H LO 3D Hing JI Loo ini H CRAOR H		L so	function table, showing all posts to conditions. The upper per of the describes the normal operation der all conditions that will eccur for all conditions that will eccur feel and conditions that will eccur feel to the table output are mutually exit the lower per of the table, the of
A ₃ =B ₃ A ₃ =B ₃ A ₃ =B ₃	A ₂ =B ₂ A ₂ =B ₂ A ₂ =B ₂	A ₁ =B ₁ A ₁ =B ₁ A ₁ =B ₁	A0=B0 A0=B0 A0=B0	HA BLA FLA	L H L	E>Al Li=Al H <al< td=""><td>H L L</td><td>L & H & L & A</td><td>L L H</td><td>at in the parallel expansion scheme recorder from the spander inputs $(A>9, A=9$ and 1 the least significant position must</td></al<>	H L L	L & H & L & A	L L H	at in the parallel expansion scheme recorder from the spander inputs $(A>9, A=9$ and 1 the least significant position must
A ₃ =B ₃ A ₃ =B ₃ A ₃ =B ₃	A ₂ =B ₂ A ₂ =B ₂ A ₂ =B ₂	A ₁ =B ₁ A ₁ =B ₁ A ₁ =B ₁	A ₀ =B ₀ A ₀ =B ₀ A ₀ =B ₀	X H L	X H L	H	L L H	L B K	H L L ed nes	H = HIGH voltage level L = LOW voltage level X =don't care





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

			-		T _{amb} (°C)					TEST CONDITIONS	
CVANDO	PARAMETER				74H	С			LINUT		WANTEDDAM.	
SYMBOL		+25			-40 to +85		-40 to +125		UNIT	VCC V	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
^t PHL [/] ^t PLH	propagation delay An, Bn to QA>B or QA <b< td=""><td></td><td>63 23 18</td><td>195 39 33</td><td></td><td>245 49 42</td><td></td><td>295 59 50</td><td>ns</td><td>2.0 4.5 6.0</td><td>Fig. 6</td></b<>		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6	
^t PHL [/] ^t PLH	propagation delay A _n , B _n to Q _{A=B}		58 21 17	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6	
^t PHL [/]	propagation delay $ A < B, A = B, A > B \text{ to}$ $QA < B, QA > B$		50 18 14	140 28 24	H,	175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 6	
^t PHL [/] ^t PLH	propagation delay		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 6	
t _{THL} /	output transition time		19 7 6	75 15 13	-,1	95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

V S of CMD = IV: V S, I + IVV : TOH

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD
IA <b< td=""><td>1.00</td></b<>	1.00
IA>B	1.00
IA=B	1.50
An, Bn	1.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

					T _{amb} (°C)				TEST CONDITIONS			
					74H	СТ							
SYMBOL	PARAMETER		+25		-40	to +85	-40 to	+125	UNIT	V _{CC}	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.		CONTRACT.			
tPHL/ tPLH	propagation delay A_n , B_n to $Q_{A>B}$ or Q_{A		26	44		55		66	ns	4.5	Fig. 6		
tPHL/ tPLH	propagation delay A_n , B_n to $Q_{A=B}$		24	40		50		60	ns	4.5	Fig. 6		
^t PHL [/] ^t PLH	propagation delay $ A < B, A = B, A > B \text{ to}$ $QA < B, QA > B$		18	31		39		47	ns	4.5	Fig. 6		
t _{PHL} /	propagation delay I _{A=B} to Q _{A=B}		18	31		39		47	ns	4.5	Fig. 6		
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 6		

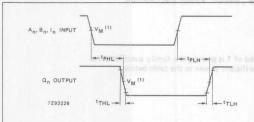


Fig. 6 Waveforms showing the word A inputs (A_{Π}) , word B inputs (B_{Π}) and expansion inputs (I_{Π}) to the outputs (Q_{Π}) propagation delays and the output transition times.

OC CHARACTERISTICS FOR TAHOT

Output depability: standard Inc. category: MSI

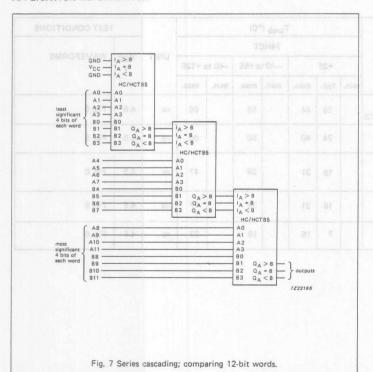
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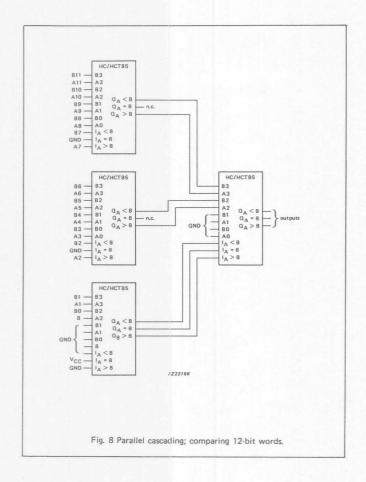
To determine \$100 per input, multiply this
INPUT UNIT LOAD
OOSFFICIENT

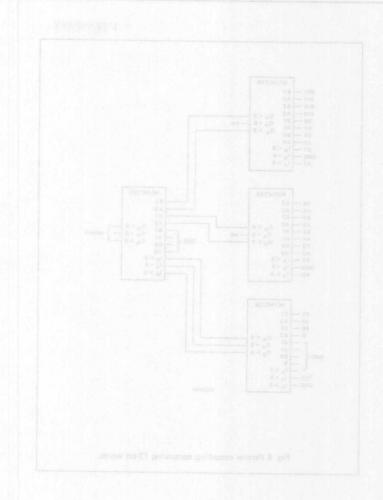
Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_1 = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_1 = GND$ to 3 V.

APPLICATION INFORMATION







QUAD 2-INPUT EXCLUSIVE-OR GATE

FEATURES

- Output capability: standard
- · ICC category: SSI

GENERAL DESCRIPTION

The 74HC/HCT86 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT86 provide the EXCLUSIVE-OR function.

		CONDITIONS	TYF	UNIT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
tPHL/	propagation delay nA, nB to nY	C _L = 15 pF V _{CC} = 5 V	11	14	ns
CI	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per gate	notes 1 and 2	30	30	pF

GND = 0 V;
$$T_{amb} = 25 \,^{\circ}\text{C}$$
; $t_r = t_f = 6 \, \text{ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

fi = input frequency in MHz f_O = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 VUTTUO

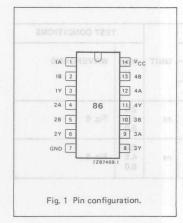
PACKAGE OUTLINES

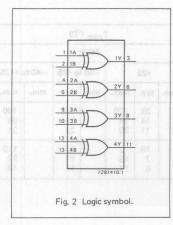
14-lead DIL; plastic (SOT27)

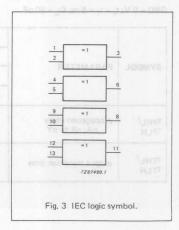
14-lead mini pack; plastic (SO14; SOT108A)

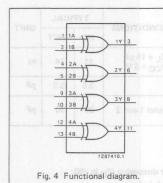
PIN DESCRIPTION

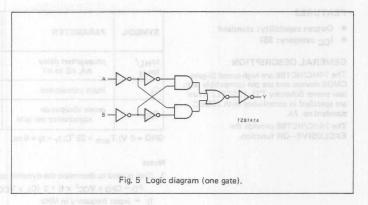
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs 12000 598 coltra entra DC arts 10-3
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	Vcc	positive supply voltage











FUNCTION TABLE

INP	UTS	OUTPUTS
nA	nB	nΥ
L	L	L
L	Н	Н
Н	L	Н
H	Н	L

H = HIGH voltage level L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: SSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	10 1				T _{amb} (°C)				TEST CONDITIONS		
SYMBOL				74HC	UNIT	V	WAVEFORMS					
	PARAMETER		+25		-401	to +85	-40 t	o +125	ONT	V _{CC}	WAVEFORMS	
	-	min.	typ.	max.	min.	max.	min.	max.		48 BI		
tPHL/	propagation delay nA, nB to nY		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 6	
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.0

AC CHARACTERISTICS FOR 74HCT VE. 1 - MV TOH

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

					r _{amb} (°C)				TEST CONDITIONS		
SYMBOL	DADAMETER				74HC	Т			UNIT	V _{CC}	WAVEFORMS Fig. 6	
	PARAMETER		+25		-40 t	to +85	-40 t	o +125	Oldii			
		min.	typ.	max.	min.	max.	min.	max.				
^t PHL/ ^t PLH	propagation delay nA, nB to nY		17	32		40		48	ns	4.5	Fig. 6	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 6	

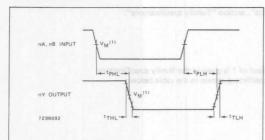


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

For the DD standard define on shower WWW.

Output capability: standard

The value of additional quiescent supply current (office) for a To determine office or locut, muttiply this value by the unit

INPUT LOAD TUNIT LOAD TUNIT LOAD TO THE TOTAL TO THE TOTA

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} .

HCT: V_M = 1.3 V; V_I = GND to 3 V.

4-BIT BINARY RIPPLE COUNTER

FEATURES

- Various counting modes
- Asynchronous master reset
- Output capability: standard
 ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT93 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT93 are 4-bit binary ripple counters. The devices consist of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input (CF0 and CF1) to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Ω_0 outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous master reset (MR₁ and MR₂) is provided which overrides both clocks and resets (clears) all flio-floos.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output C_0 must be connected externally to input \overline{CP}_1 . The input count pulses are applied to clock input \overline{CP}_0 . Simultaneous frequency divisions of 2, 4, 8 and 16 are performed at the Q_0 , Q_1 , Q_2 and Q_3 outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input \overline{CP}_1 .

Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1 , Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

CP ₁ 1	U	14 CP ₀
MR ₁ 2		13 n.c.
MR ₂ 3		12 Q ₀
n.c. 4	93	11 03
Vcc 5		10 GND
n.c. 6		9 Q ₁
n.c. 7		8 Q ₂
	7293	820
Fig. 1 Pi	n confi	guration.

SYMBOL	PARAMETER	CONDITIONS	TYP	UNIT	
STIVIBUL	PARAMETER	CONDITIONS	НС	нст	UNIT
t _{PHL} /	propagation delay CP ₀ to Q ₀	C _L = 15 pF V _{CC} = 5 V	12	15	ns
f _{max}	maximum clock frequency	ACC = 2 A	100	77	MHz
CI	input capacitance	15	3.5	3.5	pF
CPD power dissipation capacitance per package		notes 1 and 2	22	22	pF

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD
$$\times$$
 VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

f; = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF

VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC $\,$ the condition is V $_{\rm I}$ = GND to V $_{\rm CC}$ For HCT the condition is V $_{\rm I}$ = GND to V $_{\rm CC}$ - 1.5 V

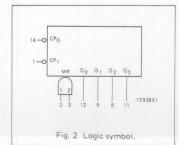
PACKAGE OUTLINES

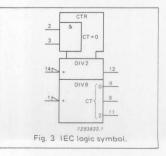
14-lead DIL; plastic (SOT27)

14-lead mini pack; plastic (SO14; SOT108A)

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP ₁	clock input 2 nd , 3 rd and 4 th section (HIGH-to-LOW, edge-triggered)
2, 3	MR ₁ , MR ₂	asynchronous master reset (active HIGH)
4, 6, 7, 13	n.c.	not connected
5	Vcc	positive supply voltage
10	GND	ground (0 V)
12, 9, 8, 11	Q ₀ to Q ₃	flip-flop outputs
14	CP ₀	clock input 1 st section (HIGH-to-LOW, edge-triggered)





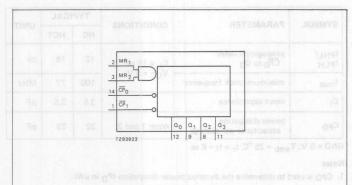
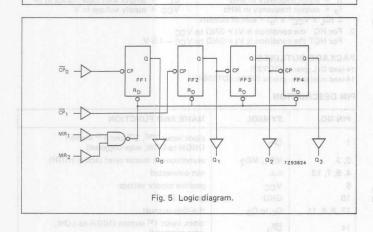


Fig. 4 Functional diagram.



FUNCTION TABLE

COUNT	masser	OUTI	PUTS	2 4
COUNT	Ω ₀	01	02	03
		L DL30	L ERAL MHJ N	-
	Haz	Hio 8	0. L O s	L.
4 beilio	H	rarLT .(. VitinUEI	Ha	
8 9 10 11	L H L		Table 1	HHH
12 13 14 15	MSD DOWN	en ste	H	HHHH

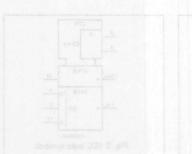
MODE SELECTION

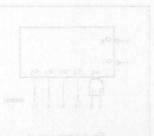
RESET	INPUTS	6 8200	OUTPUTS							
MR ₁	MR ₂	00	01	02	03					
Holbi	Н	Luci	est <u>i</u> lite	n Li ne	L					
L od s	H soivs	b outr	COL	unt	succe					
H	orti anine	s cour	count state							
FO in	Etto entr	atnuc	strucc s count							

Note to function table Output Q₀ connected to $\overline{\text{CP}}_1$.

H = HIGH voltage level

L = LOW voltage level







DC CHARACTERISTICS FOR 74 HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL					Tamb	°C)		TEST CONDITIONS				
					74H	С		FIA	\$10174340			
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/	propagation delay CP ₀ to Q ₀		41 15 12	125 25 21		155 31 26		190 38 32	ns _{Aq}	2.0 4.5 6.0	Fig. 6	
t _{PHL} /************************************	propagation delay		49 16 13	135 27 23	(0°) _d	170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} /	propagation delay CP ₁ to Q ₂	851	61 22 18	185 37 31	+ 07 01	230 46 39	25	280 56 48	ns	2.0 4.5 6.0	Fig. 6	JOSMY
t _{PHL} /	propagation delay	n i	80 29 23	245 49 42	E4+	305 61 52	NS 1	370 71 63	ns	2.0 4.5 6.0	Fig. 6	PHL/ PLH
^t PHL	propagation delay MR _n to Q _n	d t	50 18 14	155 31 26	43	195 39 33	34	235 47 40	ns	2.0 4.5 6.0	Fig. 7	PHE/ PLH PULL
t _{THL} /	output transition time	0 6	19 7 6	75 15 13	EC .	95 19 16	88 1	110 22 19	ns	2.0 4.5 6.0	Fig. 6	PLH PHL/
^t rem	removal time MR _n to $\overline{\text{CP}}_0$, $\overline{\text{CP}}_1$	50 10 9	8 3 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7	JH9
tw	pulse width CP ₀ , CP ₁	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6	UHT HUT
tw	master reset pulse width	80 16 14	14 5 4	24	100 20 17	20	120 24 20	16 7	ns	2.0 4.5 6.0	Fig. 7	W
f _{max}	maximum clock pulse frequency $\overline{\text{CP}}_0$, $\overline{\text{CP}}_1$	6.0 30 35	30 91 108	es l	4.8 24 28	20	4.0 20 24	2 at	MHz	2.0 4.5 6.0	Fig. 6	W

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
CP ₀ , CP ₁	0.60 VAW 33 0.40

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	2,0 ns 4.5 Fig. 6	T _{amb} (°C)								TEST CONDITIONS		
SYMBOL	0.3	74HCT 88 81									Un or Lan Ha	
	PARAMETER D.S.	08	+25	+25		-40 to +85		-40 to +125		VCC	WAVEFORMS	
	0,8	min.	typ.	max.	min.	max.	min.	max.			2000110	HII9
tPHL/ tPLH	propagation delay CP ₀ to Q ₀	1 1	18	34	58	43	AS 42	51	ns	4.5	Fig. 6	
tPHL/ tPLH	propagation delay	35	18	34	91 39	43	31 (1 18 31	51	ns	4.5	Fig. 6	1149
tPHL/	propagation delay	01	24	46	80	58	35 6	69	ns	4.5	Fig. 6	A read
t _{PHL} /	propagation delay CP ₁ to Q ₃	6	30	58	81	73		87	ns	4.5	Fig. 6	HJ
^t PHL	propagation delay MR _n to Q _n		17	33		41		50	ns	4.5	Fig. 7	ente
tTHL/ tTLH	output transition time		7	15	0	19		22	ns	4.5	Fig. 6	V
^t rem	removal time MR _n to CP ₀ , CP ₁	10	3	20	13		15	A A.	ns	4.5	Fig. 7	
tw	pulse width \overline{CP}_0 , \overline{CP}_1	16	7	24	20	20	24	a a	ns	4.5	Fig. 6	V
tw	master reset pulse width MRn	16	5	20	20	4 52 4	24	E 03	ns	4.5	Fig. 7	хвг
f _{max}	maximum clock pulse frequency \overline{CP}_0 , \overline{CP}_1	30	70		24		20		MHz	4.5	Fig. 6	

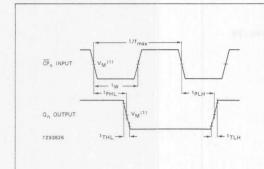


Fig. 6 Waveforms showing the clock (\overline{CP}_n) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

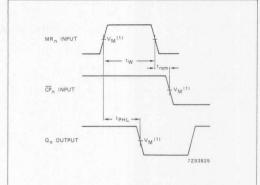


Fig. 7 Waveforms showing the master reset (MRn) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock $(\overline{\mathsf{CP}}_n)$ removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

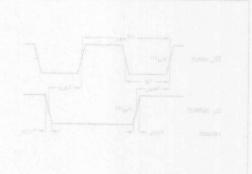


Fig. 6 Waveforms showing the clock $(\overline{\mathbb{CP}}_n)$ to ourset (\mathbb{O}_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.



Fig. 7. Waveforms showing the master reset (MR) guits width, the master reset to output $\{O_{n}\}$ incopagation delays and the master reset to clock $\{O_{n}\}$; removed time.

Marin an All manufaces

(1) HC: $V_M = 50\%$; $V_1 = 6ND$ to V_{CC} .

HCT: $V_M = 1.3 V$; $V_1 = 6ND$ to 3 V.

DUAL JK FLIP-FLOP WITH RESET; NEGATIVE-EDGE TRIGGER

FEATURES

- Output capability: standard
- ICC category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT107 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT107 are dual negative-edge triggered JK-type flip-flops featuring individual J, K, clock (nCP) and reset (nR) inputs; also complementary Q and Q outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset $(n\,\overline{R})$ is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the \overline{Q} output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

CVMPOL	LH nCP to nQ nR to nQ, nQ	CONDITIONS	TYF	LIMIT	
SAMBOL	PARAMETER	CONDITIONS	НС	нст	ns ns ns MHz
^t PHL [/] ^t PLH	nCP to nQ nCP to nQ	C _L = 15 pF V _{CC} = 5 V	16 16 16	16 18 17	ns
fmax	maximum clock frequency		78	73	MHz
CI	input capacitance	a los [3.5	3.5	pF
C _{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	30	30	pF

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

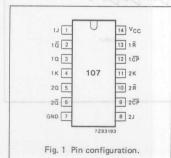
- 1. CPD is used to determine the dynamic power dissipation (PD in μ W):
 - PD = CPD x VCC^2 x f_i + Σ (CL x VCC^2 x f_o) where:
 - f; = input frequency in MHz f_O = output frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V
- Σ (C_L x V_{CC}² x f₀) = sum of outputs Σ (C_C = supply voltage in
- 2. For HC the condition is VI = GND to VCC For HCT the condition is VI = GND to VCC - 1.5 V

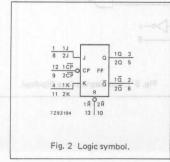
PACKAGE OUTLINES

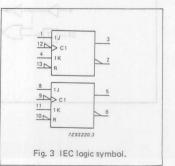
- 14-lead DIL; plastic (SOT27).
- 14-lead mini-pack; plastic (SO14; SOT108A).

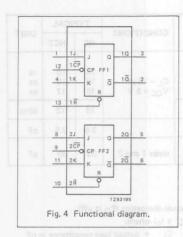
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 8, 4, 11 2, 6	1J, 2J, 1K, 2K 1\overline{Q}, 2\overline{Q}	synchronous inputs; flip-flops 1 and 2 complement flip-flop outputs
3, 5	1Q, 2Q GND	true flip-flop outputs ground (0 V)
12, 9	1CP, 2CP	clock input (HIGH-to-LOW, edge-triggered)
13, 10	1R, 2R	asynchronous reset inputs (active LOW)
14	Vcc	positive supply voltage









FUNCTION TABLE

ODED A TIMO MODE		INPU	OUTPUTS			
OPERATING MODE	nR	nCP	J	К	Q	ā
asynchronous reset	L	×	Х	X	L	Н
toggle	Н	1	h	h	q	q
load "0" (reset)	Н	1	1 -	h	DS TIG	H
load "1" (set)	Н	+	h	1	Н	L
hold "no change"	Н	1	1	1	q	q

Da of 50n \ \1967 \ Da of 50n \ \1967 \ Da of 50n \ \1967 \ Da of 50n \ Da of 50n \ Da of 6n \ Da o

CAND = 0 V: $T_{\rm BMD}$ = 25 °C; $t_{\rm F}$ = $t_{\rm F}$ = 6 m. Notes: 1. CPD is used to determine the dynami

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition

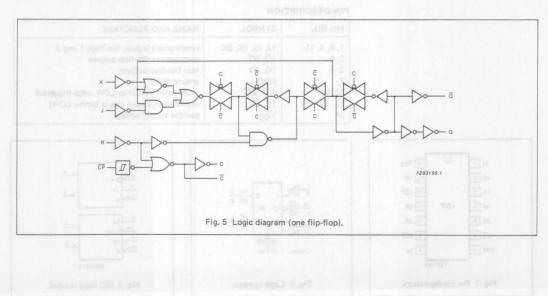
L = LOW voltage level

I = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition

X = don't care

↓ = HIGH-to-LOW CP transition



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", as a section and a section of the DC characteristics are chapter of the DC characteristics.

Output capability: standard ICC category: flip-flops

AC CHARACTERISTICS FOR 74HC must set in days at 1 to be of time a not (2016) the two yields the scale plane in block to outer set (2016) the two yields and time at 10 and yields and yield yields and time at 10 and yields and an

						Tamb (°C)				9	TEST CONDIT	IONS
						74HC	;				TV	COEFFICIE	
SYMBOL	PARAMETER		+25			-40	-40 to +85 -40 to +		o +125	UNIT	V _{CC}	WAVEFORMS	
			min.	typ.	max.	min.	max.	min.	max.			1.00	
^t PHL [/]	propagation delay nCP to nQ			52 19 15	160 32 27		200 40 34		240 48 41	7AHCT	2.0 4.5 6.0	Fig. 6	
aMON tPHL/ tPLH	propagation delay	LAUL		52 19 15	160 32 27	O") dm	200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6	IOSMY2
tPHL/	propagation delay nR to nQ, nQ		e125 mex.	52 19 15	155 31 26	40 to	195 39 33	+25 typ. n	235 47 40	ns	2.0 4.5 6.0	Fig. 7	
THL/	A.B. Fig. 6 output transition time	art	48	19 7 6	75 15 13	4	95 19 16	19	110 22 19	ns	2.0 4.5 6.0	Fig. 6	HTIA /THA
tw	clock pulse width HIGH or LOW	an	80 16 14	22 8 6	8	100 20 17	83	120 24 20		ns	2.0 4.5 6.0	Fig. 6	HJ9
tw	reset pulse width	arr	80 16 14	22 8 6	8	100 20 17	2	120 24 20		ns en	2.0 4.5 6.0	Fig. 7	UHT THU
^t rem	removal time	sn	60 12 10	19 7 6		75 15 13	1	90 18 15	91	ns	2.0 4.5 6.0	Fig. 7	W
t _{su}	set-up time nJ, nK to nCP	211	100 20 17	22 8 6		125 25 21		150 30 26	20	ns	2.0 4.5 6.0	Fig. 6	man
-h	hold time nJ, nK to nCP	sn	3 3 3	-6 -2 -2		3 3 3		3 3 3	20	ns	2.0 4.5 6.0	Fig. 6	FIE
max	maximum clock pulse frequency	su	6.0 30 35	23 70 85	en Ge	4.8 24 28		4.0 20 24	â	MHz	2.0 4.5 6.0	Fig. 6	B

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", see a submissional DC and no P

Output capability: standard ICC category: flip-flops

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD
nK nR	0.60 0.65
nCP, nJ	1.00

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

				240		00	Tamb (°C)					TEST CONDITION	NS
SYMBOL	PARAMET			74HCT SE ST						UNIT	Vcc	WAVEFORMS	HT45	
STWBOL	FARAMET	2.0		235	+25	- 80	-40	to +85	-40 to	+125	Olari	V	noitsescore	
	Fig. 7	4.5	20	min.	typ.	max.	min.	max.	min.	max.			n R to nQ.	H182
t _{PHL} /	propagation nCP to nQ		en	110	19	36	9	45	7 81	54	ns	4.5	Fig. 6	URT
t _{PHL} /	propagation nCP to nQ			18	21	36		45	22	54	ns	4.5	Fig. 6	
tPHL/ tPLH	propagation nR to nQ,		en.		20	38	Y	48	100	57	ns	4.5	Fig. 7	16/
t _{THL} /	output tran	sition time	20		7	15	00	19	82	22	ns	4.5	Fig. 6	W
tw	clock pulse HIGH or L		an	16	9	9	20		24	60 12	ns	4.5	Fig. 6	man
tw	reset pulse v	width		20	11		25		30	100	ns	4.5	Fig. 7	
^t rem	removal tim		217	14	8		18	8	21	17	ns	4.5	Fig. 7	F15
t _{su}	set-up time nJ, nK to	n CP	661	20	7		25		30	2000	ns	4.5	Fig. 6	11
^t h	hold time nJ, nK to	nCP	THIS	5	-2	6	5		5 68	0.0	ns	4.5	Fig. 6	MEN
f _{max}	maximum c	lock pulse		30	66		24		20	35	MHz	4.5	Fig. 6	

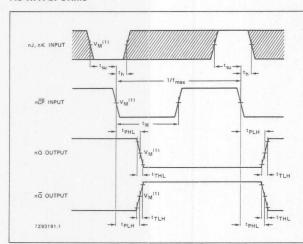
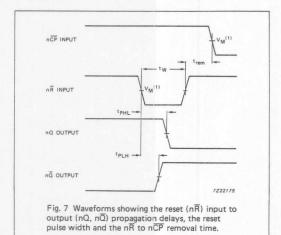


Fig. 6 Waveforms showing the clock ($n\overline{CP}$) to output (nQ, $n\overline{Q}$) propagation delays, the clock pulse width, the J and K to $n\overline{CP}$ set-up and hold times, the output transition times and the maximum clock pulse frequency.

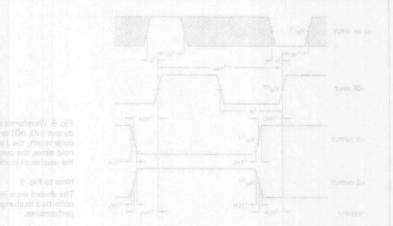
Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.



Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND \text{ to } V_{CC}$. HCT: $V_M = 1.3 \text{ V}$; $V_I = GND \text{ to } 3 \text{ V}$.



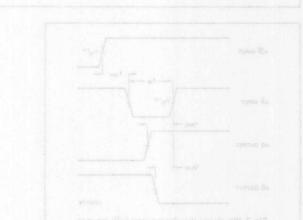


Fig. 7 Waveforms showing the reset (nR) input in output (nQ, nG) propagation delays, the reset pulse width and the nR to nGV removal time.

Vate to AC waveforms

1) HC: V_M = 50%, V_I = GND to V_{GC}

DUAL JK FLIP-FLOP WITH SET AND RESET; POSITIVE-EDGE TRIGGER

FEATURES

- J, K inputs for easy D-type flip-flop
- Toggle flip-flop or "do nothing" mode
- Output capability: standard
- · ICC category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT109 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT109 are dual positive-edge triggered, $J\overline{K}$ flip-flops with individual J, \overline{K} inputs, clock (CP) inputs, set (\overline{S}_D) and reset (\overline{R}_D) inputs; also complementary Ω and $\overline{\Omega}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and \overline{K} inputs control the state changes of the flip-flops as described in the mode select function table

The J and \overline{K} inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The $J\overline{K}$ design allows operation as a D-type flip-flop by tying the J and \overline{K} inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

			TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT	
^t PHL [/] ^t PLH	propagation delay nCP to nQ, nQ nSp to nQ, nQ nRp to nQ, nQ	C _L = 15 pF V _{CC} = 5 V	15 12 12	17 14 15	ns ns ns	
f _{max}	maximum clock frequency		75	61	MHz	
C ₁	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	22	pF	

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

f_i = input frequency in MHz f_o = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 f_{O} = output frequency in MHz VCC = supply voltage in V Σ (C_L x V_{CC}² x f_{O}) = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

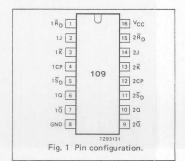
PACKAGE OUTLINES

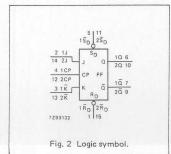
16-lead DIL; plastic (SOT38Z).

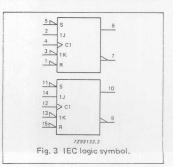
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	1RD, 2RD	asynchronous reset-direct input (active LOW)
2, 14, 3, 13	1J, 2J, 1K, 2K	synchronous inputs; flip-flops 1 and 2
4, 12	1CP, 2CP	clock input (LOW-to-HIGH, edge-triggered)
5, 11	1\$\overline{S}_D, 2\$\overline{S}_D	asynchronous set-direct input (active LOW)
6, 10	10, 20	true flip-flop outputs
7, 9	10, 20	complement flip-flop outputs
8	GND	ground (0 V)
16	Vcc	positive supply voltage







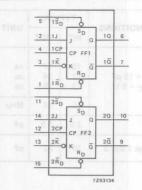


Fig. 4 Functional diagram.

FUNCTION TABLE

0000 471110 11000	propagato	OUTPUTS					
OPERATING MODE	Ī _D	\overline{R}_{D}	СР	J	K	Q	ā
asynchronous set	L	Н	X	X	X	н	L
asynchronous reset	Husel	L	X	X	X	L	Н
undetermined	LHJ9	L	X	X	X	Н	Н
toggle	Н	Н	1	Mh Te	ESGRI	q	q
load "0" (reset)	Hoose	Н	↑ bes	a deld	18 PO F	SHEDRI	H
load "1" (set)	н	Н	↑ mid	h	h	SCHO	STEL.
hold "no change"	н	Н	11100	ower Sc	h	m q	q

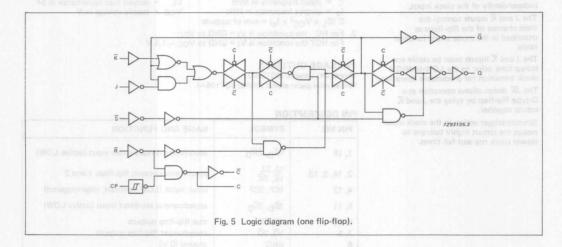
H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

 I = NGN voltage level
 I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
 q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition

X = don't care

↑ = LOW-to-HIGH CP transition



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: flip-flops

AC CHARACTERISTICS FOR 74HC with a month of the best flow and $\{g_0\}_{n=1}^{2}$ for the property of substances and $\{g_0\}_{n=1}^{2}$ for the property of the substance of the s

					T _{amb} (°C)				TEST CONDITIONS			
average.	DARAMETER				74HC				UNIT	V	WAVEFOR	Me	
SYMBOL	PARAMETER	+25			-40	-40 to +85		-40 to +125		V _{CC}	WAVEFOR		
		min.	typ.	max.	min.	max.	min.	max.			0.35		
tPHL/	propagation delay nCP to nQ, n $\overline{\mathbb{Q}}$		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6	C CHARA	
tPLH the	propagation delay nSD to nQ		30 11 9	120 24 20	P) an	150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 7		
^t PHL	propagation delay nSD to nQ	8514 A6m	41 15 12	155 31 26	orion-	195 39 33	35+ 1 - 684	235 47 40	ns	2.0 4.5 6.0	Fig. 7	TORWAS	
^t PHL	propagation delay nRD to nQ	Ea	41 15 12	185 37 31	5	230 46 39	2 05	280 56 48	ns	2.0 4.5 6.0	Fig. 7	F144 /1944	
^t PLH	propagation delay nRD to nQ	86	39 14 11	170 34 29		215 43 37	13 3	255 51 43	ns	2.0 4.5 6.0	Fig. 7	H.Jq ²	
tTHL/ tTLH	output transition time	83	19 7 6	75 15 13		95 19 16	0 01	110 22 19	ns	2.0 4.5 6.0	Fig. 6	789	
tw	clock pulse width HIGH or LOW	80 16 14	19 7 6	9	100 20 17	2	120 24 20		ns	2.0 4.5 6.0	Fig. 6	HJP	
tw	set or reset pulse width HIGH or LOW	80 16 14	14 5 4	9	100 20 17	ě	120 24 20		ns	2.0 4.5 6.0	Fig. 7	THE	
t _{rem}	removal time nSD, nRD to nCP	70 14 12	19 7 6		90 18 15		105 21 18	ai	ns	2.0 4.5 6.0	Fig. 7	NA.	
t _{su}	set-up time nJ, nK to nCP	70 14 12	17 6 5		90 18 15		105 21 18	ar	ns	2.0 4.5 6.0	Fig. 6	rren?	
^t h	hold time nJ, nK to nCP	5 5 5	0 0		5 5 5		5 5 5	81	ns	2.0 4.5 6.0	Fig. 6	tel	
f _{max}	maximum clock pulse frequency	6.0 30 35	22 68 81		5.0 24 28		4.0 20 24	27	MHz	2.0 4.5 6.0	Fig. 6	xem)	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: flip-flops

Note to HCT types

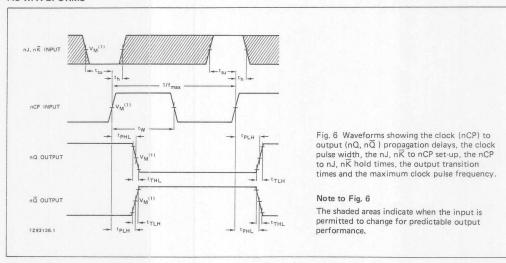
The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. The property of the determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nJ, nK	0.35
nRD	0.35
nSD	0.35
nCP	0.35

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	2.0 ns 4.5 Fig. 7	081		1 0	T _{amb} (°C)				velan	TEST CONDITIO	NS
	0.0	18		1 - 8	74H0	T O	9 2		UNIT		ou of Ogu	HJS
SYMBOL	PARAMETER	808	+25	86	-40	-40 to +85 -4		-40 to +125		VCC	WAVEFORMS	
	0.8	min.	typ.	max.	min.	max.	min.	max.			On of Older	. JHq2
t _{PHL} /	propagation delay nCP to nQ, nQ	280 56 48	20	35	14 4 6	44	14 p 15 p 17 p	53	ns	4.5	Fig. 6	JHS
^t PLH	propagation delay nSD to nQ	286	13	26	2	33	39	39	ns	4.5	Fig. 7	
[†] PHL	propagation delay	43	19	35	9	44	2 17	53	ns	4.5	Fig. 7	
^t PHL	propagation delay nRD to nQ	15 61	19	35		44	T B	53	ns ⁹ m	4.5	Fig. 7	HUTP
^t PLH	propagation delay		16	32	00	40	21 T	48	ns	4.5	Fig. 7006	W
tTHL/ tTLH	output transition time		700	15		19	N a	22	ns Alb	4.5	Fig. 6	
tW	clock pulse width HIGH or LOW	18	9		23		27	14	ns	4.5	Fig. 6	79
tw	set or reset pulse width HIGH or LOW	16	8		20		24	14	ns	4.5	Fig. 7	
^t rem	removal time $n\overline{S}_D$, $n\overline{R}_D$ to nCP	16	8		20		24	70 14 12	ns	4.5	Fig. 7	ns3
t _{su}	set-up time nJ, nK to nCP	18	8		23		27	8	ns	4.5	Fig. 6	
th	hold time nJ, nK to nCP	3	-3		3		3	5	ns	4.5	Fig. 6	
f _{max}	maximum clock pulse frequency	27	55		22		18	36	MHz	4.5	Fig. 6	xamil



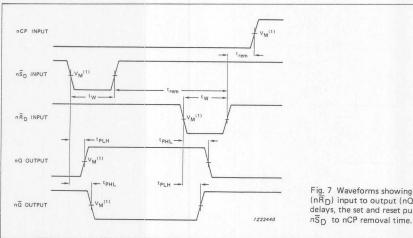
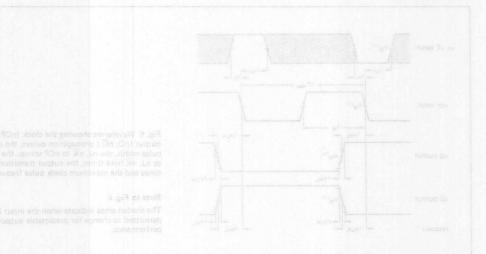
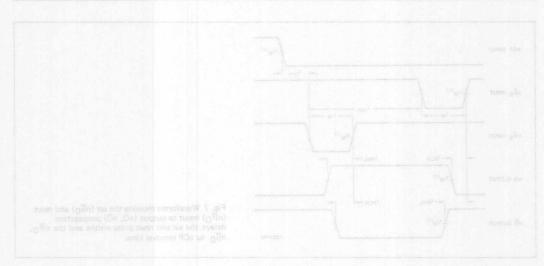


Fig. 7 Waveforms showing the set $(n\overline{S}_D)$ and reset $(n\overline{R}_D)$ input to output $(nQ, n\overline{Q})$ propagation delays, the set and reset pulse widths and the $n\overline{R}_D$, $n\overline{S}_D$ to nCP removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.





1) HG : V_M = 50%; V₁ = 6ND to V_{GC} HGT: V_M = 1,3 V; V₁ = 6ND to 3 V

DUAL JK FLIP-FLOP WITH SET AND RESET; NEGATIVE-EDGE TRIGGER

FEATURES

- Output capability: standard · Icc category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT112 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT112 are dual negativeedge triggered JK-type flip-flops featuring individual nJ, nK, clock (nCP), set (nSD) and reset (nRD) inputs. The set and reset inputs, when LOW, set or reset the outputs as shown in the function table at MC regardless of the levels at the other inputs.

A HIGH level at the clock (nCP) input enables the nJ and nK inputs and data will be accepted. The nJ and nK inputs control the state changes of the flip-flops as shown in the function table. The nJ and $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$ prior to the HIGH-to-LOW clock transition for predictable operation. Output state changes are initiated by the HIGH-to-LOW transition of nCP

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

	23841 NOH 2004		TYF	PICAL	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
tPHL/ tPLH	propagation delay nCP to nQ, nQ nSp to nQ, nQ nRp to nQ, nQ	C _L = 15 pF V _{CC} = 5 V	17 15 18	19 15 19	ns ns ns
f _{max}	maximum clock frequency	5 (B)	66	70	MHz
C ₁	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	27	30	pF

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

Notes of the community of the beautiful to

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

f; = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

nK inputs must be stable one set-up time 2. For HC the condition is $V_1 = GND$ to V_{CC} For HCT the condition is V_I = GND to V_{CC} - 1.5 V

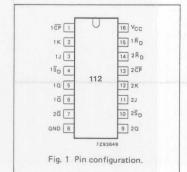
PACKAGE OUTLINES

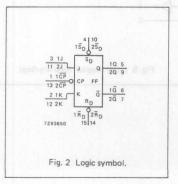
16-lead DIL; plastic (SOT38Z).

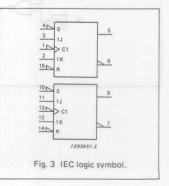
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1CP, 2CP	clock input (HIGH-to-LOW, edge triggered)
2, 12	1K, 2K	data inputs; flip-flops 1 and 2
3, 11	1J, 2J	data inputs; flip-flops 1 and 2
4, 10	15D, 25D	set inputs (active LOW)
5, 9	10, 20	true flip-flop outputs
6, 7	10, 20	complement flip-flop outputs
8	GND	ground (0 V)
15, 14	$1\overline{R}_D$, $2\overline{R}_D$	reset inputs (active LOW)
16	Vcc	positive supply voltage
	- 66	Lancotte Laboration and Control of the Control of t







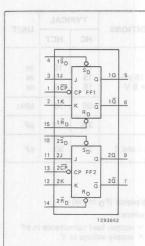


Fig. 4 Functional diagram.

FUNCTION TABLE

ASTEMATAN	JOSN	1 5.55	NPUTS			OUT	PUTS
OPERATING MODE	nSD	$n\overline{R}_D$	nCP	nJ	nK	nQ	ηQ
asynchronous set	LV	Н	×	×	×	H	L
asynchronous reset	Н	L	X	X	X	DE OF	Н
undetermined	L	sm L	X	X	X	H	o L
toggle	Н	Н	At ont	h	h	q	q
load "0" (reset)	Н	H	1 minutes	1 500	h	L	H
load "1" (set)	H	H	1	h	1 Lucia	Н	L
hold "no change"	H	Н	+	1	1	q	q

Note to function table

If $n\overline{S}_D$ and $n\overline{R}_D$ simultaneously go from LOW to HIGH, the output states will be unpredictable.

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition

L = LOW voltage level

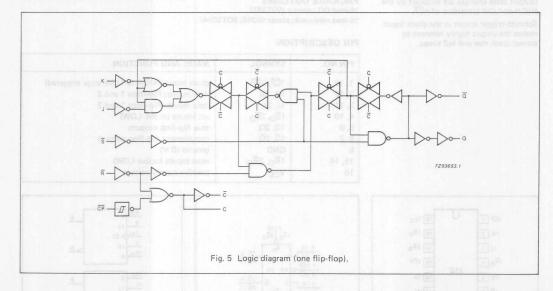
= LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition

q = lower case letters indicate the state of the referenced output one set-up time

prior to the HIGH-to-LOW CP transition

X = don't care

↓ = HIGH-to-LOW CP transition



DC CHARACTERISTICS FOR 74HC

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: flip-flops

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

	200000 010	MA 28519 1			T _{amb} ((°C)			min Avena	7111 (312)	TEST CONDITIONS
					74H	С				TH	NEUT COEFFICIE
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			K. 2K 0.6 Fig. 2Rg 0.65
tPHL/	propagation delay nCP to nQ		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
tPHL/	propagation delay nCP to nQ		55 20 16	175 35 30		220 44 37		265 53 45	ns ⁹ 9	2.0 4.5 6.0	Fig. 6
tPHL/	propagation delay nRD to nQ, nQ		58 21 17	180 36 31	TOP	225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 7
tPHL/	propagation delay nSD to nQ, nQ	125 13K	50 18 14	155 31 26	n. m	295 39. 33	25	235 47 40	ns	2.0 4.5 6.0	Fig. 7
tTHL/	output transition time	1	19 7 6	75 15 13	15.54	95 19 16	38	110 22 19	ns	2.0 4.5 6.0	Fig. 6
tw	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
tw	set or reset pulse width	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
^t rem	removal time	80 16 14	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7 HJT
^t rem	removal time	80 16 14	-19 -7 -6	TS .	100 20 17	22	120 24 20	r Bi	ns	2.0 4.5 6.0	Fig. 7
t _{su}	set-up time nJ, nK to nCP	80 16 14	19 7 6	be	100 20 17	25	120 24 20	1 08	ns	2.0 4.5 6.0	Fig. 6
t _h	hold time nJ, nK to nCP	0 0 0	-11 -4 -3	06 1	0 0	26	0 0 0	- 00 T at	ns	2.0 4.5 6.0	Fig. 6
f _{max}	maximum clock pulse frequency	6 30 35	20 60 71	0	4.8 24 28	0	4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6 blon

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: flip-flops

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1\$\overline{S}_D, 2\$\overline{S}_D\$ 1\$K, 2\$K 1\$\overline{R}_D, 2\$\overline{R}_D\$	0.5 0.6 0.65
1J, 2J 1CP, 2CP	1 0.

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	4.0	11.0			T _{amb} (°CI					TEST CONDITION	15
	2.0 4.5 Fig. 7	1	0		74HC		18.1	2		delay aG	Do at all e	ATH
SYMBOL	PARAMETER	26	+25		-40	to +85	-40 t	o +125	UNIT	VCC	WAVEFORMS	
	ns 4,5 Fig 7 6.0	min.	typ.	max.	min.	max.	min.	max.		dalay Ön	On or gan	HIJ9
t _{PHL} /	propagation delay nCP to nQ	2	21	35	10	44	17 8	53	ns	4.5	Fig. 6	
t _{PHL} /	propagation delay nCP to nQ		23	40	0	50	5	60	ns	4.5	Fig. 6	
t _{PHL} /	propagation delay nRD to nQ, nQ		22	37		46		56	ns	4.5	Fig. 7	16
t _{PHL} /	propagation delay $n\overline{S}_{\overline{D}}$ to $n\overline{Q}$		18	32	- 10	40		48	ns	4.5	Fig. 7	Į.
t _{THL} / t _{TLH}	output transition time		7	15	18	19		22	ns	4.5	Fig. 6	771.00
t _W	clock pulse width HIGH or LOW	16	8	27	20	S	24	08	ns	4.5	Fig. 6	
tw	set or reset pulse width LOW	18	10	20	23	20	27	- 61	ns	4.5	Fig. 7	me
t _{rem}	removal time	20	11	12	25		30	08 08 08	ns	4.5	Fig. 7	0
t _{rem}	removal time	20	-8		25	0	30	- 0	ns	4.5	Fig. 7	
t _{su}	set-up time nJ, nK to nCP	16	7	ō	20	0	24		ns	4.5	Fig. 6	
t _h	hold time nJ, nK to nCP	0	-7	(IC)	0	100	0	30 S	ns	4.5	Fig. 6	XBST
f _{max}	maximum clock pulse frequency	30	64		24		20		MHz	4.5	Fig. 6	

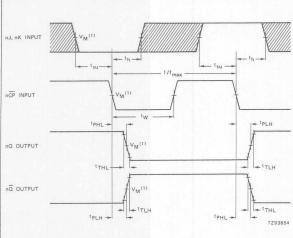


Fig. 6 Waveforms showing the clock ($n\overline{CP}$) to output (nQ, $n\overline{Q}$) propagation delays, the clock pulse width, the nJ, nK to $n\overline{CP}$ set-up times, the $n\overline{CP}$ to nJ, nK hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

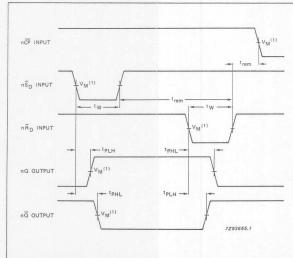
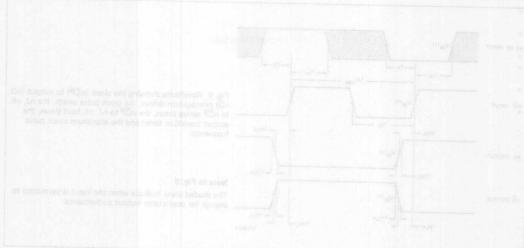


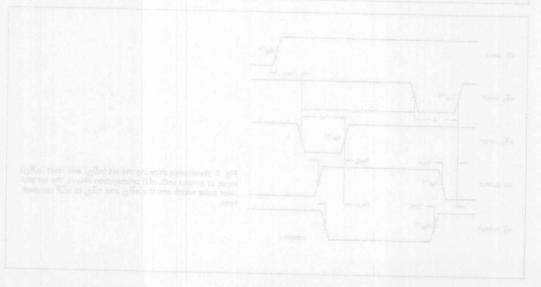
Fig. 7 Waveforms showing the set $(n\overline{S}_D)$ and reset $(n\overline{R}_D)$ input to output $(nQ, n\overline{Q})$ propagation delays, the set and reset pulse width and the $n\overline{R}_D$ and $n\overline{S}_D$ to $n\overline{CP}$ removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.







lore to AC wavelorms

1) HC: VM = 50%; VI = 6ND to Vcc

1) HC: VM = 12 VI VI = 6ND to 3 V

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

FEATURES

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- Output capability: standard (except for nR_{EXT}/C_{EXT})
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT123 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT123 are dual retriggerable monostable multivibrators with output pulse width control by three methods. The basic pulse time is programmed by selection of an external resistor (REXT) and capacitor (CEXT). The external resistor and capacitor are normally connected as shown in Fig. 6.

Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input (n $\overline{\rm A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ = HIGH, n $\overline{\rm A}$ = LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input n $\overline{\rm R}$ D, which also inhibits the triggering.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYF	PICAL	LIBILT
STWIBOL	FARAWETER 3	COMPLICING	нс	нст	UNIT
t _{PHL} /	propagation delay $n\overline{A}$, nB to nQ , $n\overline{Q}$ $n\overline{R}_D$ to nQ , $n\overline{Q}$	C _L = 15 pF V _{CC} = 5 V R _{EXT} = 5 kΩ C _{EXT} = 0 pF	26 20	26 23	ns ns
C ₁	input capacitance		3.5	3.5	pF T
C _{PD}	power dissipation capacitance per monostable	notes 1 and 2	54	56	pF

$$GND = 0 \text{ V}; T_{amb} = 25 \,^{\circ}\text{C}; t_r = t_f = 6 \text{ ns}$$

Notes

1. CpD is used to determine the dynamic power dissipation (PD in μ W):

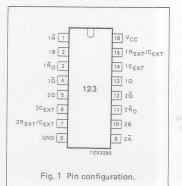
$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT}$$

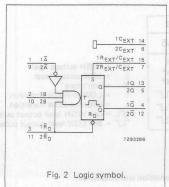
 $\times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$ where:

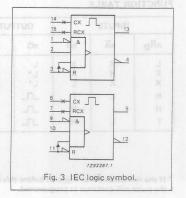
- f = input frequency in MHz
 - f_o = output frequency in MHz D = duty factor in %
- $\Sigma(C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} - 1.5 V

PACKAGE OUTLINES

- 16-lead DIL; plastic (SOT38Z).
- 16-lead mini-pack; plastic (SO16; SOT109A).





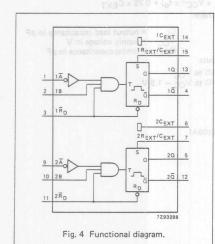


= output load capacitance in pF

VCC = supply voltage in V CEXT = timing capacitance in pF

PIN DESCRIPTION

PIN NO	0.	SYMBOL	NAME AND FUNCTION	
1, 9 2, 10	TOB	1Ā, 2Ā 1B, 2B	trigger inputs (negative-edge triggered) trigger inputs (positive-edge triggered)	1407
3, 11		1R _D , 2R _D	direct reset LOW and trigger action at positive edge outputs (active LOW)	
7 Fg		2REXT/CEXT	external resistor/capacitor connection	
8 13, 5		GND 1Q, 2Q	ground (0 V) outputs (active HIGH)	
14, 6 15		1C _{EXT} , 2C _{EXT} 1R _{EXT} /C _{EXT}	external capacitor connection external resistor/capacitor connection	
16		Vcc	positive supply voltage	



GENERAL DESCRIPTION (Cont'd)

An internal connection from nRD to the input gates makes it possible to trigger the circuit by a positive-going signal at input nRD as shown in the function table. Figures 7 and 8 illustrate pulse control by retriggering and early reset. The basic output pulse width is essentially determined by the values of the external timing components REXT and CEXT. For pulse widths, when CEXT < 10 000 pF, see Fig. 9.

When CEXT > 10 000 pF, the typical output pulse width is defined as:

 $t_W = 0.45 \times R_{EXT} \times C_{EXT}$ (typ.),

where, tw = pulse width in ns; $REXT = external resistor in k\Omega$; CEXT = external capacitor in pF.

Schmitt-trigger action in the nA and nB inputs, makes the circuit highly tolerant to slower input rise and fall times.

The '123' is identical to the '423' but can be triggered via the reset input.

FUNCTION TABLE

	INPUTS		OUTP	UTS
$n\overline{R}_{D}$	nĀ	nB	nQ	ηQ
L	×	X	L	Н
X	Н	X	L*	H*
×	X	L	L.	H*
Н	L	1	7	75
Н	1	Н	1	T
1	L	Н	1	7

= HIGH voltage level = LOW voltage level

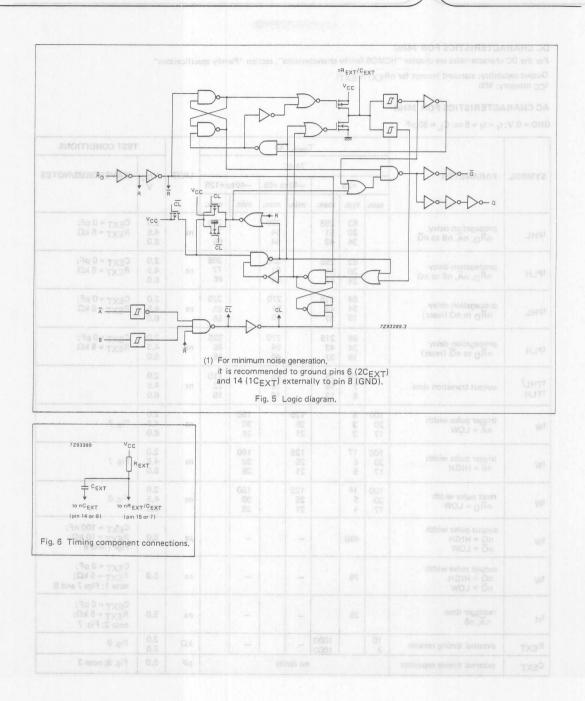
= don't care

= LOW-to-HIGH transition

= HIGH-to-LOW transition
= one HIGH level output pulse ☐ = one LOW level output pulse

* If the monostable was triggered before this condition was established, the pulse will continue as programmed.





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for nREXT/CEXT)

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

					Tamb (°C)	b				TEST CONDITIONS
OVIADOL	DADAUSTED A				74H	;			LIAUT		WAVEFORMS/NOTES
SYMBOL	PARAMETER		+25		-40 ·	to +85	-40 t	o +125	UNIT	VCC	WAVEFORMS/NOTES
ile ele		min.	typ.	max.	min.	max.	min.	max.	5		
^t PHL	propagation delay nRD, nA, nB to nQ		83 30 24	255 51 43		320 64 54	○ ~	385 77 65	ns	2.0 4.5 6.0	C _{EXT} = 0 pF; R _{EXT} = 5 kΩ
^t PLH	propagation delay nRD, nA, nB to nQ	E	83 30 24	255 51 43	J	320 64 54	4	385 77 65	ns	2.0 4.5 6.0	C _{EXT} = 0 pF; R _{EXT} = 5 kΩ
^t PHL	propagation delay nRD to nQ (reset)		66 24 19	215 43 37) <u>-</u>	270 54 46		325 65 55	ns	2.0 4.5 6.0	C _{EXT} = 0 pF; R _{EXT} = 5 kΩ
^t PLH	propagation delay nRD to nQ (reset)		66 24 19	215 43 37	menen	270 54 46	numirum	325 65 55	ns	2.0 4.5 6.0	C _{EXT} = 0 pF; R _{EXT} = 5 kΩ
^t THL [/] ^t TLH	output transition time	TX 3	19 7 6	75 15 13	to gre xtenna oaic di	95 19 16	regomi 14 (10	110 22 19	ns	2.0 4.5 6.0	
tw	trigger pulse width nA = LOW	100 20 17	8 3 2		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
tW	trigger pulse width nB = HIGH	100 20 17	17 6 5		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
tW	reset pulse width nRD = LOW	100 20 17	14 5 4		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
tW	output pulse width $nQ = HIGH$ $n\overline{Q} = LOW$		450		-		-		μs enoite	5.0	C _{EXT} = 100 nF; R _{EXT} = 10 kΩ; Figs 7 and 8
tw	output pulse width $nQ = HIGH$ $n\overline{Q} = LOW$		75		_		-		ns	5.0	C _{EXT} = 0 pF; R _{EXT} = 5 kΩ; note 1; Figs 7 and 8
t _{rt}	retrigger time nĀ, nB		26		-		-		ns	5.0	C _{EXT} = 0 pF; R _{EXT} = 5 kΩ; note 2; Fig. 7
REXT	external timing resistor	10 2		1000 1000	-		-		kΩ	2.0 5.0	Fig. 9
CEXT	external timing capacitor	J. T.			no lim	its			pF	5.0	Fig. 9; note 3

DC	CLIA	DACT	ED	CTICC	EOD	74HCT
D.C.	LHA	HALI	ER	121162	FUR	/4FTC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for nREXT/CEXT) ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

					_		
						UNIT LOAD	INPUT
						0.35 0.50	nĀ, nB nRD
propagation dalay nRp tunu (reset)							

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)					TEST CONDITIONS	
SYMBOL	DADAMETER				74HC	т			UNIT	Van	C WAVEFORMS/NOTES	
STIMBOL	PARAMETER office of the world side	+25			-40 to +85		-40 to +125		100000000000000000000000000000000000000		in jad 33 j v adiminish o	
		min.	typ.	max.	min.	max.	min.	max.				
^t PHL	propagation delay nRD, nA, nB to nQ		30	51		64		77	ns	4.5	$C_{EXT} = 0 pF;$ $R_{EXT} = 5 k\Omega$	
^t PLH	propagation delay nRD, nA, nB to nQ		28	51		64		77	ns	4.5	$C_{EXT} = 0 \text{ pF};$ $R_{EXT} = 5 \text{ k}\Omega$	
^t PHL	propagation delay		27	46		58		69	ns	4.5	C _{EXT} = 0 pF; R _{EXT} = 5 kΩ	
^t PLH	propagation delay $n\overline{R}_D$ to $n\overline{\Omega}$ (reset)		23	46		58		69	ns	4.5	C _{EXT} = 0 pF; R _{EXT} = 5 kΩ	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5		
tW	trigger pulse width nA = LOW	20	3		25		30		ns	4.5	Fig. 7	
tw	trigger pulse width nB = HIGH	20	5		25		30		ns	4.5	Fig. 7	
t _W	reset pulse width nRD = LOW	20	7		25		30		ns	4.5	Fig. 8	
tw	output pulse width $nQ = HIGH$ $n\overline{Q} = LOW$		450		-		-		μs	5.0	C_{EXT} = 100 nF; R_{EXT} = 10 k Ω ; Figs 7 and 8	
tW	output pulse width $n\underline{Q} = HIGH$ $n\overline{Q} = LOW$		75		-		_		ns	5.0	$C_{EXT} = 0 \text{ pF};$ $R_{EXT} = 5 \text{ k}\Omega;$ note 1; Figs 7 and 8	
^t rt	retrigger time nĀ, nB		40		-		-		ns	5.0	$C_{EXT} = 0 \text{ pF};$ $R_{EXT} = 5 \text{ k}\Omega;$ note 2; Fig. 7	
REXT	external timing resistor	2		1000	-		-		kΩ	5.0	Fig. 9	
CEXT	external timing capacitor				no lim	its			pF	5.0	Fig. 9; note 3	

Notes to AC characteristics

1. For other REXT and CEXT combinations see Fig. 9.

If $C_{EXT} > 10$ nF, the next formula is valid:

tW = K x REXT x CEXT (typ.)

where, tw = output pulse width in ns;

 $_{\rm EXT}$ = external resistor in k $_{\rm M}$; $_{\rm CEXT}$ = external capacitor in pF; $_{\rm K}$ = constant = 0.45 for $_{\rm VCC}$ = 5.0 V and 0.48 for $_{\rm VCC}$ = 2.0 V.

The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is approximately 7 pF. 2. The time to retrigger the monostable multivibrator depends on the values of $R_{\mbox{EXT}}$ and $C_{\mbox{EXT}}$.

The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time.

If $C_{EXT} > 10 \text{ pF}$, the next formula (at $V_{CC} = 5.0 \text{ V}$) for the set-up time of a retrigger pulse is valid:

$$t_{rt} = 35 + (0.11 \times C_{EXT}) + (0.04 \times R_{EXT} \times C_{EXT})$$
 (typ.)

= retrigger time in ns;

CEXT = external capacitor in pF;

 $R_{EXT} = external resistor in k\Omega$.

The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is approximately 7 pF.

3. When the device is powered-up, initiate the device via a reset pulse, when CEXT < 50 pF.

AC WAVEFORMS

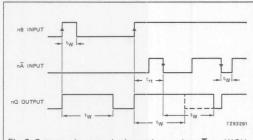


Fig. 7 Output pulse control using retrigger pulse; $n\overline{R}_D = HIGH$.

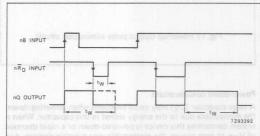


Fig. 8 Output pulse control using reset input $n\overline{R}_D$; $n\overline{A} = LOW$.

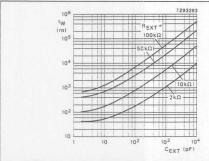


Fig. 9 Typical output pulse width as a function of the external capacitor values at V_{CC} = 5.0 V and T_{amb} = 25 °C.

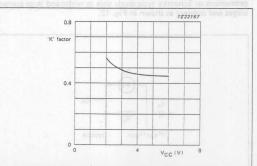


Fig. 10 HCT typical "k" factor as a function of VCC; $C_X = 10 \text{ nF}$; $R_X = 10 \text{ k}\Omega$ to $100 \text{ k}\Omega$.

APPLICATION INFORMATION

Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of $R_{\mbox{\scriptsize X}}$ and $C_{\mbox{\scriptsize X}}$, this output pulse can be eliminated using the circuit shown in Fig. 11.

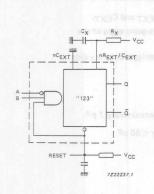


Fig. 11 Power-up output pulse elimination circuit.

Power-down considerations

A large capacitor $(C\chi)$ may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may substain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode $(D\chi)$ preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Fig. 12.

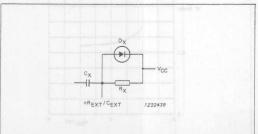


Fig. 12 Power-down protection circuit.



QUAD BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Output capability: bus driver
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT125 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT125 are four noninverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A HIGH at nOE causes the outputs to assume a HIGH impedance OFF-state.

The "125" is identical to the "126" but has active LOW enable inputs.

SYMBOL	PARAMETER	CONDITIONS	TY	UNIT		
	PARAMETER	CONDITIONS	нст	UNIT		
tpHL/ propagation delay tpLH nA to nY		C _L = 15 pF V _{CC} = 5 V		12	ns	
CI	input capacitance	4 50s A	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per buffer	notes 1 and 2	22	24	pF	

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

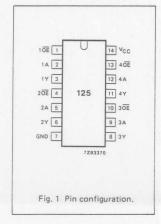
- f; = input frequency in MHz
- CL = output load capacitance in pF
- fo = output frequency in MHz VCC = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

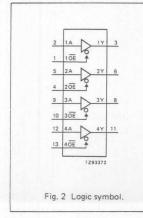
PACKAGE OUTLINES

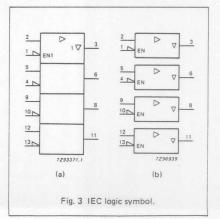
- 14-lead DIL; plastic (SOT27)
- 14-lead mini pack; plastic (SO14; SOT108A)

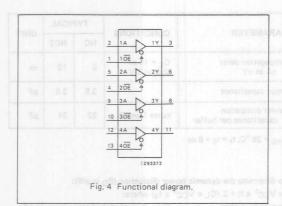
PIN DESCRIPTION

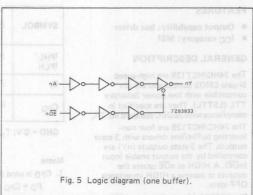
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	10E to 40E	output enable inputs (active LOW)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	Vcc	positive supply voltage











FUNCTION TABLE

INPL	JTS	OUTPUT
nŌĒ	nA	nY
L	L	L
L	Н	Н
Н	X	Z

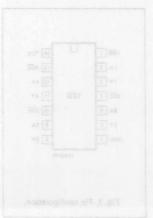
H = HIGH voltage level

Z = h	igh im	pedance	OFF-state

L = LOW voltage level X = don't care Z = high impedance OFF-state	







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

		T _{amb} (°C)								TEST CONDITIONS		
OVER DO L	242445				74H					Maion	COEF	
SYMBOL	PARAMETER	+25		5	-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.	з ланот	OS FO	CTERIST	
tPHL/	propagation delay nA to nY		30 11 9	100 20 17	0°) dim	125 25 21		150 30 26	ns ns	2.0 4.5 6.0	Fig. 6	(VD = GVi
^t PZH [/] 2MF	3-state output enable time nOE to nY	+125	41 15 12	125 25 21	7414C1 -40 to	155 31 26	-25	190 38 32	ns	2.0 4.5 6.0	Fig. 7	
^t PHZ [/]	3-state output disable time	max. 38	41 15 12	125 25 21	,aim	155 31 26	ryp.	190 38 32	ns	2.0 4.5 6.0	Fig. 7	Valent
^t THL [/]	output transition time	42	14 5 4	60 12 10		75 15 13	ar	90 18 15	ns' eld	2.0 4.5 6.0	Fig. 6	724) /HZd1
	ns 4.5 Fig. 7	38		178		8	ar		emiz pide		3-state out	YSHP

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

Note to HCT types

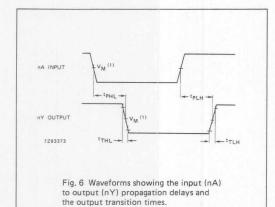
The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

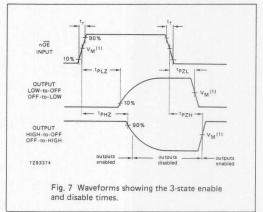
INPUT	UNIT LOAD COEFFICIENT
nA, nŌĒ	1.00 30V

AC CHARACTERISTICS FOR 74HCT North Company Com

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

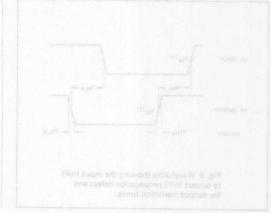
	0.8	58	T _{amb} (°C)				TEST CONDITIONS					
CVMPOL	2.0	1.90	OST 74HCT SCT 14							No. Total	WAVEFORMS	\H39 ²
SYMBOL	PARAMETER	38	+25		-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
	2.0	min.	typ.	max.	min.	max.	min.	max.	acola alci	alh sur	Burn state C	Version T
tPHL/	propagation delay nA to nY	38	15	25		31	S1	38	ns	4.5	Fig. 6	274
tPZH/ tPZL	3-state output enable time nOE to nY	81	15	28		35	5	42	ns smil	4.5	Fig. 7	UHT!
^t PHZ/ ^t PLZ	3-state output disable time nOE to nY		15	25		31		38	ns	4.5	Fig. 7	
tTHL/ tTLH	output transition time		5	12		15		18	ns	4.5	Fig. 6	

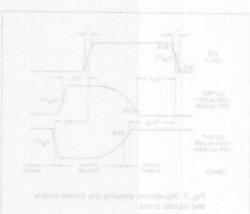




Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.





Note to AC waveforms
(1) HC : V_M = 50%; V_I = GND to V_{GC}
HCT: V₆₆ = 1.3 V; V_I = GND to 3 V

QUAD BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Output capability: bus driver
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT126 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The HC/HCT126 are four noninverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a HIGH impedance OFF-state.

The "126" is identical to the "125" but has active HIGH enable inputs.

SYMBOL	PARAMETER	CONDITIONS	TYF	UNIT		
STWIBUL	FARAMETER	CONDITIONS	нс	нст	UNIT	
tpHL/ propagation delay tpLH nA to nY		C _L = 15 pF V _{CC} = 5 V	9	11	ns	
CI	input capacitance	1 30S a	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per buffer	notes 1 and 2	23	24	pF	

GND = 0 V;
$$T_{amb} = 25 \,^{\circ}\text{C}$$
; $t_r = t_f = 6 \, \text{ns}$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD ×
$$VCC^2$$
 × f_i + Σ (CL × VCC^2 × f_0) where:

f; = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

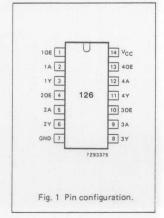
PACKAGE OUTLINES

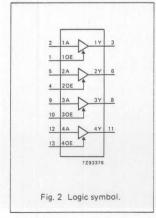
14-lead DIL; plastic (SOT27)

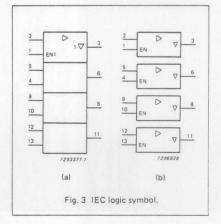
14-lead mini pack; plastic (SO14; SOT108A)

PIN DESCRIPTION

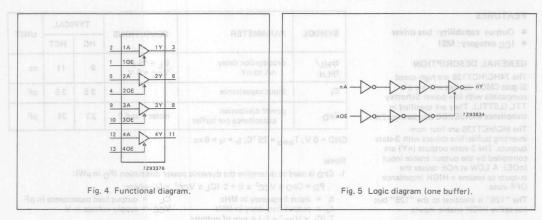
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	10E to 40E	output enable inputs (active HIGH)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	Vcc	positive supply voltage





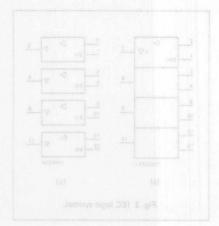


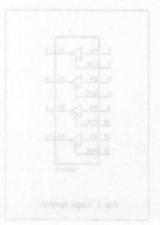
QUAD BUFFER/LINE DRIVER; 3-STATE

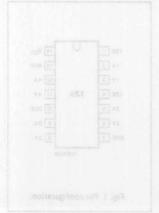


FUNCTION TABLE

INPUTS		OUTPUT	PACKAGE OUTLINES 4-lead-D1 Lipitario (80727)			
nOE	nA	nY	ead mini pack; ples tic (SO14; SOT108A)			
H H	L H	L H				
L	X	ditands and	MAN			
H = HIGH vo	oltage level	t enable inputs (a				
X = don't car	re					
Z = high imp	edance OFF	-state	o atsb			
			ristang			







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC and of moving at 5 to best from a vol. (2014) from the yielder processing tenderalists to suley set

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

AMETER agation delay	min.	+25 typ.	max.	74H0	to +85	-40 to	o +125 max.	UNIT	V _{CC} V	WAVEFO	RMS
agation delay	min.	typ.	max.					UNIT		WAVEFO	Aa
	min.	30		min.	max.	min.	max.				
			100								
		9	20	Plates	125 25 21		150 30 26	ns 900	2.0 4.5 6.0		ANAMO UN SNO = OVE
te output enable time DE to nY	821 ÷ 0	41 15 12	125 25 21	74HC	155 31 26	95%	190 38 32	ns	2.0 4.5 6.0	Fig. 7	SAMBOF
te output disable time DE to nY	MATE.	41 15 12	125 25 21	nin.	155 31 26	-099	190 38 32	ns	2.0 4.5 6.0	Fig. 7	Vision
ut transition time	88	14 5 4	60 12 10		75 15 13	13	90 18 15	ns	2.0 4.5 6.0	Fig. 6	/HZdz HTdz
	DE to nY te output disable time DE to nY ut transition time	te output disable time DE to nY ut transition time	te output enable time DE to nY 15 12 te output disable time DE to nY 15 15 12 41 15 12 41 15 12 41 15 12	te output enable time DE to nY 15 25 12 21 12 21 15 25 15 25 15 25 12 21 14 60 15 12 4 10 10 10 10 10 10 10 10 10 10 10 10 10	te output enable time DE to nY 15 25 12 21 12 15 15 25 15 25 15 25 15 25 12 21 14 60 5 12 4 10 10 10 10 10 10 10 10 10 10 10 10 10	te output enable time DE to nY 15 25 31 26 26 27 26 27 26 28 27 26 28 28 29 29 29 29 29 29 29 29 29 29 29 29 29	te output enable time DE to nY				

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Output capability: bus driver ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nOE	1.00

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_1 = 50 pF$

	0.8			Т	amb (°C)				1	TEST CONDI	TIONS
SYMBOL PARAMETER	2:0 ns 4:5 Eld 2	8E 74HCT est fa							UNIT	ane sudi	ngret 3-state out	
	PAHAMETER	+25			-40 to +85 -40 t			0 +125	Older	V _{CC}	WAVEFORMS	
	min.	typ.	max.	min.	max.	min.	max.	emir side		G-state ou		
tPHL/	propagation delay nA to nY	35	14	24		30	12	36	ns	4.5	Fig. 6	5.)41
tPZH/	3-state output enable time nOE to nY	ar ar	13	25 81		31 01	\$ \$	38	ns	4.5	Fig. 7	HUT
tPHZ/ tPLZ	3-state output disable time nOE to nY		18	28		35		42	ns	4.5	Fig. 7	
tTHL/	output transition time		5	12		15		18	ns	4.5	Fig. 6	

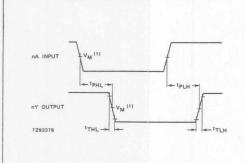


Fig. 6 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

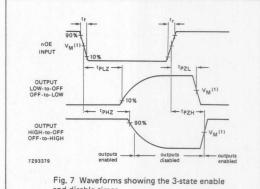
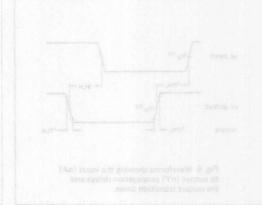


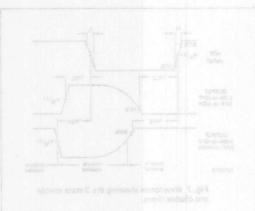
Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

STATE OF THE PERSON





Note to AC waveforms
(1) NC: V_M = 50%; V_I = 6ND to V_{CC}.
HCT: V_M = 1.3 V; V₁ = 6ND to 3 V.

QUAD 2-INPUT NAND SCHMITT TRIGGER

FEATURES

- Output capability: standard
- ICC category: SSI

GENERAL DESCRIPTION

The 74HC/HCT132 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT132 contain four 2-input NAND gates which accept standard input signals. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The gate switches at different points for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_T is defined as the hysteresis voltage V_H.

		CONDITIONS	TYF	PICAL	UNIT
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
t _{PHL} /	propagation delay nA, nB to nY	C _L = 15 pF V _{CC} = 5 V	11	.17	ns
CI	input capacitance	8 YS /	3.5	3.5	pF
CPD	power dissipation capacitance per gate	notes 1 and 2	24	20	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

- f; = input frequency in MHz fo = output frequency in MHz
- C_L = output load capacitance in pF V_{CC} = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

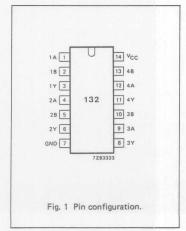
PACKAGE OUTLINES

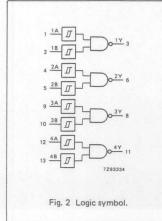
14-lead mini-pack; plastic (SO14; SOT108A).

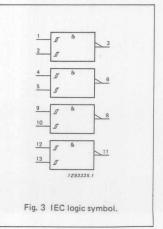
16-lead DIL; plastic (SOT38Z).

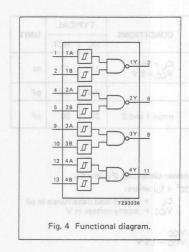
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTI	ON	
1, 4, 9, 12	1A to 4A	data inputs		
2, 5, 10, 13	1B to 4B	data inputs		
3, 6, 8, 11	1Y to 4Y	data outputs		
7	GND	ground (0 V)		AOT = T
14	Vcc	positive supply voltage	9	









7293337 Fig. 5 Logic diagram (one Schmitt trigger).

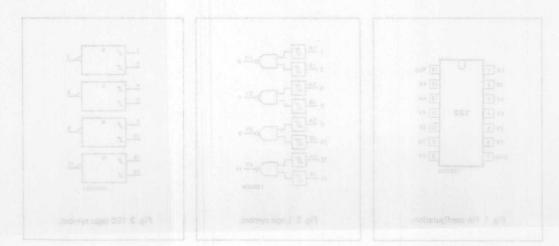
APPLICATIONS

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

FUNCTION TABLE

UTS	OUTPUT
nB	nY
L	es out House
Н	Н
L	Н
Н	L
	UTS nB L H L

INP	UTS	ОИТРИТ		: piario (SD14; SC (la (SDT382).	
nA	nB	nY			
L	L H	HINU	NAME AND E		
Н	L H	H	deta inputsi		
	H voltage level		studiuo area		
L = LOV	V voltage level				



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard ICC category: SSI

Transfer characteristics for 74HC

Voltages are referenced to GND (ground = 0 V). The voltages are referenced to GND (ground = 0 V).

					T _{amb} (°C)				-	TEST CONDITIO	
OVIMBOL	242445752				74	НС			UNIT	. 1	COEFFICIEN	
SYMBOL	SYMBOL PARAMETER	+25	+25		-40 to +85		-40 to +125		VCC	WAVEFORMS		
	min.	typ.	max.	min.	max.	min.	max.	T	r 74Hr			
V _{T+}	positive-going threshold	0.7 1.7 2.1	1.18 2.38 3.14	3.15	0.7 1.7 2.1	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	V tinuo	2.0 4.5 6.0	Figs 6 and 7	ltager si
V _T	negative-going threshold	0.3 0.9 1.2	0.63 1.67 2.26	2.2	0.3 0.9 1.2	1.0 2.2 3.0	0.3 0.9 1.2	1.0 2.2 3.0	v	2.0 4.5 6.0	Figs 6 and 7	JOSMY
VH	hysteresis (V _{T+} - V _T _)	0.2 0.4 0.6	0.55 0.71 0.88	1.4	0.2 0.4 0.6	1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	V	2.0 4.5 6.0	Figs 6 and 7	

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)					TEST CONDITIONS
SYMBOL	PARAMETER				74	НС			UNIT	V	WAVEFORMS
STINIBUL	PARAMETER		+25	yn j	-40	to +85	-40 t	o +125	UNIT	VCC	WAVEFORMS
_	min. typ. m	max.	min.	max.	min.	max.	3	Dē =	(D = 0 V; c _K = c _f = 6 ns; C		
tPHL/ tPLH	propagation delay nA, nB to nY	IVU	36 13 10	125 25 21	(3°) TOH	155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 13
t _{THL} / t _{TLH}	output transition time	3	19 7 6	75 15 13	100 +880 (mm)	95 19 16	Marri .	110 22 19	ns	2.0 4.5 6.0	Fig. 13

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard ICC category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD
nA, nB	0.3

Transfer characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

		I I		. 2.1	Tamb (°C)	2.4 4.2	18 11			TEST CONDITIONS
	2.0 Eqs 6 and 7	74HCT								.,	WAVEFORMS
SYMBOL	+25 -40 to +85 -40 to +125	UNIT	V _{CC}	WAVEFORMS							
2,0 4.5 Flos 6 and 7	min.	typ.	max.	min.	max.	min.	max.		eV -	TVI alaegorayri	
V _{T+}	positive-going threshold	1.2	1.41 1.59	1.9	1.2	1.9	1.2	1.9 2.1	٧	4.5 5.5	Figs 6 and 7
V _T _	negative-going threshold	0.5 0.6	0.85 0.99	1.2 1.4	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	٧	4.5 5.5	Figs 6 and 7
VH	hysteresis (V _{T+} - V _T _)	0.4 0.4	0.56		0.4	=	0.4 0.4	=	٧	4.5 5.5	Figs 6 and 7

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

SYMBOL PARAMETER 0.5 PARAMETER 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5	4,5 Fig. 13	T _{amb} (°C)								TEST CONDITIONS		
		10	38		74HCT 35 81				UNIT	Vcc	WAVEFORMS	
	+25			-40 to +85 -40 to +12			o +125	O. III	V	MAYE! ORIVIS		
	4,5 Fig. 13 6,0	min.	typ.	max.	min.	max.	min.	max.		onil n	H output transitio	
t _{PHL} /	propagation delay nA, nB to nY		20	33		41		50	ns	4.5	Fig. 13	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 13	

TRANSFER CHARACTERISTIC WAVEFORMS

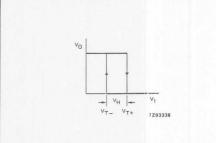
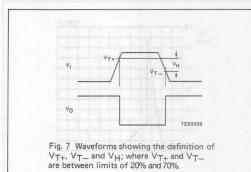


Fig. 6 Transfer characteristic.



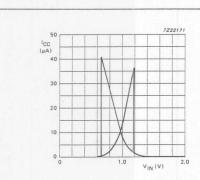


Fig. 8 Typical HC transfer characteristics; $V_{CC} = 2 \text{ V}$.

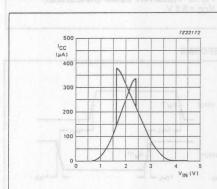


Fig. 9 Typical HC transfer characteristics; V_{CC} = 4.5 V.

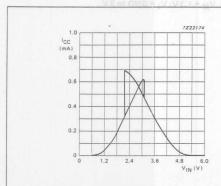


Fig. 10 Typical HC transfer characteristics; $V_{CC} = 6 \text{ V}$.

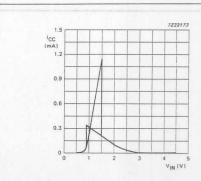


Fig. 11 Typical HCT transfer characteristics; V_{CC} = 4.5 V.

TRANSFER CHARACTERISTIC WAVEFORMS (Cont'd)

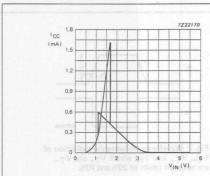


Fig. 12 Typical HCT transfer characteristics; $V_{CC} = 5.5 \text{ V}$.

AC WAVEFORMS

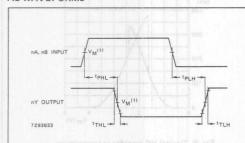
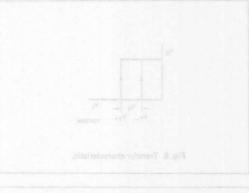
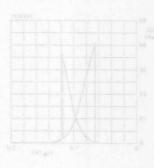


Fig. 13 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

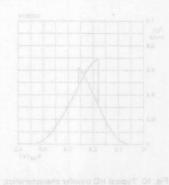




Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.

HCT: V_M = 1.3 V; V_I = GND to 3 V.



APPLICATION INFORMATION

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$$P_{ad} = f_i \times (t_r \times I_{CCa} + t_f \times I_{CCa}) \times V_{CC}$$

Where:

Pad = additional power dissipation (μ W)

= input frequency (MHz)

 $t_{\rm r}$ = input rise time (ns); 10% – 90% $t_{\rm f}$ = input fall time (ns); 10% – 90% $t_{\rm f}$ = average additional supply current (μ A)

Average $I_{\mbox{\scriptsize CCa}}$ differs with positive or negative input transitions, as shown in Figs 14 and 15.

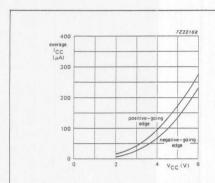


Fig. 14 Average I $_{\rm CC}$ for HC Schmitt trigger devices; linear change of V $_{\rm i}$ between 0.1 V $_{\rm CC}$ to 0.9 V $_{\rm CC}$.

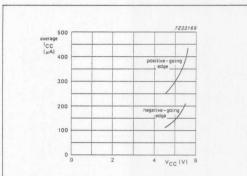


Fig. 15 Average I $_{\rm CC}$ for HCT Schmitt trigger devices; linear change of V $_{\rm i}$ between 0.1 V $_{\rm CC}$ to 0.9 V $_{\rm CC}$.

HC/HCT132 used in a relaxation oscillator circuit, see Fig. 16.

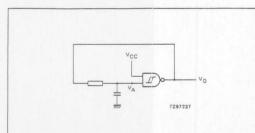


Fig. 16 Relaxation oscillator using HC/HCT132.

Note to Application information

All values given are typical unless otherwise specified.

Note to Fig. 16

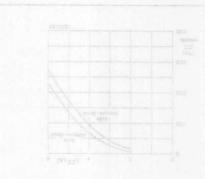
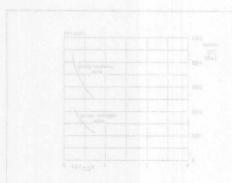
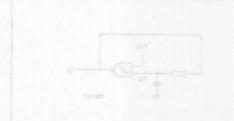


Fig. 14 Average ICC for HC Schmitt trigger devices;





74HC133

FEATURES

- · Output capability: standard
- I_{cc} category: SSI

GENERAL DESCRIPTION

The HC133 is an high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.

The 74HC133 provides the 13-input NAND function.

QUICK REFERENCE DATA

 $GND = 0 V; T_{amb} = 25^{\circ}C; t_r = t_f = 6 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t _{PHL} /t _{PLH}	propagation delay AM to Y	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	9	ns
Cı	input capacitance	gly	3.5	pF
C _{PD}	power dissipation per gate	notes 1 and 2	19	pF

Notes to the quick reference data

- 1. C_{pD} is used to determine the dynamic power dissipation (P_D in μ W) $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$ $f = \text{input fraguency in MHz} \cdot C_{CD} = \text{output load capacitance in p.F.}$
 - f_1 = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V;
- Σ (C_L x V_{CC}² x f_o) = sum of the outputs. 2. For HC the condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER		PACKAGES									
TYPE NUMBER	PINS	PIN POSITION	MATERIAL	CODE							
74HC133N	16	DIL	plastic	SOT38							
74HC133D	16	SO	plastic	SOT109A							

PINNING

PIN NO.	SYMBOL	NAME AND FUN	ICTION	×
17, 1015	AG, HM	data input	X	X
8	GND	ground (0 V)	TX	X
9	Y	data output		
16	V _{cc}	positive supply voltage	1 3	27

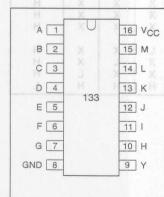
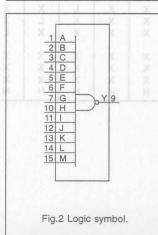
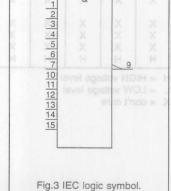
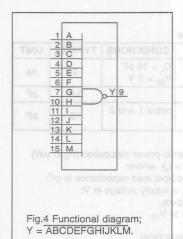


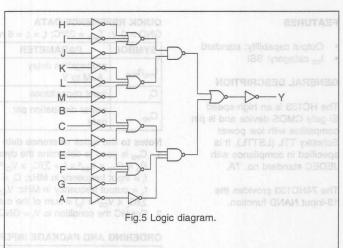
Fig.1 Pin configuration.





etsp СИАИ74HC133





FUNCTION TABLE TAM | MOTTEDS MIS EMIS

						INPUTS	3 1488						OUTPUT
A	ов	oli C la	D	E	F	G	H	DELT	J	K	L	M	Y
L	X	X	X	X	X	X	X	X	X	X	X	X	Н
X	L	X	X	X	X	X	X	X	X	X	X	X	Н
X	X	NO DAN	X	X	X	X	X	X	X	X	X	X	Н
X	X	X	L	TUCX S	X	X	AX	X	X	X	X	X	Н
X	X	X	X	0) Laur	X	X	X	X	X	X	X	X	Н
X	X	X	X	X	L	X	X	X	X	X	X	X	Н
X	X	X	X	X	X	L	X	X	X	X	X	X	Н
X	X	X	X	X	X	X	L	X	X	X	X	X	Н
X	X	X	X	X	X	X	X	L	X	X	X	X	Н
Χ	X	X	X	X	X	X	X	X	L	X	a X	X	H
X	X	X	X	X	X	X	X	X	X	LM	X	X	SH
X	X	X	X	X	X	X	X	X	X	X	L	X	Н
X	X	X	X	X	X	X	X	X	X	X	X	L	Н
Н	Н	Н	Н	Н	Н	H	Н	Н	Н	Hs	E H	Н	T A

H = HIGH voltage level L = LOW voltage level

X = don't care

otsp G/A 74HC133

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{cc} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_1 = 50 \text{ pF}$

					T _{amb} (°	JH	TEST CONDITIONS					
SYMBOL	PARAMETER	+25			-40 1	to +85	-40 to	-40 to +125		Vcc	WAVEFORMS	
		MIN.	TYP.			MAX.		MAX.		(V)	Fig. 6 Waveforms	
	tion delet	-	36	110	-	140	1-con	165	K.L.	2.0	C, D, E, F, G, H,	
	propagation delay AM to Y	-	13	22	-	28	-Jud	33	ns	4.5	Fig.6	
	AIVI to Y	-	10	19	-	23	-	28		6.0	transition times.	
	output transition	-	19	75	-	95	-	110		2.0		
T/T		-	7	15	-	19	-	22	ns	4.5	Fig.6	
	time	-	6	13	-	16	-	19		6.0		

74HC133

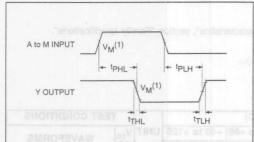


Fig.6 Waveforms showing the input (A, B, C, D, E, F, G, H, I, J, K, L, M) to output (Y) propagation delays and the output transition times.

Note to the AC waveforms

(1) HC: $V_M = 50\%$; $V_1 = GND$ to V_{CC} .

3-TO-8 LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES; INVERTING

FEATURES

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active LOW mutually exclusive
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT137 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT137 are 3-to-8 line decoder/demultiplexers with latches at the three address inputs (A_n). The "137" essentially combines the 3-to-8 decoder function with a 3-bit storage latch. When the latch is enabled (LE = LOW), the "137" acts as a 3-to-8 active LOW decoder. When the latch enable (LE) goes from LOW-to-HIGH, the last data present at the inputs before this transition, is stored in the latches. Further address changes are ignored as long as LE remains HIGH.

The output enable input $(\overline{E}_1 \text{ and } E_2)$ controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless \overline{E}_1 is LOW and E_2 is HIGH.

The "137" is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented

SYMBOL PARAMETER		1	TYP	LIBILT	
SYMBOL	20 a P	CONDITIONS	нс	нст	UNIT
^t PHL [/] ^t PLH	propagation delay An to \overline{Y}_n LE to \overline{Y}_n \overline{E}_1 to \overline{Y}_n E2 to \overline{Y}_n	C _L = 15 pF V _{CC} = 5 V	18 17 15 15	19 21 17 15	ns ns ns ns
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	57	59	pF

GND = 0 V; $T_{amb} = 25 \,^{\circ}\text{C}$; $t_r = t_f = 6 \, \text{ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x VCC^2 x f_i + Σ (CL x VCC^2 x f_o) where:

fi = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

fo = output frequency in MHz Σ (C_L x V_{CC}² x f₀) = sum of outputs

2. For HC the condition is VI = GND to VCC For HCT the condition is $V_I = GND$ to VCC - 1.5 V

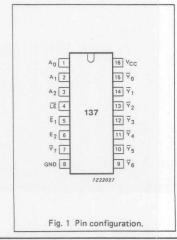
PACKAGE OUTLINES

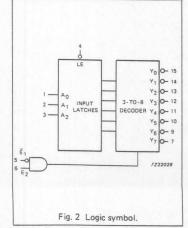
16-lead DIL; plastic (SOT38Z).

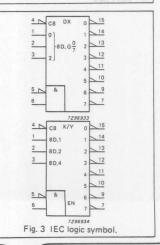
16-lead mini-pack; plastic (SO16; SOT109A).

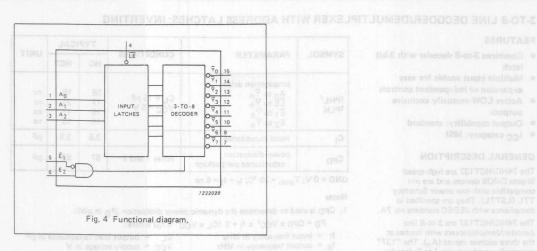
PIN DESCRIPTION H H H H H H H H

			200	4.7	
PIN NO.	SYMBOL	NAME AND FUNCTION			
1, 2, 3	An to A2	data inputs	Fi		1
4	LE H H H	latch enable input (active LOW)			
5	E ₁ H H H	data enable input (active LOW)			
6	E ₂ H H J	data enable input (active HIGH)			
8	GND	ground (0 V)			
15, 14, 13, 12, 11, 10, 9, 7	₹ ₀ to ₹ ₇	multiplexer outputs			
16	Vcc	positive supply voltage			







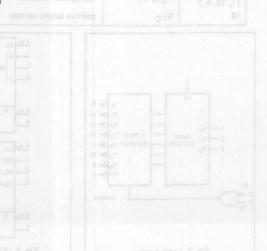


FUNCTION TABLE

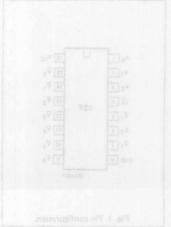
		INP	UTS			V	8.1	-07	TUC	PUT	3	V-ei	nodi	For HCT the core
LE	Ē ₁	E ₂	A ₀	A ₁	A ₂	\overline{Y}_0	\overline{Y}_1	\overline{Y}_2	₹3	₹4	₹5	\overline{Y}_6	₹7	PACKAGE OUTLI
Н	L	Н	X	X	X				sta	ble	roa;	aroi	3) siz	B-limid milni-park; pis
X	H X	X	X	X	X	Н	H	Н	Н	Н	Н	Н	Н	PIR DESCRIPTION
L	L	Н	L	LV	QIT	afic.	Н	н	н	Н	Н	н	Н	PIN NO.
L L		НН	H L H	H	LLL	H H	H H	H	H	H H H	H H	H	H	1,2,3 A
L L L		HHHH	L H L	LLHH	HHHH	1111	TTTT	TITI	1111		HLHH	HHLH	HHHL	3 8 3 8

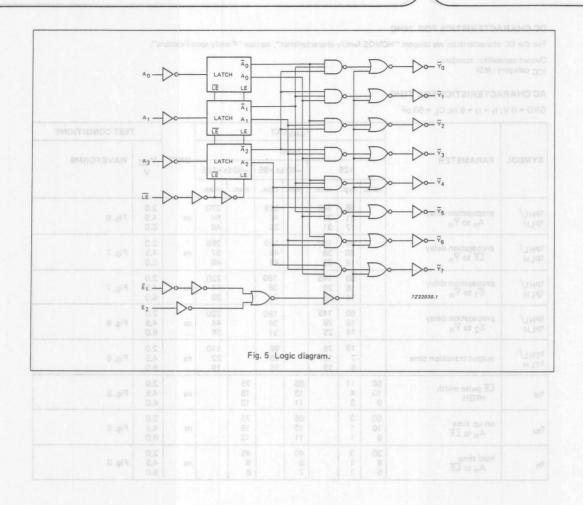
H = HIGH voltage level L = LOW voltage level

X = don't care









DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

				-	T _{amb} (°C)	24	52			TEST CONDITIONS
SYMBOL	PARAMETER	- CTE			74H	С			LINUT	.,	WAVEFORMS
STIMBUL			+25	-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
	.▼-∞<	min.	typ.	max.	min.	max.	min.	max.			
^t PHL [/]	propagation delay A_n to \overline{Y}_n		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 6
^t PHL/	propagation delay LE to ₹n		55 20 16	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 7
t _{PHL} /	propagation delay \overline{E}_1 to \overline{Y}_n		50 18 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
^t PHL/	propagation delay		50 18 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
tTHL/ tTLH	output transition time		19 7 6	75 15 13	gid dig	95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
tw	LE pulse width HIGH	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 8
t _{su}	set-up time A _n to LE	50 10 9	3 1 1		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 8
t _h	hold time A _n to LE	30 6 5	3 1 1		40 8 7		45 9 8		ns	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
An	1.50
E ₁	1.50
E ₂	1.50
LE	1.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

					T _{amb} (°C)				TEST CONDITIONS		
OVMDOL	DADAMETED				74HC	т	UNIT		TUSKI "A			
SYMBOL	PARAMETER	+25			-40	-40 to +85		-40 to +125		V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.	-			
tPHL/	propagation delay A _n to ∇ _n		22	38		48		57	ns	4.5	Fig. 6	
tPHL/ tPLH	propagation delay		25	44		55	nit blo	66	ns	4.5	Fig. 7	
tPHL/ tPLH	propagation delay		20	37		46	e pulso	56	ns	4.5	Fig. 7	
tPHL/ tPLH	propagation delay		18	35		44		- 53	ns	4.5	Fig. 6	
tTHL/ tTLH	output transition time	emisols	7	15	u	19	beztin	22	ns	4.5	Fig. 6	
tw	LE pulse width	10	5	: OH :	13		15	.9206	ns	4.5	Fig. 8	
t _{su}	set-up time A _n to LE	10	2		13		15		ns	4.5	Fig. 8	
^t h	hold time A _n to LE	7	2		9		11		ns	4.5	Fig. 8	

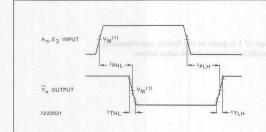
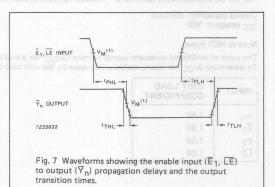
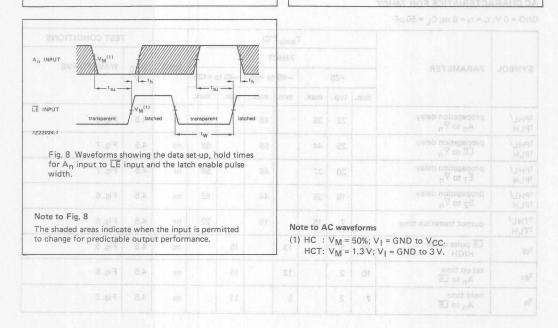
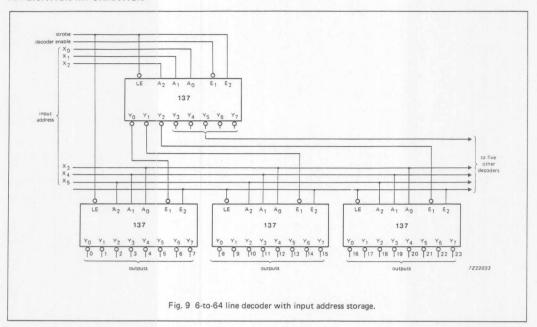


Fig. 6 Waveforms showing the address input (A_n) and enable inputs (E_2) to output (\overline{Y}_n) propagation delays and the output transition times.

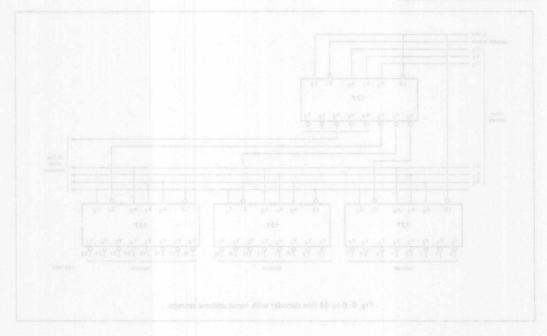




APPLICATION INFORMATION



APPLICATION INFORMATION



3-TO-8 LINE DECODER/DEMULTIPLEXER; INVERTING

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT138 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT138 decoders accept three binary weighted address inputs (A $_0$, A $_1$, A $_2$) and when enabled, provide 8 mutually exclusive active LOW outputs (\overline{Y}_0 to \overline{Y}_7).

The "138" features three enable inputs: two active LOW (\overline{E}_1 and \overline{E}_2) and one active HIGH (E_3). Every output will be HIGH unless \overline{E}_1 and \overline{E}_2 are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the "138" to a 1-of-32 (5 lines to 32 lines) decoder with just four "138" ICs and one inverter.

The "138" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The $^{\prime\prime}138^{\prime\prime}$ is identical to the $^{\prime\prime}238^{\prime\prime}$ but has inverting outputs.

SYMBOL PARAMETER		CONDITIONS	TYF	UNIT	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
tPHL/	propagation delay	C _L = 15 pF V _{CC} = 5 V	12	17	ns
tPHL/ tPLH	E ₃ to \overline{Y}_n	VCC = 5 V	14	19	ns
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	67	67	pF

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

 $PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$ where:

fi = input frequency in MHz fo = output frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC})^2 \times f_0 = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_CC

2. For HC the condition is $V_1 = GND$ to V_{CC} For HCT the condition is $V_1 = GND$ to $V_{CC} = 1.5$ V

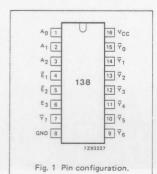
PACKAGE OUTLINES

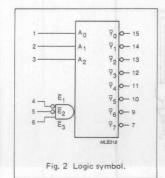
16-lead DIL; plastic (SOT38Z).

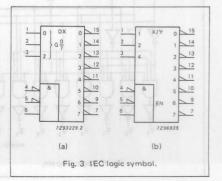
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3 4, 5 6 8	A ₀ to A ₂ E ₁ , E ₂ E ₃ GND	address inputs enable inputs (active LOW) enable input (active HIGH) ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	₹ ₀ to ₹ ₇	outputs (active LOW)
16	Vcc	positive supply voltage

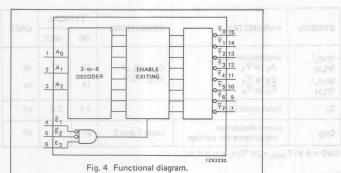






3-TO-8 LINE DECODER/DEMULTIPLEXER: INVERTING

Multiple input enable for easy



FUNCTION TABLE

		INF	UTS		ylqq	OUTPUTS In young									
Ē ₁	Ē ₂	E3	A ₀	A ₁	A ₂	\overline{Y}_0	\overline{Y}_1	\overline{Y}_2	\overline{Y}_3	\overline{Y}_4	\overline{Y}_5	\overline{Y}_6	¥7		
H	X	X	X	X	X	H	Н	Н	Н	Н	H	Н	Н		
Χ	Х	L	X	Χ	X	Н	Н	Н	Н	Н	Н	Н	Н		
L	L	Н	L	L	L	L	Н	Н	Н	Н	H	Н	Н		
L	L	Н	Н	L	L	H	L	Н	Hen	H	H	Н	H		
L	L	Н	L	Н	L	Н	Н	L	Н	Н	Н	Н	H		
L	L	Н	Н	Н	L	Н	Н	Н	L	Н	Н	Н	Н		
L	L	Н	L	L	н	н	Н	Н	Н	L	Н	н	Н		
L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	H	H		
L	L	Н	L	H	Н	Н	Н	Н	Н	Н	Н	L	Н		
L	L	Н	Н	H	Н	H	Н	Н	H	Н	H	Н	L		

85)

7A. vide

Z (CL x VCC 2. For HC the For HCT the PACKAGE OU

6-lead D1L, p 6-lead mini-p

H=HIGH voltage level L=LOW voltage level

X = don't care

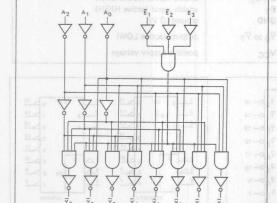
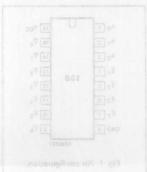


Fig. 5 Logic diagram.

7793231.1



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Output capability: standard I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

							T _{amb} (°C)				TEST CONDITIONS		
				74HC								TMB	COEFFICE	TOTAL
SYMBOL	PARAMETER			+25			-40	to +85	-40 t	-40 to +125		V _{CC}	WAVEFORMS	IS NA
				min.	typ.	max.	min.	max.	min.	max.			1.00	
^t PHL [/] ^t PLH	propagation A_n to \overline{Y}_n	delay			41 15 12	150 30 26		190 38 33		225 45 38	ns Age	2.0 4.5 6.0	Fig. 6	
t _{PHL} /	propagation E ₃ to \overline{Y}_n	delay			47 17 14	150 30 26	to") d	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} /	propagation En to Yn		TNU	925 1934	47 17 14	150 30 26	H 57 08	190 38 33	225 VD. 100	225 45 38	ns	2.0 4.5 6.0	Fig. 7	TOBMAS
^t THL/ ^t TLH	output transi	tion time	20	83	19 7 6	75 15 13	4.6	95 19 16	es o	110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7	H74s /TH4s
	Fig. 6	4.5	an	08			80		8 40			vslab	propagation Eg to Vn	H74; /3H4;

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
An	1.50
En	1.25 V
E ₃	1.00

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

			225		- 0	T _{amb} (°C)				TEST CONDITIONS		
			BE			74HC	т	26 26				WA OT ES. HTL	
SYMBOL PAR	PARAMETER		+25			-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS	
			min.	typ.	max.	min.	max.	min.	max.				HUS
t _{PHL} /	propagation delay A_n to \overline{Y}_n	20	110	20	35	19	44	75	53	ns	4.5	Fig. 6	\unit
tPHL/ tPLH	propagation delay E ₃ to \overline{Y}_n			18	40		50		60	ns	4.5	Fig. 6	
tPHL/ tPLH	propagation delay \overline{E}_n to \overline{Y}_n			19	40		50		60	ns	4.5	Fig. 7	
tTHL/ tTLH	output transition time			7	15		19		22	ns	4.5	Figs 6 and 7	

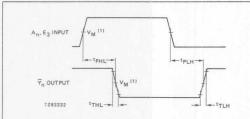


Fig. 6 Waveforms showing the address input (A_n) and enable input (E3) to output (\overline{Y}_n) propagation delays and the output transition times.

$\overline{\epsilon}_1, \overline{\epsilon}_2$ INPUT $V_M^{(1)}$ $V_M^{(1)}$ 7293233 v_{THL}

Fig. 7 Waveforms showing the enable input (\overline{E}_n) to output (\overline{Y}_n) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

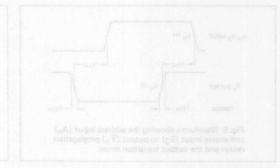




Fig. 7. Waveforms showing the enable input $\{\vec{E}_n\}$ to couput $\{\vec{Y}_n\}$ propagation delays and the output rewritten times

impotavaw SA er stol/

(1) HC: V_M = 50%; V₁ = GND to V_G HCT: V_M = 1.3 V; V₁ = GND to 3 V

DUAL 2-TO-4 LINE DECODER/DEMULTIPLEXER

FEATURES

- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT139 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT139 are high-speed, dual 2-to-4 line decoder/demultiplexers. This device has two independent decoders, each accepting two binary weighted inputs (nA₀ and nA₁) and providing four mutually exclusive active LOW outputs $(n\overline{Y}_0 \text{ to } n\overline{Y}_3)$. Each decoder has an active LOW enable input

When nE is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

The "139" is identical to the HEF4556 of the HE4000B family.

APPLICATIONS

- Memory decoding or data-routing
- Code conversion

	FUNCTION	CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	нс	нст	Olvii	
tPHL/	propagation delay $ \begin{matrix} nA_n \text{ to } n\overline{Y}_n \\ n\overline{E} \text{ to } n\overline{Y}_n \end{matrix} $	C _L = 15 pF V _{CC} = 5 V	11 10	13 13	ns ns	
CI	input capacitance	5 T T T T T T T T T T T T T T T T T T T	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	42	44	pF	

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

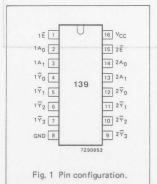
- f; = input frequency in MHz fo = output frequency in MHz
- CL . = output load capacitance in pF VCC = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is VI = GND to VCC
- For HCT the condition is $V_I = GND$ to $V_{CC} 1.5 V$

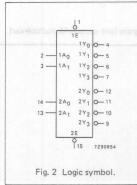
PACKAGE OUTLINES

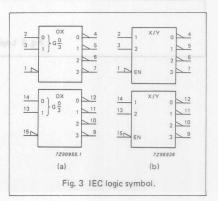
16-lead DIL; plastic (SOT38Z). 16-lead mini-pack; plastic (SO16; SOT109A).

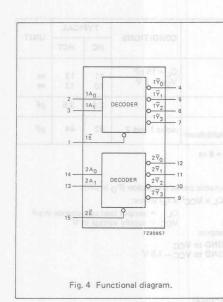
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	1Ē, 2Ē	enable inputs (active LOW)
2,3	1A ₀ , 1A ₁	address inputs
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	outputs (active LOW)
8	GND	ground (0 V)
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	outputs (active LOW)
14, 13	2A ₀ , 2A ₁	address inputs
16	Vcc	positive supply voltage









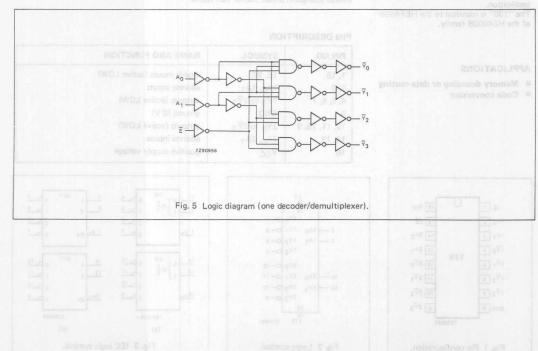
FUNCTION TABLE

		INPUTS	MILE !	OUTPUTS							
	nĒ	nA ₀	nA ₁	n∀0	n₹1	n₹2	n₹3				
1	Н	X	X	Н	Н	H a	uqHo				
	L juq	L H L	L L	L H H	H 18	H L	H H				
	L	Н	O9H	Н	Н	H	HEM				

H = HIGH voltage level

L = LOW voltage level

X = don't care



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC Set of the set

						Tamb	°C)				0	TEST CONDITI	ONS
SYMBOL	PARAMETER					74H	С			LINUT	.,	WAVEFORMS	
STIVIBUL	PANAMETER			+25		-40 t	to +85	-40 t	0 +125	UNIT	V _{CC}	WAVEFORMS	IAn B
			min.	typ.	max.	min.	max.	min.	max.				
^t PHL/ ^t PLH	propagation d nA _n to \overline{Y}_n	lelay		39 14 11	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6	RAHO ON NO = 0 V
^t PHL/	propagation d	lelay		33 12 10	135 27 23	(0°) (170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 7	
t _{THL} / t _{TLH}	output transit		25	7	75 15 13	8+ pr 0	19	am l.g	110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7	
		4.5	2/1	8		43		6 34	ı		yslet	propagation on the Potential of the Potential	/1H93

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	COEFFICIEN
1An	0.70
1A _n 2A _n	0.70
nĒ"	1.35

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	8.0 1.5 Fig. 7		305		C	T _{amb} (°C)				ystal	TEST CONDITIONS
SYMBOL			74HCT 85 01								.,	NAMES OF ALIS
SYMBOL	PARAMETER		10	+25		-40 t	o +85	-85 -40 to +125	UNIT	V _{CC}	WAVEFORMS	
	4.5 Figs 6 and 7 6,0		min.	typ.	max.	min.	max.	min.	max.		ER INDE	
tPHL/ tPLH	propagation delay nA _n to \overline{Y}_n			16	34		43		51	ns	4.5	Fig. 6
t _{PHL} /	propagation delay			16	34		43		51	ns	4.5	Fig. 7
tTHL/ tTLH	output transition t	ime		7	15		19		22	ns	4.5	Figs 6 and 7

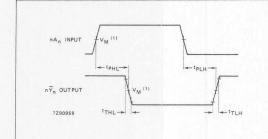


Fig. 6 Waveforms showing the address input (nA_n) to output $(n\overline{Y}_n)$ propagation delays and the output transition times.

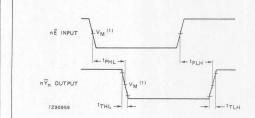
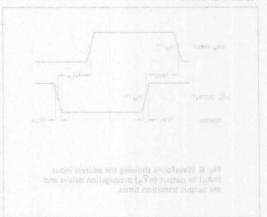


Fig. 7 Waveforms showing the enable input (n \overline{E}) to output (n \overline{Y}_n) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.



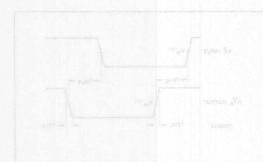


Fig. 7. Waveforms showing the enable input (not output (n \overline{V}_{n}) propagation dalays and the output transition times.

Note to AC waveforms

(1) HC: V_M = 50%; V_i = GND to V_{CC} HCT: V_M = 1.3 V; V_i = GND to 3 V.

10-TO-4 LINE PRIORITY ENCODER

FEATURES

- Encodes 10-line decimal to 4-line BCD
- Useful for 10-position switch encoding
- Used in code converters and generators
- Output capability: standard
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT147 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT147 9-input priority encoders accept data from nine active LOW inputs $(\overline{A}_0$ to $\overline{A}_8)$ and provide a binary representation on the four active LOW outputs $(\overline{Y}_0$ to $\overline{Y}_3)$. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line \overline{A}_8 having the highest priority.

The devices provide the 10-line to 4-line priority encoding function by use of the implied decimal "zero". The "zero" is encoded when all nine data inputs are HIGH, forcing all four outputs HIGH.

OV/MED CI	OADAMETED.	CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	ns	
tPHL/ tPLH	propagation delay \overline{A}_n to \overline{Y}_n	C _L = 15 pF V _{CC} = 5 V	15	17		
Cl	input capacitance	9 9	3.5	3.5	pF	
CPD power dissipation capacitance per package		notes 1 and 2	30	33	рF	

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x VCC^2 x f_i + Σ (CL x VCC^2 x f_o) where:

fi = input frequency in MHz fo = output frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to VCC

For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 \text{ V}$

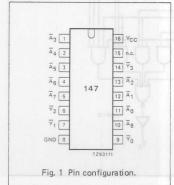
PACKAGE OUTLINES

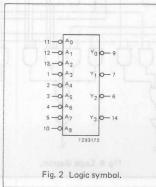
16-lead DIL; plastic (SOT38Z).

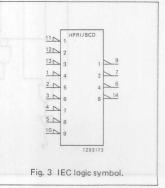
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9, 7, 6, 14	\overline{Y}_0 to \overline{Y}_3	BCD address outputs (active LOW)
11, 12, 13, 1, 2, 3, 4, 5, 10	\overline{A}_0 to \overline{A}_8	decimal data inputs (active LOW)
15	n.c.	not connected
16	Vcc	positive supply voltage







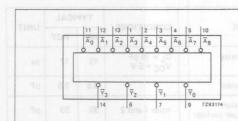


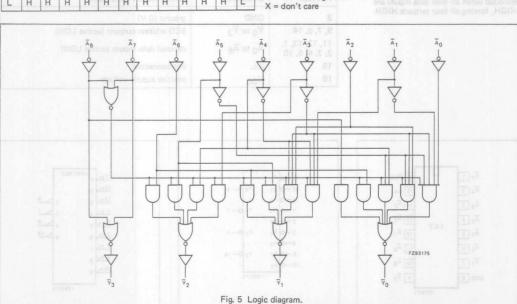
Fig. 4 Functional diagram.

- Useful for 10-position switch

FUNCTION TABLE

	k fg	PUTS	OUT	Vx.	- 200	(ot)	neriv.	S	NPUT	11			
	\overline{Y}_0	\overline{Y}_1	\bar{Y}_2	\bar{Y}_3	Ā8	Ā7	\overline{A}_{6}	\overline{A}_{5}	Ā ₄	Ā ₃	\overline{A}_2	Ā ₁	\overline{A}_0
	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
For HCT the control of the control o	L H L H	H H L	HHLL	L H H	L H H	X L H	X L H	X X X L	X X X	X X X	X X X	X X X	X X X
H = HIGH voltage le	L H L	H H L	L H H	H H H	H H H	H H H	HHHH	нннн	LHHH	X L H	X X L	X X X L	X X X
L = LOW voltage let X = don't care	L	H	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

H = HIGH voltage level L = LOW voltage level



DC CHARACTERISTICS FOR 74HC

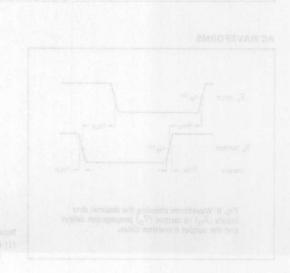
For the DC characteristics see chapter."HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

					T _{amb} (°C)				TEST CONDITIONS			
SVMPOL P	SYMBOL PARAMETER	74HC								VIII	WAVEFORMS		
SAMBOL		+25			-40 1	to +85	-40 t	-40 to +125		V _{CC}			
		min.	typ.	max.	min.	max.	min.	max.					
tPHL/	propagation delay Ā _n to ∀ _n		50 18 14	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6		
t _{THL} /	output transition time		19 7 6	75 15 6		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6		



DC CHARACTERISTICS FOR 74HCT

11

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{\underline{A}}_{3}, \overline{\underline{A}}_{4}, $	1.50
$\overline{\underline{A}}_{5}, \overline{\underline{A}}_{6}, $	1.10

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V; } t_r = t_f = 6 \text{ ns; } C_L = 50 \text{ pF}$

SYMBOL PARAMETER					T _{amb} (TEST CONDITIONS					
	DADAMETER				UNIT	.,	WAVEFORMS					
SAMBOL	PARAMETER		+25			-40 to +85		-40 to +125		V _{CC}		
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/ tPLH	propagation delay \overline{A}_n to \overline{Y}_n		20	35		44		53	ns	4.5	Fig. 6	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 6	

AC WAVEFORMS

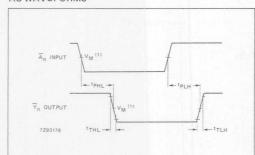


Fig. 6 Waveforms showing the decimal data inputs (\overline{A}_n) to output (\overline{Y}_n) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

8-INPUT MULTIPLEXER

FEATURES

- True and complement outputs
- Multifunction capability
- Permits multiplexing from n lines to 1 line
- Non-inverting data path
- See the "251" for the 3-state version
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT151 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

	FUNCTION TABLE		TYF			
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT	
tpHL/ tPLH	propagation delay In to Y, \(\overline{Y} \) Sn to Y, \(\overline{Y} \) E to \(\overline{Y} \)	C _L = 15 pF V _{CC} = 5 V	17 19 12 14	19 20 13 18	ns ns ns	
C _I	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	40	40	pF	

 $GND = 0 \text{ V}; T_{amb} = 25 \,^{\circ}\text{C}; t_r = t_f = 6 \text{ ns}$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD × VCC^2 × f_i + Σ (CL × VCC^2 × f_o) where:

 $\begin{array}{lll} f_1 &=& \text{input frequency in MHz} & & \text{CL} &=& \text{output load capacitance in pF} \\ f_0 &=& \text{output frequency in MHz} & & \text{VCC} &=& \text{supply voltage in V} \end{array}$

- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$ 2. For HC the condition is VI = GND to VCC
- For HCT the condition is $V_I = GND$ to VCC 1.5 V

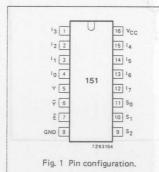
PACKAGE OUTLINES

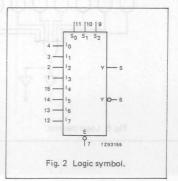
16-lead DIL; plastic (SOT38Z).

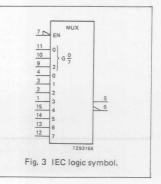
16-lead mini-pack; plastic (SO16; SOT109A).

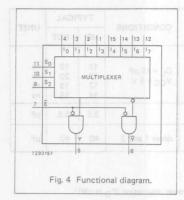
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	10 to 17	multiplexer inputs
5	Y	multiplexer output
6	Y	complementary multiplexer output
7	Ē	enable input (active LOW)
8	GND	ground (0 V)
11, 10, 9	So, S1, S2	select inputs
16	S ₀ , S ₁ , S ₂ VCC	positive supply voltage







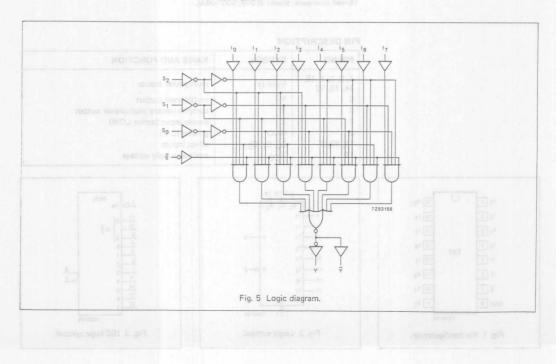


FUNCTION TABLE

	B	BLSW	PERA	11	INP	JTS		Mil	grub)	memi	lama	оит	PUTS
Ē	S ₂	S ₁	S ₀	10	11	12	13	14	15	16	17	Y	Y
Н	X	X	X	X	X	X	X	X	X	X	X	Н	de e
L L L	L	L	LHH	L H X X	X X L H	X X X	X X X	X X X	X X X	X X X	X X X	H L H L	L H L H
L L L	E O	H H H	L H H	X X X	× × ×	H X X	X X L H	X X X	X X X	× × ×	X X X	H L H L	L H L
L L L	H H H	L D L D L	L H H	X X X	××××	× × ×	X X X	L H X	X X L	× × ×	× × ×	H L H L	H L H
LLLL	H H H	H H H	L H H	X X X	X X X	X X X	X X X	X X X	X X X	L H X	X X L H	H L H L	L H L

H = HIGH voltage level L = LOW voltage level

X = don't care



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)					TEST CONDIT	ONS
					74HC	:	UNIT	V	WAVEFORMS			
SYMBOL	PARAMETER		+25			-40 to +85		-40 to +125		V _{CC}	WAVEFORMS	5
		min.	typ.	max.	min.	max.	min.	max.			1.50	100
tPHL/	propagation delay I _n to Y		52 19 15	170 34 29		215 43 37	10.99	255 51 43	ns TOMA	2.0 4.5 6.0	Fig. 6	
tPHL/	propagation delay I _n to ₹		58 21 17	185 37 31	(3°)	230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 6	.v e = qv
tPHL/	propagation delay S _n to Y	23	61 22 18	185 37 31	13H 3+ or 0	230 46 39	83	280 56 48	ns	2.0 4.5 6.0	Fig. 7	TORMA
tPHL/	propagation delay S_n to \overline{Y}	,98	61 22 18	205 41 35	600 J.A	255 51 43	SE 3	310 62 53	ns	2.0 4.5 6.0	Fig. 7	VIH9
^t PHL/ ^t PLH	propagation delay E to Y		41 15 12	125 25 21	84-	155 31 26	86 5	190 38 32	ns	2.0 4.5 6.0	Fig. 7	\168 H17
tPHL/	propagation delay 톤 to Ÿ		47 17 14	145 29 25	18	180 36 31	14 8	220 44 38	ns	2.0 4.5 6.0	Fig. 7	PER
^t THL/ ^t TLH	output transition time		19 7 6	75 15 13	88	95 19 16	88 7	110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7	PLH.

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I _n S _n	0.45 1.50 0.30

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_1 = 50 pF$

	4.5 Fig. 6	ET 8	T _{amb} (°C)							YETE	TEST CONDITION	IS
	0.5	74HCT								.,	WAVEFORMS	
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC	WAVEFORING	
	2.0	min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay In to Y	21 8	22	38	13	48	35	57	ns	4.5	Fig. 6	HIL
t _{PHL} / t _{PLH}	propagation delay I_{n} to \overline{Y}	20 3	22	38	1E 3E	48	28 28 21 21	57	ns	4.5	Fig. 6	HT. /TH.
tPHL/ tPLH	propagation delay S _n to Y	105	23	41		51	14	62	ns	4.5	Fig. 7	
tPHL/	propagation delay S_n to \overline{Y}	0.2	25	43	ae a	54	75	65	ns	4.5	Fig. 7	THE PERSON NAMED IN COLUMN
tPHL/ tPLH	propagation delay E to Y		16	29		36	13	44	ns	4.5	Fig. 7	HU
t _{PHL} /	propagation delay E to Y		21	36		45		54	ns	4.5	Fig. 7	
t _{THL} /	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7	

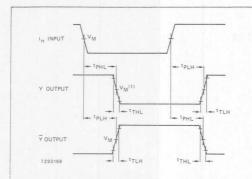


Fig. 6 Waveforms showing the multiplexer input (I_n) to outputs (Y and $\overline{Y})$ propagation delays and the output transition times.

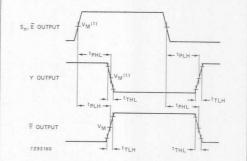


Fig. 7 Waveforms showing the select input (S_n) and enable input (\overline{E}) to outputs (Y and $\overline{Y})$ propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

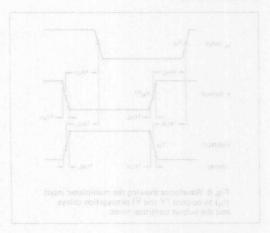




Fig. ? Waveforms showing the select input (S_n) and enable input (E) to outputs (Y and Y) opposition delays and the output banking of the output (Y and Y)

DUAL 4-INPUT MULTIPLEXER

FEATURES THE PARTY OF THE PARTY

- Non-inverting outputs
- · Separate enable for each output
- Common select inputs
- See '253" for 3-state version
- Permits multiplexing from n lines to 1 line
- · Enable line provided for cascading (n lines to 1 line)
- Output capability: standard
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT153 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT153 have two identical 4-input multiplexers which select two bits of data from up to four sources selected by common data select inputs (S_0, S_1) . The two 4-input multiplexer circuits have individual active LOW output enable inputs (1E, 2E) which can be used to strobe the outputs independently. The outputs (1Y, 2Y) are forced LOW when the corresponding output enable inputs are HIGH.

The "153" is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to So and S1.

The logic equations for the outputs are:

$$1\mathsf{Y} = 1\overline{\mathsf{E}}.(11_0.\overline{\underline{\mathsf{S}}}_1.\overline{\mathsf{S}}_0 + 11_1.\overline{\mathsf{S}}_1.\mathsf{S}_0 +$$

+112.S₁.S₀+113.S₁.S₀)

 $\begin{array}{c} 2\mathsf{Y} = \ 2\overline{\mathsf{E}}. (2\mathsf{I}_0.\overline{\mathsf{S}}_1.\overline{\mathsf{S}}_0 + 2\mathsf{I}_1.\overline{\mathsf{S}}_1.\mathsf{S}_0 + \\ + 2\mathsf{I}_2.\mathsf{S}_1.\overline{\mathsf{S}}_0 + 2\mathsf{I}_3.\mathsf{S}_1.\mathsf{S}_0) \end{array}$

(continued on next page)

		CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	нс нст		UNIT	
^t PHL [/] ^t PLH	propagation delay 11 _n , 21 _n to nY Sn to nY nE to nY	C _L = 15 pF V _{CC} = 5 V	14 15 10	16 17 11	ns ns ns	
C ₁	input capacitance		3.5	3.5	pF	
CPD power dissipation capacitance per multiples		notes 1 and 2	30	30	pF	

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

f; = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF

VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is VI = GND to VCC For HCT the condition is $V_1 = GND$ to VCC - 1.5 V

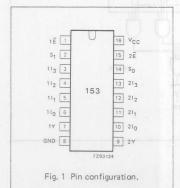
PACKAGE OUTLINES

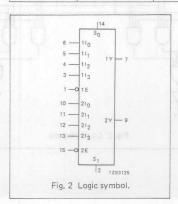
16-lead DIL; plastic (SOT38Z).

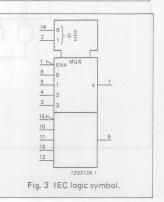
16-lead mini-pack; plastic (SO16; SOT109A).

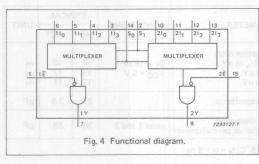
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15 14, 2 6, 5, 4, 3 7 8 9 10, 11, 12, 13	1E, 2E S ₀ , S ₁ 1l ₀ to 1l ₃ 1Y GND 2Y 2l ₀ to 2l ₃	output enable inputs (active LOW) common data select inputs data inputs from source 1 multiplexer output from source 1 ground (0 V) multiplexer output from source 2 data inputs from source 2 positive supply voltage









FUNCTION TABLE

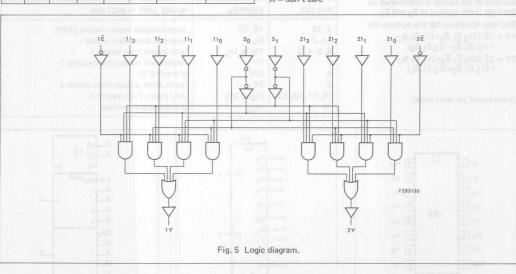
SEL		[DATA	INPUT	Sw fol	OUTPUT	ОИТРИТ	
S ₀	s ₁	nlo	nlı	nl ₂	nl3	ηĒ	M nY	
X	X	X	X	X	X	ооу н аиз	= (VL) ne	
L	L	L	X	X	X	L L	L IV 21 (18)	
L	L	Н	X	X	X	L	Н	
Н	L	X	L	X	X	L	L 8	
Н	L	X	Н	X	X	L	Hose	
L	Н	X	X	L	X	- L	L L	
L	Н	X	X	Н	X	L	Н	
Н	Н	I X X X L		L	L	L		
H	Н	X	X	X	Н	L	Н	

H = HIGH voltage level
L = LOW voltage level
X = don't care

GENERAL DESCRIPTION

The "153" can be used to move data to a common output bus from a group of registers. The state of the select inputs would determine the particular register from which the data came. An alternative application is a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

The "153" is similar to the "253" but has standard outputs.



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C₁ = 50 pF

							T _{amb} (°C)					TEST CONDIT	IONS
0.4501	240445755						74H				UNIT	TM	WAVEFORM	TU9M
SYMBOL	PARAMETER	•		+25			-40 to +85		-40 to +125		UNIT	V _{CC}	0.45	
				min.	typ.	max.	min.	max.	min.	max.			0.60	ne en
^t PHL/ ^t PLH	propagation d 1I _n to nY; 2I _n to nY	elay			47 17 14	145 29 25		180 36 31		220 44 38	ns 73H4	2.0 4.5 6.0	Fig. 6	
^t PHL [/]	propagation d	elay			50 18 14	150 30 26	(03)	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	(V-0 = UV
^t PHL/ ^t PLH	propagation d	elay	Tilve	as	33 12 10	100 20 17	7.0k	125 25 21	8	150 30 26	ns	2.0 4.5 6.0	Fig. 7	JOSMY
tTHL/ tTLH	output transit	ion time	20	7.5	19 7 6	75 15 13	E(I)	95 19 16	34	110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7	PHI
													21 _D to nY	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". In section "HCMOS family characteristics are chapter and the section of the property o

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
11 _n , 21 _n	0.45
1I _n , 2I _n	0.60
Sn	1.35

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

		an 8	14 16		T _{amb} (°C)		18		Yasa	TEST CONDITION	IS
CVMPOL	PARAMETER 02	74HCT							UNIT			
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
^t PHL	propagation delay 1I _n to nY; 2I _n to nY	20 3	19	34	18	43	18	51	ns	4.5	Fig. 6	HTI.
^t PLH	propagation delay 1I _n to nY; 2I _n to nY		13	24		30		36	ns	4.5	Fig. 6	
t _{PHL} /	propagation delay S _n to nY		20	34		43		51	ns	4.5	Fig. 7	
^t PHL/ ^t PLH	propagation delay nE to nY		14	27		34		41	ns	4.5	Fig. 7	
t _{THL} /	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7	

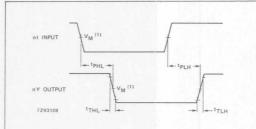


Fig. 6 Waveforms showing the input $(11_n, 21_n)$ to output (1Y, 2Y) propagation delays and the output transition times.

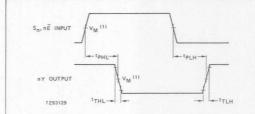


Fig. 7 Waveforms showing the select input (S0, S1) and the output enable input (\overline{E}) to output (1Y, 2Y) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.





Note to AC waveforms

[1] HC : V_M = SUB; V₁ = GND to V_{GC}

4-TO-16 LINE DECODER/DEMULTIPLEXER

FEATURES

- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- 2-input enable gate for strobing or expansion
- Output capability: standard
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT154 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT154 decoders accept four active HIGH binary address inputs and provide 16 mutually exclusive active LOW outputs.

The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for the expansion of the decoder.

The enable gate has two AND'ed inputs which must be LOW to enable the outputs.

The "154" can be used as a 1-to-16 demultiplexer by using one of the enable inputs as the multiplexed data input.

When the other enable is LOW, the addressed output will follow the state of the applied data.

SYMBOL	PARAMETER	CONDITIONS	TYF	UNIT		
STINIBUL	PARAMETER	CONDITIONS	НС	нст	ONT	
$\frac{tPHL^{\prime}}{PLH}$ propagation delay $A_{n}, E_{n} to Y_{n}$		C _L = 15 pF V _{CC} = 5 V	11	13	ns	
CI	input capacitance		3.5	3.5	pF	
C _{PD} power dissipation capacitance per package		notes 1 and 2	60	60	pF	

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

fi = input frequency in MHz f_O = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

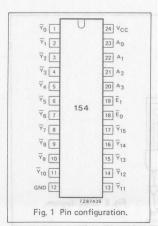
2. For HC the condition is VI = GND to VCCFor HCT the condition is VI = GND to VCC - 1.5 V

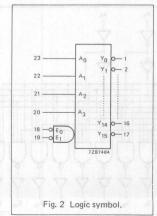
PACKAGE OUTLINES

24-lead DIL; plastic (SOT101A). 24-lead mini-pack; plastic (SO24; SOT137A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION								
1, 2, 3, 4, 5, 6,	BBBB	H H H H J J H		1						
7, 8, 9, 10, 11,	\overline{Y}_0 to \overline{Y}_{15}	H H H H H H H H H H H H H H H H H H H								
13, 14, 15, 16,	10 to 115	outputs (active LOW)								
17										
18, 19	\overline{E}_0 , \overline{E}_1	enable inputs (active LOW)								
12	GND	ground (0 V)								
23, 22, 21, 20	A ₀ to A ₃	address inputs								
24	VCC	positive supply voltage								





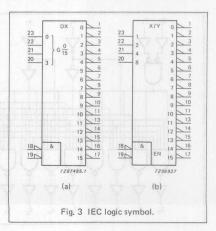




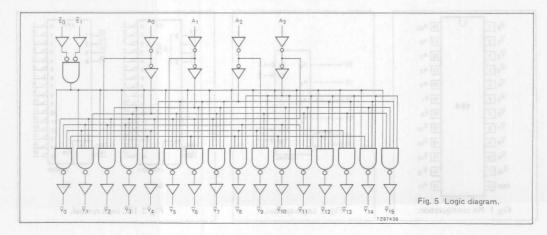
Fig. 4 Functional diagram.

FUNCTION TABLE

			INP	UTS									01	JTPU	TS						
Ē ₀	Ē1	A ₀	A1	A ₂	А3	\overline{Y}_0	\overline{Y}_1	\bar{Y}_2	₹ ₃	\overline{Y}_4	₹ ₅	\overline{Y}_6	₹ ₇	₹8	₹ ₉	₹ ₁₀	₹ ₁₁	₹12	₹ ₁₃	₹ ₁₄	₹ ₁₅
H H L	H L H	X X X	X X X	X X	X X X	Н	H H H	H H	H H H	H H	H H H	HH	H H H	HHH	HHH	H H	H H	H VIII H	H	H sv H sb ii H u g	H
	L L L	L H L	L H H	L L L	L∀ L L	H H H	H L H H	H H L H	H H L	HHHH	HHHH	HHHH	HHHH	HHHH	HHH	H H H	H H H	H H H H	H H H	H H H	H H H
L L L	L L L	L H L	L H H	H H H	L L L	H H H	H H H	H H H H	H H H	L H H H	HLHH	H H L	HHHL	HHHH	ннн	H H H H	H H H	H H H	HHHH	H H H H	H H H
L L L	L L L	L H L	L L H	L L L	нннн	H H H	H H H	H H H	H H H	HHHH	H H H	H H H	H H H H	LHHH	H L H	H H L H	H H L	H H H	H H H	H bo	H H H
		L H L	L H H	H H H	H H H H	H H H	H H H	HHHH	H H H	ННН	ННН	НННН	HHHH	HHHH	H H H	HHHH	НННН	L H H	H L H H	H H L H	H H L

H = HIGH voltage level L = LOW voltage level

X = don't care



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

					r _{amb} (°C)				TEST CONDITIONS		
		74HC								TVIST	UN14309	
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/	propagation delay A _n to \overline{Y}_n		36 13 10	150 30 26		190 38 33		225 45 38	ns ag	2.0 4.5 6.0	Fig. 6	
t _{PHL} /	propagation delay \overline{E}_n to \overline{Y}_n		39 14 11	150 30 26	(3°) _{di}	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
tTHL/ tTLH	output transition time	129	19 7 6	75 15 13	- 01 (1)	95 19 16	899	110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

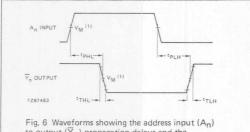
The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
An BM	1.0 VAW 30

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

				T _{amb} (°C)								TEST CONDITIONS			
			18			74HCT						1 01 112	HJS		
SYMBOL PARAMETI	2.0	011	+25			-40 to +85 -40 to -		o +125	UNIT	V _{CC}	WAVEFORMS				
	6.0		min.	typ.	max.	min.	max.	min.	max.			HJ			
tPHL/ tPLH	propagation A _n to ₹			16	35		44		53	ns	4.5	Fig. 6			
tPHL/	propagation E _n to \overline{Y}_r			15	32		40		48	ns	4.5	Fig. 7			
tTHL/	output trans	ition time		7	15		19		22	ns	4.5	Figs 6 and 7			



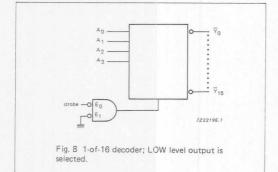


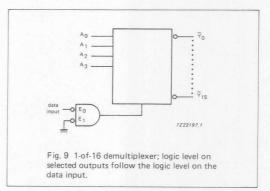
Yn OUTPUT 7287482 Fig. 7 Waveforms showing the enable input $(\overline{\mathbb{E}}_n)$ to output (\overline{Y}_n) propagation delays and the output transition times.

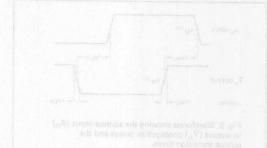
Note to AC waveforms

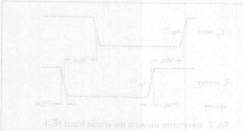
(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

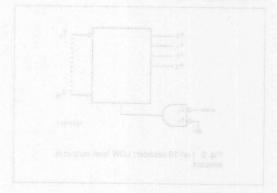
APPLICATION INFORMATION

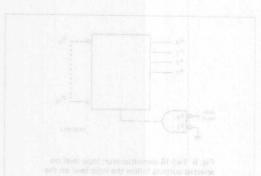












QUAD 2-INPUT MULTIPLEXER

FEATURES

- Non-inverting data path
- Output capability: standard
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT157 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT157 are quad 2-input multiplexers which select 4 bits of data from two sources under the control of a common data select input (S). The four outputs present the selected data in the true (non-inverted) form. The enable input (Ē) is active LOW. When Ē is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the "157". The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

The device is usefull for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The "157" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations are:

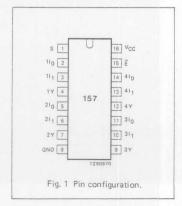
 $1Y = \overline{E}.(11_1.S + 11_0.\overline{S})$

 $2Y = \overline{E}.(21_1.S + 21_0.\overline{S})$

 $3Y = \overline{E}.(31_1.S + 31_0.\overline{S})$

 $4Y = \overline{E}.(41_1.S + 41_0.\overline{S})$

The "157" is identical to the "158" but has non-inverting (true) outputs.



AT MOITS		CONDITIONS	TYF	LINUT	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
^t PHL [/] ^t PLH	propagation delay nlo, nl1 to nY E to nY S to nY	C _L = 15 pF V _{CC} = 5 V	11 11 12	13 12 19	ns ns ns
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	70	70	pF

VCC = supply voltage in V

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

 $PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$ where:

f; = input frequency in MHz CL = output load capacitance in pF

fo = output frequency in MHz

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

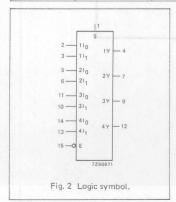
PACKAGE OUTLINES

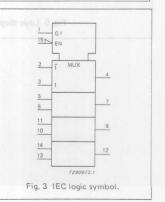
16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	
1	S	common data select input	
2, 5, 11, 14	11 ₀ to 41 ₀	data inputs from source 0	
3, 6, 10, 13	11 ₁ to 41 ₁	data inputs from source 1	
4, 7, 9, 12	1Y to 4Y	multiplexer outputs	
8	GND	ground (0 V)	
15	E 35 -00	enable input (active LOW)	
16	Vcc	positive supply voltage	





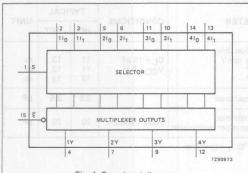


Fig. 4 Functional diagram.

FUNCTION TABLE

	IN	IPUTS	abrasta ayaifi	OUTPUT
Ē	S	nlo	nl ₁	YIOMNYO
Н	X	X	×	ZAHE HETTS
L L	L	L H	×	te CMOS days of the Little of the Heat The
L	H	×	L DEC	H H

H = HIGH voltage level L = LOW voltage level

X = don't care

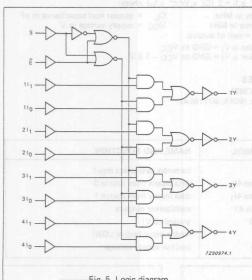


Fig. 5 Logic diagram.



DC CHARACTERISTICS FOR 74HC (1980) VINTER TO MOSTORE CONTRIBUTION OF THE PROPERTY OF THE PROPE

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC and said in review 1 to beet this a not (2012) the rough young respective to solve and

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

		T _{amb} (°C)								TEST CONDITIONS		
0)44001	DADAMETER				74HC	;			UNIT	V	WAVEFORM	ie oln
SYMBOL PARAMETER min		+25		-40 t	-40 to +854		-40 to +125		V _{CC}	WAVEFORMS	i in	
		min.	typ.	max.	min.	max.	min.	max.			1.00	
^t PHL/ ^t PLH	propagation delay nI ₀ to nY; nI ₁ to nY		36 13 10	125 25 21		155 31 26		190 38 32	ns Hat	2.0 4.5 6.0	Fig. 7	
t _{PHL} / ^{AO}	propagation delay E to nY		39 14 11	115 23 20	io") a	145 29 25		175 35 30	ns	2.0 4.5 6.0	Fig. 6	
^t PHL/ ^t PLH	propagation delay S to nY	125 125 118X	41 15 12	125 25 21	e of D	155 31 26	25 25 m	190 38 32	ns	2.0 4.5 6.0	Fig. 7	TOSMA
^t THL/ ^t TLH	output transition time	l n	19 7 6	75 15 13	34	95 19 16	8 2	110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7	/JH¢

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LO	
nlo a	1.00	
nl 1 E	0.60	

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		75 1 116		- 8	T _{amb} (°C)				yelso	TEST CONDITION	VS
		100			74HC	т	1 20				71101 3	HIS
SYMBOL	PARAMETER	0.00	+25	a	-40 t	o +85	-40 to	+125	UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			Yatora	
tPHL/	propagation delay nI ₀ to nY; nI ₁ to nY	61 15 10 10	16	27	96 91	34	9 75 31 15	41	ns Bi	4.5	Fig. 7 (1990)	MUT?
tPHL/ tPLH	propagation delay E to nY		15	26		33		39	ns	4.5	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay S to nY		22	37		46		56	ns	4.5	Fig. 7	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7	

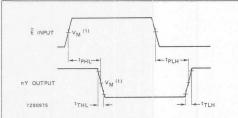
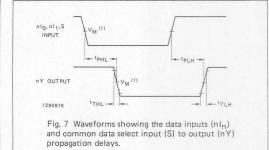


Fig. 6 Waveforms showing the enable input (\vec{E}) to output (nY) propagation delays and the output transition times.



Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.





Fig. ? Waveforms showing the data inputs (n|n) and common data solvet input (S) to purput (n|Y) programion delays.

Note to AC waveforms

OV OF BURY AND SOUND OF SOUND

QUAD 2-INPUT MULTIPLEXER; INVERTING

FEATURES

- Inverting data path
- · Output capability: standard
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT158 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT158 are quad 2-input multiplexers which select 4 bits of data from two sources and are controlled by a common data select input (S). The four outputs present the selected data in the inverted form. The enable input (\overline{E}) is active LOW.

When \overline{E} is HIGH, all the outputs $(1\overline{Y}$ to $4\overline{Y})$ are forced HIGH regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the "158". The state of S determines the particular register from which the data comes. It can also be used as a function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The "158" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations for the output are:

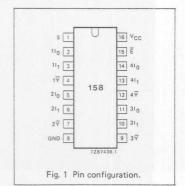
$$1\overline{Y} = \overline{E}.(11_1.S + 11_0.\overline{S})$$

$$2\overline{Y} = \overline{E}.(21_1.S + 21_0.\overline{S})$$

$$3\overline{Y} = \overline{E}.(31_1.S + 31_0.\overline{S})$$

$$4\overline{Y} = \overline{E}.(41_1.S + 41_0.\overline{S})$$

The "158" is identical to the "157" but has inverting outputs.



SYMBOL	PARAMETER	CONDITIONS	TYF	UNIT	
STIMBUL	PARAMETER	CONDITIONS	нс	нст	UNIT
^t PHL [/] ^t PLH	propagation delay nlo, nl1 to nY E to nY S to nY	C _L = 15 pF V _{CC} = 5 V	12 14 14	13 16 16	ns ns ns
CI	input capacitance	95	3.5	3.5	pF
C _{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	40	40	pF

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

$$\Sigma$$
 (C_L × V_{CC}² × f_o) = sum of outputs

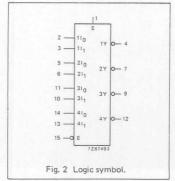
PACKAGE OUTLINES

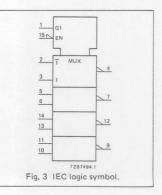
16-lead DIL; plastic (SOT38Z).

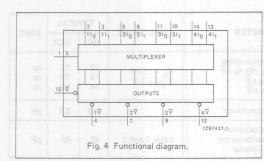
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	
1	S	common data select input	
2, 5, 11, 14	11 ₀ to 41 ₀	data inputs from source 0	
3, 6, 10, 13	11 ₁ to 41 ₁	data inputs from source 1	
4, 7, 9, 12	1₹ to 4₹	multiplexer outputs	
8	GND	ground (0 V)	
15	Ē	enable input (active LOW)	
16	Vcc	positive supply voltage	





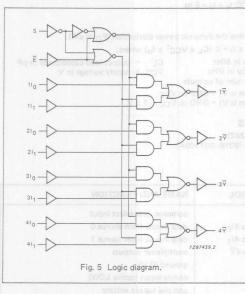


FUNCTION TABLE

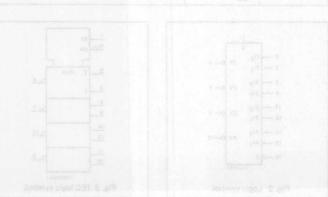
	11	IPUTS		OUTPUT
Ē	S	nlo	nl ₁	n∀
Н	X	X	X	ENERAL DES
L	h-L	L be	X	астан Нирх эл
L	L	Н	X	Joseph 2014/0 error-
L	Н	X	end Lunes	of daine Hollageres
L	Н	X	Н	דנ (נגדלונו). דה

H = HIGH voltage level L = LOW voltage level

X = don't care



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a mine the dynamic pewer disclined	
- \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	
110	A Vector
111 David Cho = Walnon	
210	
21,	
310	
311	
4	
Fig. 5 Logic diagram.	
CC positive supply voltage	





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF. sldat ett ni nwork melonikaan baol tinu eri

					T _{amb} (°C)				TVIE	TEST CONDITIONS
CVMADOL	DADAMETED				74H	:			LINUT	.,	WAYEFORMS
SYMBOL	PARAMETER		+25		-40	to +85	40 t	o +125	UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			E 0.60
tPHL/ tPLH	propagation delay nI ₀ , nI ₁ to n∀		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
tPHL/	propagation delay		47 17 14	145 29 25	(0°1 a	180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
tPHL/ a	propagation delay S to n∀	asi	47 17 14	145 29 25	TORU	180 36 31	25	220 44 38	ns	2.0 4.5 6.0	Fig. 7 PAN JOEMYS
tTHL/ tTLH	output transition time	336c.	19 7 6	75 15 13	an La	95 19 16	9. (08	110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

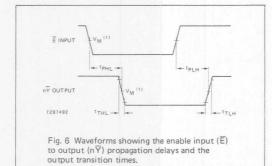
The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nlo	0.40
nlo	0.40
S	2.80
E	0.60

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	0.8	8	T _{amb} (°C)							TEST CONDITIONS		
CVMDOL	2.0	20	\$	0	74H	ст	Day 1	T B	LINUT	V	WAVEFORMS	UH
SYMBOL	PARAMETER	+25		-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORING		
	2.0	min.	typ.	max.	min.	max.	min.	max.				Value
t _{PHL} / t _{PLH}	propagation delay nI_0 , nI_1 to $n\overline{Y}$	6	16	30	21	38	er er	45	ns	4.5	Fig. 7	HJ.
t _{PHL} / t _{PLH}	propagation delay E to nY		19	35		44		53	ns	4.5	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay S to n∀		19	35		44		53	ns	4.5	Fig. 7	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7	





(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

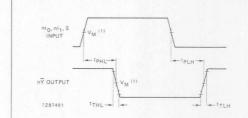


Fig. 7 Waveforms showing the data input (nI $_0$, nI $_1$) to output (n \overline{Y}) propagation delays and the output transition times.







PRESETTABLE SYNCHRONOUS BCD DECADE COUNTER: ASYNCHRONOUS RESET

FEATURES THE STATE OF LANGUAGE

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Asynchronous reset
- Output capability: standard
- Icc category: MSI

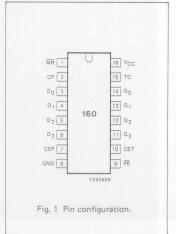
GENERAL DESCRIPTION

The 74HC/HCT160 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT160 are synchronous presettable decade counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input (PE) disables the counting action and causes the data at the data inputs (Do to D3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

(continued on next page)



01/44001	242445752	201101710110	TYPICAL		110117	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT	
^t PHL	propagation delay CP to Qn CP to TC MR to Qn MR to TC CET to TC	C _L = 15 pF V _{CC} = 5 V	19 21 21 21 14	21 24 23 26 14	ns ns ns ns	
^t PLH	propagation delay CP to Qn CP to TC CET to TC	040an 10 07 0-	19 21 14	21 20 7	ns ns ns	
fmax	maximum clock frequency	Fig. 4. Fundi	61	31	MHz	
Cl	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	39	34 08	pF	

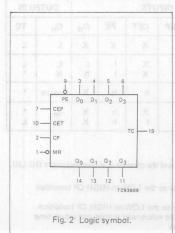
GND = 0 V;
$$T_{amb} = 25 \,^{\circ}C$$
; $t_r = t_f = 6 \, \text{ns}$

Notes September September 2016

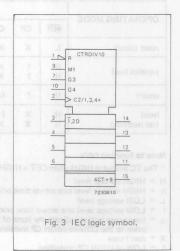
- 1. CPD is used to determine the dynamic power dissipation (PD in μ W):
 - PD = CPD x VCC^2 x f_i + Σ (CL x VCC^2 x f_o) where:
 - f; = input frequency in MHz fo = output frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is VI = GND to VCC For HCT the condition is $V_1 = GND$ to $V_{CC} - 1.5 V$

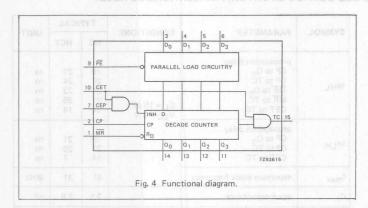
PACKAGE OUTLINES

- 16-lead DIL; plastic (SOT38Z).
- 16-lead mini-pack; plastic (SO16; SOT109A).









PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	MR	asynchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D ₀ to D ₃	data inputs count enable input
8	GND	ground (0 V)
garage in pFg	PE of Turno	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q ₀ to Q ₃	flip-flop outputs
15	TC V	
16	Vcc	positive supply voltage

FUNCTION TABLE

ODEDATING MODE		OUTPUTS						
OPERATING MODE	MR	СР	CEP	CET	PE	Dn	Qn	TC
reset (clear)	L	X	X	X	X	X	L	L
parallel load	H	†	×	X	1	l h	L H	L *
count	Н	†	h	h —	h	X	count	*
hold (do nothing)	H H	X	I X	X	h h	×	q _n q _n	* L

Note to function table

- * The TC output is HIGH when CET is HIGH and the counter is at terminal count (HLLH).
- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
- L = LOW voltage level
- I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
- q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
- X = don't care
- ↑ = LOW-to-HIGH CP transition

GENERAL DESCRIPTION

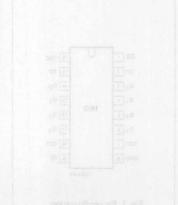
A LOW level at the master reset input (MR) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level regardless of the levels at CP, PE, CET and CEP inputs (thus providing an asynchronous clear function).

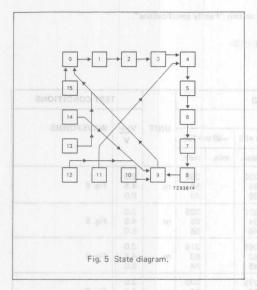
The look-ahead carry simplifies serial cascading of the counters, Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Ω_D . This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

f_{max} =

tP(max) (CP to TC) + tSU (CEP to CP)





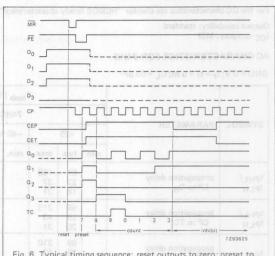
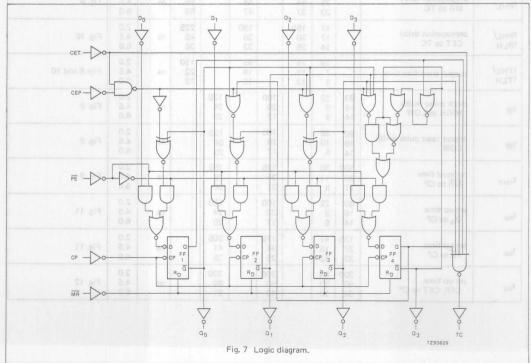


Fig. 6 Typical timing sequence: reset outputs to zero; preset to BCD seven; count to eight, nine, zero, one, two and three; inhibit.



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

		-		i	T _{amb} (°C)					TEST CONDITIONS
		M.		-	74H	С				\mathcal{X}	WAVEFORMS
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		1	
t _{PHL} /	propagation delay CP to Q _n		61 22 18	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 8
^t PHL [/]	propagation delay CP to TC		69 25 20	215 43 31		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 8
tPHL************************************	propagation delay MR to Q _n	ntes poi	69 25 20	210 42 36	Pig.	265 53 45		315 63 54	ns maga	2.0 4.5 6.0	Fig. 9
^t PHL	propagation delay MR to TC		69 25 20	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 9
t _{PHL} /	propagation delay CET to TC	¥	47 17 14	150 30 26		190 38 33	Ÿ	225 45 38	ns	2.0 4.5 6.0	Fig. 10
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 10
tw	clock pulse width HIGH or LOW	80 16 14	22 8 6	71	100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
tw	master reset pulse width	80 16 14	28 10 8	41	100 20 17	H	120 24 20		ns	2.0 4.5 6.0	Fig. 9
^t rem	removal time MR to CP	100 20 17	30 11 9		125 25 21	4	150 30 26		ns	2.0 4.5 6.0	Fig. 9
t _{su}	set-up time D _n to CP	80 16 14	22 8 6	H	100 20 17	Y	120 24 20		ns	2.0 4.5 6.0	Fig. 11
t _{su}	set-up time PE to CP	135 27 23	41 15 12		170 34 29	66-	205 41 35	19 1	ns	2.0 4.5 6.0	Fig. 11
t _{su}	set-up time CEP, CET to CP	200 40 34	63 23 18		250 50 43	an J	300 60 51		ns	2.0 4.5 6.0	Fig. 12

	"anoite of		Family	e anie	T _{amb} (°C)	and a late		HCN HCN		TEST CONDITIONS
					74H	С			UNIT		WAVEFORMS
SYMBOL	PARAMETER		+25	12.5	-40	to +85	-40 t	o +125	UNII	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			ote to HCT types
t _h	hold time D _n to CP	0 0		eig at f ode tris	0 0	non s beof r	0 0 0	Al men velue ev	ns	2.0 4.5 6.0	Figs 11 and 12
th	hold time PE to CP	0 0 0	-41 -15 -12		0 0 0	6 AF 101	0 0 0	193	ns	2.0 4.5 6.0	Figs 11 and 12
th	hold time CEP, CET to CP	0 0 0	-58 -21 -17		0 0	0	0 0 0	- 75	ns	2.0 4.5 6.0	Figs 11 and 12
f _{max}	maximum clock pulse frequency	6.0 30 35	18 55 66		4.8 24 28	ens ^T	4.0 20 24		MHz	2.0 4.5 6.0	en 8 = µ1 = p :V 0 = GM Fig. 8
					TOH	74					

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard 35% TIMB

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
MR CP	0.95
CEP	0.25

INPUT	UNIT LOAD COEFFICIENT
Dn	0.25
CET	1.05
PE	0.30

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	6.0			24	T _{amb} (°C)		38 98			TEST CONDITIONS
					74H0	СТ			UNIT		
SYMBOL	PARAMETER	+25			-40	-40 to +85		-40 to +125		V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
^t PHL/	propagation delay CP to Q _n		25	43		54		65	ns	4.5	Fig. 8
^t PHL	propagation delay CP to TC		28	48		60		72	ns	4.5	Fig. 8
^t PLH	propagation delay CP to TC		23	39		49		59	ns	4.5	Fig. 8
^t PHL	propagation delay MR to Qn		27	50		63		75	ns	4.5	Fig. 9
[†] PHL	propagation delay MR to TC		30	50		63		75	ns	4.5	Fig. 9
^t PHL	propagation delay CET to TC		17	35		44		53	ns	4.5	Fig. 10
^t PLH	propagation delay CET to TC		9	17		21		26	ns	4.5	Fig. 10
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 8 and 10
tw	clock pulse width HIGH or LOW	16	8		20		24		ns	4.5	Fig. 8
tw	master reset pulse width LOW	20	11		25		30		ns	4.5	Fig. 9
^t rem	removal time MR to CP	20	9		25		30		ns	4.5	Fig. 9
t _{su}	set-up time D _n to CP	18	10		25		30		ns	4.5	Fig. 11
t _{su}	set-up time PE to CP	30	18		44		53		ns	4.5	Fig. 11
t _{su}	set-up time CEP, CET to CP	50	30		63		75		ns	4.5	Fig. 12

					Tamb (°C)				TEST CONDITIONS		
0.41501					74H0	ст			UNIT		WAVEFORMS	
SYMBOL	PARAMETER		+25	ing	-40	to +85	-40 t	o +125	UNII	V _{CC}		
		min.	typ.	max.	min.	max.	min.	max.				
t _h	hold time D _n to CP	0	-8		0		0		ns	4.5	Figs 11 and 12	
th	hold time PE to CP	0	-13		0		0		ns	4.5	Figs 11 and 12	
th	hold time CEP, CET to CP	0	-21		0		0		ns	4.5	Figs 11 and 12	
f _{max}	maximum clock pulse frequency	16	28		13		11		MHz	4.5	Fig. 8	

PRESETTABLE SYNCHRONOUS 4-BIT BINARY COUNTER; ASYNCHRONOUS RESET

FEATURES DITEINORS LANGUAGE

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Asynchronous reset
- Output capability: standard
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT161 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT161 are synchronous presettable binary counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs $(Q_0 \text{ to } Q_3)$ of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input (PE) disables the counting action and causes the data at the data inputs (Do to D3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

(continued on next page)

MR 1	U	16 V _{CC}
CP 2		15 TC
D ₀ 3		14 Q ₀
D ₁ 4		13 Q ₁
D ₂ 5	161	12 02
D ₃ 6		11 03
CEP 7		10 CET
GND 8		9 PE
	7Z936	506

CVMDOL	DADAMETER	COMPLETIONS	TYF	118117	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
^t PHL [/] ^t PLH	propagation delay CP to Q _n CP to TC MR to Q _n MR to TC CET to TC	C _L = 15 pF V _{CC} = 5 V	19 21 20 20 10	20 24 25 26 14	ns ns ns ns
f _{max}	maximum clock frequency	SLAPE TO	44	45	MHz
CI	input capacitance	10	3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	33	35	pF

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

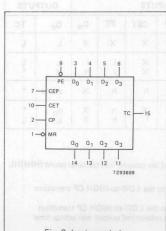
$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

- fi = input frequency in MHz CL = output load capacitance in pF
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$ 2. For HC the condition is V_I = GND to V_{CC}
- For HCT the condition is $V_1 = GND$ to VCC 1.5 V

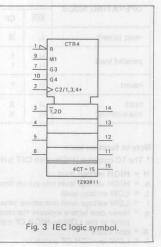
PACKAGE OUTLINES

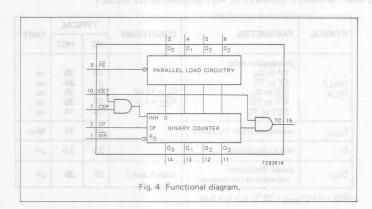
16-lead DIL; plastic (SOT38Z). Sugrue pull-gill

16-lead mini-pack; plastic (SO16; SOT109A).









PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2 3, 4, 5, 6 7 8 9 10 14, 13, 12, 11 15	MR CP D0 to D3 CEP GND PE CET Q0 to Q3 TC VCC	asynchronous master reset (active LOW) clock input (LOW-to-HIGH, edge-triggered) data inputs count enable input ground (0 V) parallel enable input (active LOW) count enable carry input flip-flop outputs terminal count output positive supply voltage

FUNCTION TABLE

OPERATING MODE			INP	UTS			OUTP	UTS
OPERATING MODE	MR	СР	CEP	CET	PE	Dn	Qn	ТС
reset (clear)	L	Χ	X	X	X	X	L	L
parallel load	H	†	×	×	al a	l h	L H	L *
count	Н	1	h	h	h	X	count	*
hold (do nothing)	H	×	l X	X	h h	×	qn	* L

Note to function table

- * The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).
- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
- L = LOW voltage level
- I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
- X = don't care
- ↑ = LOW-to-HIGH CP transition

GENERAL DESCRIPTION

A LOW level at the master reset input (MR) sets all four outputs of the flip-flops (Q₀ to Q₃) to LOW level regardless of the levels at CP, PE, CET and CEP inputs (thus providing an asynchronous clear function).

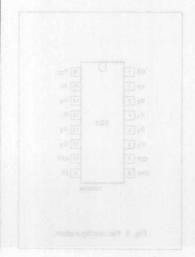
The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Qo. This pulse can be used to enable the next cascaded stage.

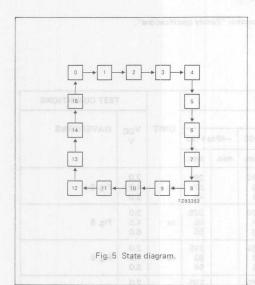
The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

f_{max} =

tP(max) (CP to TC) + tSU (CEP to CP) euts (Og to Og) of the counters present to a HIGH or LOW level.

on the positive-going edg





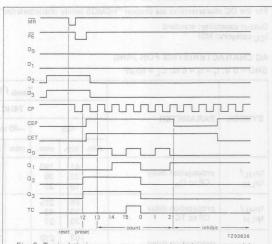
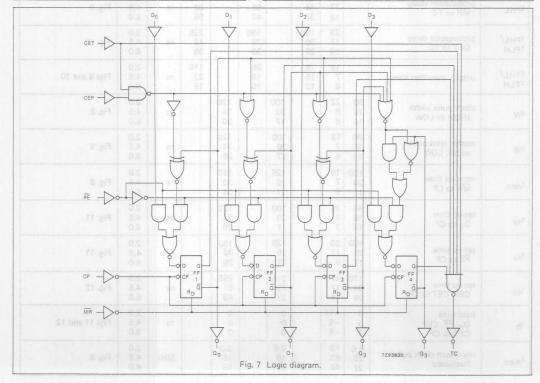


Fig. 6 Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSi

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

				1	T _{amb} (°C)					TEST CONDITIONS
TLITL		TITLE	Щ	-	74H	С		1			WAVEFORMS
SYMBOL	PARAMETER		+25	4	-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} /	propagation delay CP to Q _n		61 22 18	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 8
^t PHL [/]	propagation delay CP to TC	5) 5)	69 25 20	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 8
^t PHL	propagation delay MR to Q _n	iagas opi internation	63 23 18	210 42 36	.gi3L anid	265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 9
^t PHL	propagation delay MR to TC		63 23 18	220 44 37		275 55 47	14	330 66 56	ns	2.0 4.5 6.0	Fig. 9
tPHL/	propagation delay CET to TC		33 12 10	150 30 26		190 38 33	Y	225 45 38	ns	2.0 4.5 6.0	Fig. 10
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 10
tw	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17	V	120 24 20		ns	2.0 4.5 6.0	Fig. 8
tw	master reset pulse width; LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
^t rem	removal time MR to CP	100 20 17	19 7 6		125 25 21	Y	150 30 26		ns	2.0 4.5 6.0	Fig. 9
^t su	set-up time D _n to CP	80 16 14	25 9 7	D	100 20 17	Ų	120 24 20		ns	2.0 4.5 6.0	Fig. 11
t _{su}	set-up time PE to CP	100 20 17	30 11 9	Ţ	125 25 21		150 30 26	-5	ns	2.0 4.5 6.0	Fig. 11
t _{su}	set-up time CEP, CET to CP	170 34 29	47 17 14		215 43 37	200	255 51 43	- D 68	ns	2.0 4.5 6.0	Fig. 12
^t h	hold time D _n , PE, CEP, CET to CP	0 0 0	-14 -5 -4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 11 and 12
fmax	maximum clock pulse frequency	4.6 23 27	13 40 48	lagram.	3.6 18 21	V apis	3.0 15 18		MHz	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
MR	0.95
CP	1.10
CEP	0.25

INPUT	UNIT LOAD COEFFICIENT
Dn	0.25
CET	0.75
PE TUSTNO	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

	ulc (CP) removal timil.	of feed lettern siT _{amb} (°C)						урлаци	TEST CONDITIONS		
CVMADOL	BARAMETER				74HC	т			UNIT		WANEEODMC
SYMBOL	PARAMETER	+25			-40	to +85	-40 t	-40 to +125		V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/	propagation delay CP to Q _n	WA F	23	43		54		65	ns	4.5	Fig. 8
tPHL/	propagation delay CP to TC		28	48		60		72	ns	4.5	Fig. 8
^t PHL	propagation delay MR to Q _n	w wy	29	46		58		69	ns	4.5	Fig. 9
tPHL	propagation delay MR to TC		30	51		64		77	ns	4.5	Fig. 9
t _{PHL} /	propagation delay CET to TC		17	35		44		53	ns	4.5	Fig. 10
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 8 and 10
t _W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 8
tw	master reset pulse width; LOW	20	10	FT .gi D) rwar	25	103	30	ennis Lesmis	ns	4.5	Fig. 9
t _{rem}	removal time MR to CP	20	6		25		30		ns	4.5	Fig. 9
t _{su}	set-up time D _n to CP	18	8	Non	23		27		ns	4.5	Fig. 11
t _{su}	set-up time PE to CP	30	17		38		45	- Miles	ns	4.5	Fig. 11
t _{su}	set-up time CEP, CET to CP	40	17		50		60		ns	4.5	Fig. 12
^t h	hold time D _n , PE, CEP, CET to CP	0	-7	Moral Mark	0	acets.	0		ns	4.5	Figs 11 and 12
f _{max}	maximum clock pulse frequency	23	41		18		15		MHz	4.5	Fig. 8 .25mit blod

AC WAVEFORMS

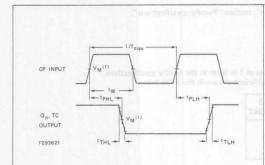


Fig. 8 Waveforms showing the clock (CP) to outputs (Ω_n , TC) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

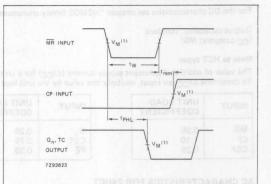


Fig. 9 Waveforms showing the master reset $(\overline{\text{MR}})$ pulse width, the master reset to output $(\Omega_{\text{D}}, \text{TC})$ propagation delays and the master reset to clock (CP) removal time.

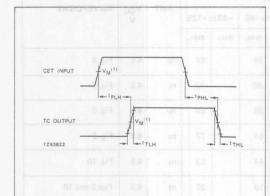


Fig. 10 Waveforms showing the input (CET) to output (TC) propagation delays and output transition times.

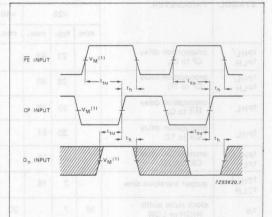


Fig. 11 Waveforms showing the set-up and hold times for the input (Dn) and parallel enable input $\overline{PE}.$

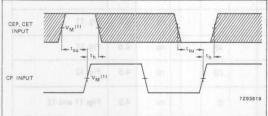


Fig. 12 Waveforms showing the CEP and CET set-up and hold times.

Note to Figs 11 and 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

PRESETTABLE SYNCHRONOUS BCD DECADE COUNTER; SYNCHRONOUS RESET

FEATURES THE PROPERTY OF THE P

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Synchronous reset
- Output capability: standard
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT162 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT162 are synchronous presettable decade counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs $(Q_0 \text{ to } Q_3)$ of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input (PE) disables the counting action and causes the data at the data inputs (Do to D3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

For the "162" the clear function is synchronous.

		CONDITIONS	TYF		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
^t PHL	propagation delay CP to Qn CP to TC CET to TC	C C	19 21 11	20 26 15	ns ns ns
^t PLH	propagation delay CP to Q _n CP to TC CET to TC	C _L = 15 pF V _{CC} = 5 V	19 21 11	20 19 10	ns ns ns
fmax	maximum clock frequency	MI	63	32	MHz
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	37	37	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

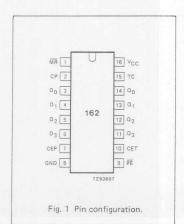
PD = CPD x
$$VCC^2$$
 x f; + Σ (CL x VCC^2 x f₀) where:

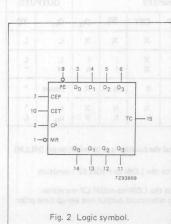
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is VI = GND to VCC For HCT the condition is $V_I = GND$ to VCC - 1.5 V

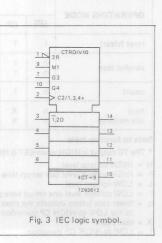
PACKAGE OUTLINES

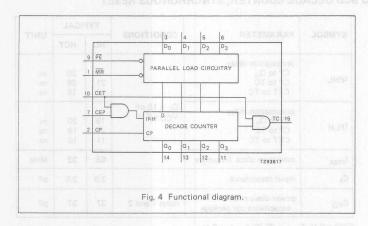
- 16-lead DIL; plastic (SOT38Z).
- 16-lead mini-pack; plastic (SO16; SOT109A).

(continued on next page)









PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1 2 3, 4, 5, 6 7 8 9 10 14, 13, 12, 11 15 16	MR CP D0 to D3 CEP GND PE CET Q0 to Q3 TC VCC	synchronous master reset (active LOW) clock input (LOW-to-HIGH, edge-triggered) data inputs count enable input ground (0 V) parallel enable input (active LOW) count enable carry input flip-flop outputs terminal count output positive supply voltage

FUNCTION TABLE

ODED ATIMO MODE		INPUTS										
OPERATING MODE	MR	СР	CEP	CET	PE	Dn	Qn	тс				
reset (clear)	_1	1	X	X	X	X	L	L				
parallel load	h h	†	×	X	1 4	l h	L H	L *				
count	h	1	h	h	h s	X	count	*				
hold (do nothing)	h h	X	l X	X	h h	×	q _n	* L				

Note to function table

- * The TC output is HIGH when CET is HIGH and the counter is at terminal count (HLLH).
- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
- L = LOW voltage level
- = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
- q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
- X = don't care
- ↑ = LOW-to-HIGH CP transition

GENERAL DESCRIPTION

A LOW level at the master reset input (\overline{MR}) sets all four outputs of the flip-flops $(Q_0$ to Q_3) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for \overline{MR} are met). This action occurs regardless of the levels at \overline{PE} , CET and CEP inputs.

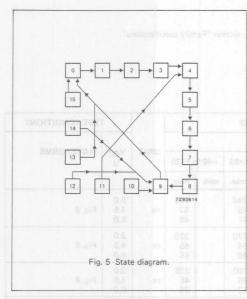
This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0 . This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

fmax =

tp(max) (CP to TC) + t_{SU} (CEP to CP)



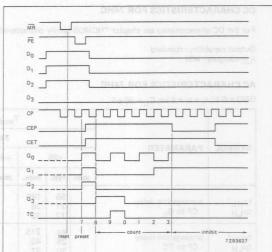
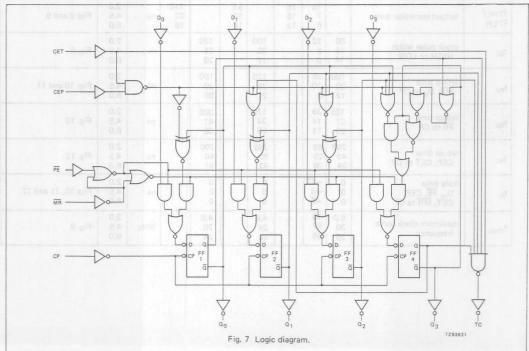


Fig. 6—Typical timing sequence: reset outputs to zero; preset to BCD seven; count to eight, nine, zero, one, two and three; inhibit.



DC CHARACTERISTICS FOR 74HC

11

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_1 = 50 pF$

					T _{amb} (°C)				1	TEST CONDITIONS
				120	74H	С			A The second		
SYMBOL	PARAMETER		+25	_ p0	-40	to +85	-40 to +125		UNIT	VCC	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.	6-4		
t _{PHL} /	propagation delay CP to Q _n		58 21 17	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 8
tpHL/	propagation delay CP to TC	100910	69 25 20	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 8
tPHL/	propagation delay CET to TC	gis er in	39 14 11	150 30 26	9	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t _{THL} /	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 9
tw	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17	¥.	120 24 20		ns	2.0 4.5 6.0	Fig. 8
t _{su}	set-up time MR, D _n to CP	100 20 17	28 10 8		125 25 21		150 30 26	4	ns	2.0 4.5 6.0	Figs 10 and 11
t _{su}	set-up time PE to CP	135 27 23	39 14 11		170 34 29		205 41 35		ns	2.0 4.5 6.0	Fig. 10
t _{su}	set-up time CEP, CET to CP	200 40 34	69 25 20		250 50 43		300 60 51	V.	ns	2.0 4.5 6.0	Fig. 12
t _h	hold time D _n , PE, CEP, CET, MR to CP	0 0 0	-17 -6 -5		0 0 0	ħ,	0 0	þt	ns	2.0 4.5 6.0	Figs 10, 11 and 12
f _{max}	maximum clock pulse frequency	6.0 30 35	19 57 68		4.8 24 28	7	4.0 20 24	Ţ	MHz	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
MR	0.95
CP	0.80
CEP	0.25

INPUT	UNIT LOAD COEFFICIENT
Dn	0.25
CET	1.05
PE	0.30

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		T _{amb} (°C)								TEST CONDITIONS		
					74HC	Т				.,	WANTEGRAG	
SYMBOL	PARAMETER		+25		-40	to +85	-40 to	+125	UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		1	TOTAL TOTAL SE	
t _{PHL} /	propagation delay CP to Q _n	-14	24	43		54		65	ns	4.5	Fig. 8	
^t PHL	propagation delay CP to TC	A	30	51		64	i	77	ns	4.5	Fig. 8	
^t PLH	propagation delay CP to TC		22	45		56	- , L	68	ns	4.5	Fig. 8	
^t PHL	propagation delay CET to TC		18	35		44		53	ns	4.5	Fig. 9	
^t PLH	propagation delay CET to TC		12	24		30	80.95	36	ns	4.5	Fig. 9	
t _{THL} / t _{TLH}	output transition time	anets	7	15		19	nt semis	22	ns	4.5	Figs 8 and 9	
tw	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 8	
t _{su}	set-up time D _n to CP	20	9		25		30		ns	4.5	Fig. 10	
t _{su}	set-up time PE to CP	35	16	569. TT	44		53		ns	4.5	Fig. 10	
t _{su}	set-up time CEP, CET to CP	40	23	#IS	50		60	100	ns	4.5	Fig. 12	
t _{su}	set-up time MR to CP	20	12		25		30		ns	4.5	Fig. 11	
^t h	hold time D _n , PE, CEP, CET, MR to CP	0 0 A	-10	(3) (3)	0	EX.	0		ns	4.5	Figs 10, 11 and 12	
f _{max}	maximum clock pulse frequency	17	29		14	bela	11	aŭ ans	MHz	4.5	Fig. 8	

AC WAVEFORMS

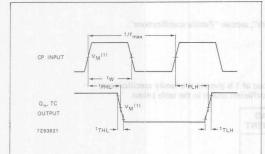


Fig. 8 Waveforms showing the clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

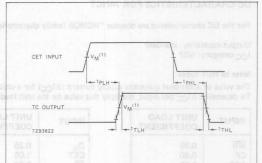


Fig. 9 Waveforms showing the input (CET) to output (TC) propagation delays and output transition times.

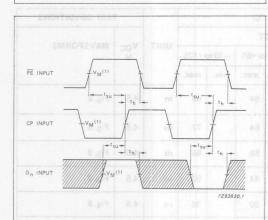


Fig. 10 Waveforms showing the set-up and hold times for the input (D_n) and parallel enable input (\overline{PE}) .

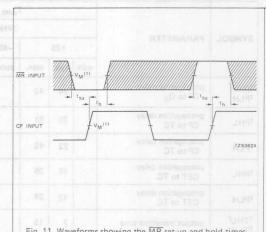


Fig. 11 Waveforms showing the MR set-up and hold times.

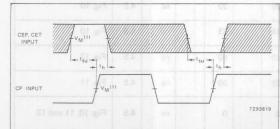


Fig. 12 Waveforms showing the CEP and CET set-up and

Note to Figs 10, 11 and 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

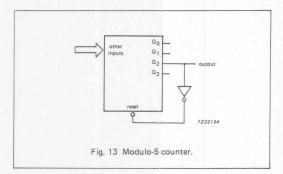
Note to AC waveforms

(1) HC : VM = 50%; VI = GND to VCC. HCT: VM = 1.3 V; VI = GND to 3 V.

APPLICATION INFORMATION

The HC/HCT162 facilitate designing counters of any modulus with minimal external logic.

The output is glitch-free due to the synchronous reset.

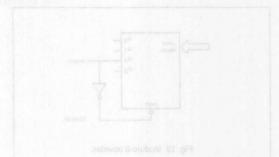


APPLICATION INFORMATION

The HC/HCT162 facilitate designing countars of any modulus with

minimal external logic.

The output is glitch-free due to the synchronous reset.



PRESETTABLE SYNCHRONOUS 4-BIT BINARY COUNTER: SYNCHRONOUS RESET

FEATURES THROUGH JARRENSO

- Synchronous counting and loading Two count enable inputs for n-bit
- Positive-edge triggered clock
- Synchronous reset

cascading

- Output capability: standard
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT163 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT163 are synchronous presettable binary counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q₀ to Q₃) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input (PE) disables the counting action and causes the data at the data inputs (Dn to D3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

For the "163" the clear function is synchronous.

(continued on next page)

CP 2

D₀ 3

D1 4

02 5

03 6

CEP 7

GND 8

SYMBOL	DADAMETED	CONDITIONS	TYF	UNIT	
SAMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
^t PHL [/] ^t PLH	propagation delay CP to Qn CP to TC CET to TC	C _L = 15 pF V _{CC} = 5 V	17 21 11	20 25 14	ns ns ns
f _{max}	maximum clock frequency		51	50	MHz
CI	input capacitance	TAKE THE T	3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	33	35	pF

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD \times VCC² \times f₁ + Σ (CL \times VCC² \times f₀) where:

fi = input frequency in MHz CL = output load capacitance in pF

fo = output frequency in MHz VCC = supply voltage in V

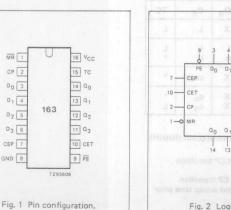
 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

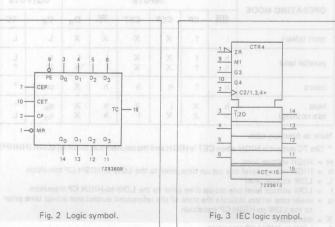
2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

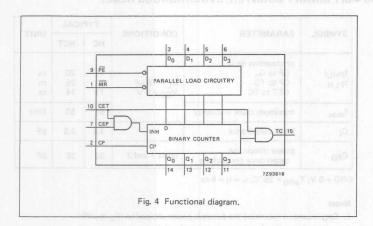
PACK AGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).







PIN DESCRIPTION

NAME AND FUNCTION
synchronous master reset (active LOW)
clock input (LOW-to-HIGH, edge-triggered)
data inputs count enable input 33ML/TUO 30A XOAS
ground (0 V) 15867021 strasta 210 869121
parallel enable input (active LOW)
count enable carry input
flip-flop outputs
terminal count output
positive supply voltage
3

FUNCTION TABLE

OPERATING MODE			INP	UTS			OUTPUTS	
OPERATING MODE	MR	СР	CEP	CET	PE	Dn	an	TC
reset (clear)	-1	1	X	X	X	X	L	L
parallel load	h	↑	×	X	1	l h	L H	L *
count	h	1	h	h	h	X	count	*
hold (do nothing)	h h	×	l X	X	h h	×	q _n q _n	· L

Note to function table

- * The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).
- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
- L = LOW voltage level
- I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
- q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
- X = don't care
- ↑ = LOW-to-HIGH CP transition

GENERAL DESCRIPTION (Cont'd)

A LOW level at the master reset input (\overline{MR}) sets all four outputs of the flip-flops $(Q_0$ to Q_3) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for \overline{MR} are met). This action occurs regardless of the levels at \overline{PE} , CET and CEP inputs.

This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Ω_0 . This pulse can be used to enable the next cascaded stage.

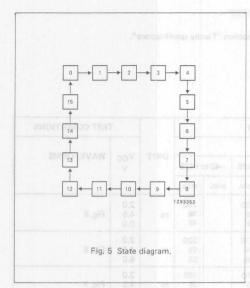
The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

fmax =

tp(max) (CP to TC) + tSU (CEP to CP)



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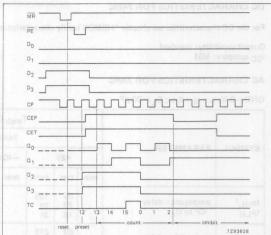
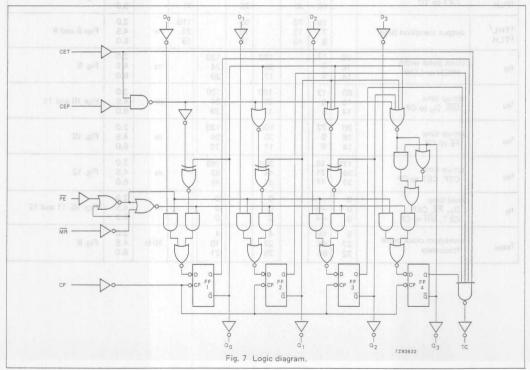


Fig. 6 Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		1			T _{amb} (°C)					TEST CONDITIONS	
CVMDO:	DADAMETER				74H	С		1	LINUT		WAVEFORMS	
SYMBOL	PARAMETER	+25		-40 to +85		-40 to +125		UNIT	VCC	WAVEFORIVIS		
		min.	typ.	max.	min.	max.	min.	max.	- E	of or		
t _{PHL} /	propagation delay CP to Q _n		55 20 16	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 8	
t _{PHL} /	propagation delay CP to TC	e printing at	69 25 20	215 43 37	Pre bid	270 54 46		320 65 55	ns	2.0 4.5 6.0	Fig. 8	
t _{PHL} /	propagation delay CET to TC		36 13 10	120 24 20	501	150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 9	
t _{THL} /	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 9	
tw	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	
t _{su}	set-up time MR, D _n to CP	80 16 14	17 6 5		100 20 17		120 24 20	4	ns	2.0 4.5 6.0	Figs 10 and 11	
t _{su}	set-up time PE to CP	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10	
t _{su}	set-up time CEP, CET to CP	175 35 30	58 21 17		220 44 37		265 53 45	9	ns	2.0 4.5 6.0	Fig. 12	
^t h	hold time D _n , PE, CEP, CET, MR to CP	0 0 0	-14 -5 -4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 10, 11 and 12	
f _{max}	maximum clock pulse frequency	5 27 32	15 46 55		4 22 26	Ĭ.	4 18 21	H	MHz	2.0 4.5 6.0	Fig. 8	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
MR	0.95
CP	1.10
CEP	0.25

INPUT	UNIT LOAD COEFFICIENT
D _n CET	0.25 0.75
PE	0.75

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)				TEST CONDITIONS		
					74HC	Т	1		UNIT	1	WAVEFORMS	
SYMBOL	PARAMETER	+25		-40 to +85		-40 to +125		UNII	V _{CC}	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.		N =	m ² — m	
tPHL/	propagation delay CP to Q _n		23	39		49		59	ns	4.5	Fig. 8	
t _{PHL} /	propagation delay CP to TC		29	49		61		74	ns	4.5	Fig. 8	
tPHL/	propagation delay CET to TC		17	32		44		48	ns	4.5	Fig. 9	
t _{THL} / t _{TLH}	output transition time		7	15		19	SCIENT.	22	ns	4.5	Figs 8 and 9	
tw	clock pulse width HIGH or LOW	20	6		25		30		ns	4.5	Fig. 8	
t _{sumb} blor	set-up time MR, D _n to CP	20	9	Fig. 1	25	arti n	30	Blort br	ns	4.5	Figs 10 and 11	
t _{su}	set-up time PE to CP	20	11		25		30		ns	4.5	Fig. 10	
t _{su}	set-up time CEP, CET to CP	40	24		50		60		ns	4.5	Fig. 12	
t _h ballionad	hold time D _n , PE, CEP, CET, MR to CP	0	-5	ET Ho	0		0		ns	4.5	Figs 10, 11 and 12	
f _{max}	maximum clock pulse frequency	26	45		21		17		MHz	4.5	Fig. 8	

AC WAVEFORMS

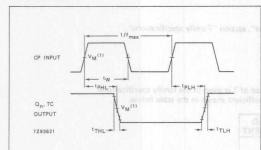


Fig. 8 Waveforms showing the clock (CP) to outputs (Q_n , TC) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

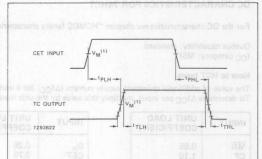


Fig. 9 Waveforms showing the input (CET) to output (TC) propagation delays and output transition times.

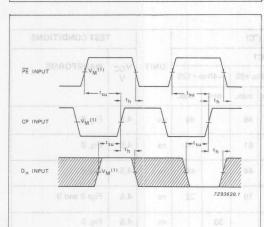


Fig. 10 Waveforms showing the set-up and hold times for the input (D_{Π}) and parallel enable input $(\overline{PE}).$

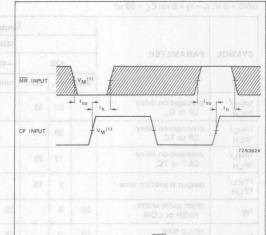


Fig. 11 Waveforms showing the $\overline{\text{MR}}$ set-up and hold times.

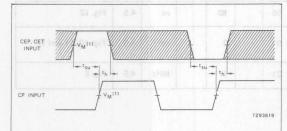


Fig. 12 Waveforms showing the CEP and CET set-up and hold times.

Note to Figs 10, 11 and 12

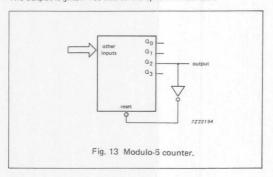
The shaded areas indicate when the input is permitted to change for predictable output performance.

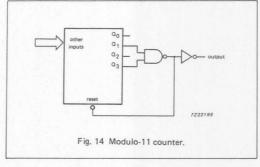
Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_1 = GND$ to V_{CC} . HCT: $V_M = 1.3$ V; $V_1 = GND$ to 3 V.

APPLICATION INFORMATION

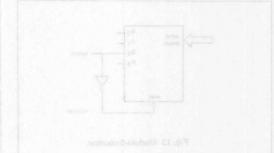
The HC/HCT163 facilitate designing counters of any modulus with minimal external logic. The output is glitch-free due to the synchronous reset.

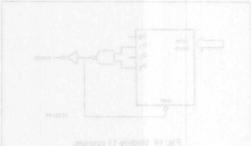




APPLICATION INFORMATION

The HC/HCT163 facilitize designing country, of any modulus with minimal external logic. The output is glitch-free due to the synchronous reset.





8-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER

FEATURES

- Gated serial data inputs
- Asynchronous master reset Output capability: standard
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT164 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT164 are 8-bit edgetriggered shift registers with serial data entry and an output from each of the eight stages.

Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock (CP) input and enters into Qo, which is the logical AND of the two data inputs (Dsa, Dsb) that existed one set-up time prior to the rising clock edge.

A LOW level on the master reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

OTTAGUE		CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	ONT	
^t PHL [/] ^t PLH	propagation delay $ \begin{array}{c} \text{CP to } Q_n \\ \overline{\text{MR}} \text{ to } Q_n \end{array} $	C _L = 15 pF - V _{CC} = 5 V	12	14 16	ns ns	
f _{max}	maximum clock frequency	05 04 05 03 0	78	61	MHz	
CI	input capacitance	8 6 8 8	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	40	40	pF	

 $GND = 0 \text{ V; } T_{amh} = 25 \, ^{\circ}\text{C; } t_r = t_f = 6 \text{ ns}$

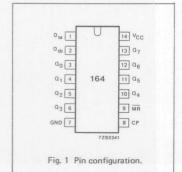
- 1. CPD is used to determine the dynamic power dissipation (PD in μ W):
 - PD = CPD x VCC^2 x f_i + Σ (CL x VCC^2 x f_o) where:
 - fi = input frequency in MHz fo = output frequency in MHz
- VCC = supply voltage in V $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to VCC For HCT the condition is V_I = GND to VCC -1.5 V

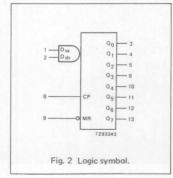
PACKAGE OUTLINES

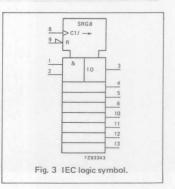
- 14-lead DIL; plastic (SOT27)
- 14-lead mini pack; plastic (SO14; SOT108A)

PIN DESCRIPTION

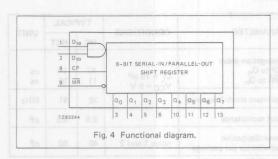
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	D _{sa} , D _{sb}	data inputs
3, 4, 5, 6, 10, 11, 12, 13	Q ₀ to Q ₇	outputs
7	GND	ground (0 V)
8	CP	clock input (LOW-to-HIGH, edge-triggered)
9	MR	master reset input (active LOW)
14	Vcc	positive supply voltage







CL = output load capacitance in pF



APPLICATIONS

Serial data transfer

FUNCTION TABLE

OPERATING MODES	(i) nai	INF	UTS		OUTPUTS		
OPERATING MODES	MR	СР	D _{sa}	D _{sb}	00	Q ₁ - Q ₇	
reset (clear)	Liggi	X	X	X	L	L n→cLn	
	Н	1	1 -	1	L	90 — 96	
shift	Н	1	1	h	L	90 - 96	
311110	Н	1	h	1	L	90 - 96	
	Н	1	h	h	Н	90 - 96	

H = HIGH voltage level

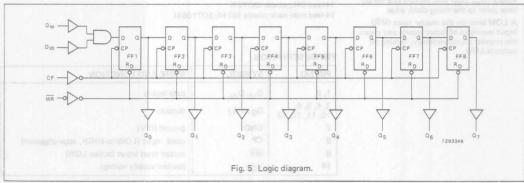
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

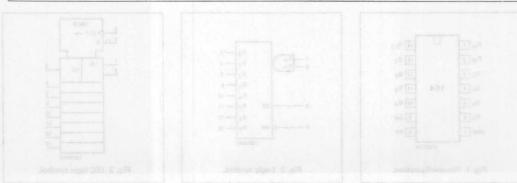
L = LOW voltage level

I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition

↑ = LOW-to-HIGH clock transition





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC at self-di-navig at 1 to had sinu/a not (53/4) toomus vincus trassesup land tipbe to suc

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

					T _{amb} (°C)				TIGH	TEST CONDITION	SNC
OVMOOL	DADAMETER				74H	:			LIMIT	,,	WAVEFORMS	
SYMBOL	PARAMETER		+25		-40	to +85	-40 to +125		UNIT	V _{CC}	OR O RM	
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay CP to Q _n		41 15 12	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6	
tPHL SMOII	propagation delay MR to Ω _n		39 14 11	140 28 24	e l'et	175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7	
tTHL/ tTLH	output transition time	(25 nox	19 7 6	75 15 13	-	95 19 16	25 /p. 10	110 22 19	ns	2.0 4.5 6.0	Fig. 6	10amy
tW	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6 93	UH9 HU9
tW	master reset pulse width; LOW	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7	JRS
t _{rem}	removal time MR to CP	60 12 10	17 6 5	\$	75 15 13	2	90 18 15	8)	ns	2.0 4.5 6.0	Fig. 7	HJT W
t _{su}	set-up time Dsa, Dsb to CP	60 12 10	8 3 2	2	75 15 13	9	90 18 15	81	ns	2.0 4.5 6.0	Fig. 8	W
^t h	hold time D _{sa} , D _{sb} to CP	4 4 4	-6 -2 -2	20	4 4 4	2	4 4 4	81	ns	2.0 4.5 6.0	Fig. 8	men
f _{max}	maximum clock pulse frequency	6 30 35	23 71 85	6	5 24 28	b	4 20 24	1	MHz	2.0 4.5 6.0	Fig. 6	if

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle 1_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle 1_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

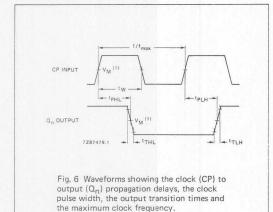
INPUT	UNIT LOAD COEFFICIENT
D _{sa} , D _{sb}	0.25
CP	0.60
MR	0.90

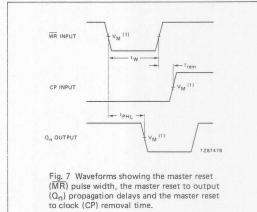
AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

				. 8	T _{amb} (°C)				walsh	TEST CONDITION	NS
	ns 4.5 Fig.7 8.0	at			74HC		2 1		LIAUT		WAVEFORMS	
SYMBOL	PARAMETER	011	+25		-40 to +85		-40 to +125		UNIT	V _{CC}		
	4.5 Fig.6	min.	typ.	max.	min.	max.	min.	max.		no nee	SURE STATE	
t _{PHL} /	propagation delay CP to Q _n		17	36	98	45	4	54	ns	4.5	Fig. 6 and a	VV
^t PHL	propagation delay MR to Qn		19	38		48	7	57	ns	4.5	Fig. 7	
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6	10
tw	clock pulse width HIGH or LOW	18	7		23	!	27	12 1	ns	4.5	Fig. 6	men
t₩	master reset pulse width; LOW	18	10	18	23	To an and an	27	08	ns	4.5	Fig.17,u-792	87.
t _{rem}	removal time MR to CP	16	7	4	20	L.	24 a	- 40	ns	4.5	Fig. 7	
t _{su}	set-up time D _{sa} , D _{sb} to CP	12	6		15	à	18		ns	4.5	Fig. 8	
^t h	hold time D _{sa} , D _{sb} to CP	4	-2	28	4	2 2	4	30	ns	4.5	Fig. 8	Xam
f _{max}	maximum clock pulse frequency	27	55		22		18		MHz	4.5	Fig. 6	

AC WAVEFORMS





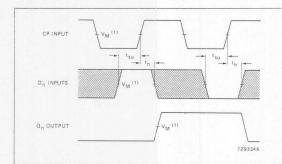
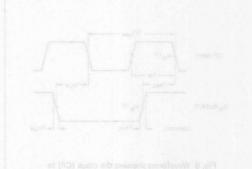


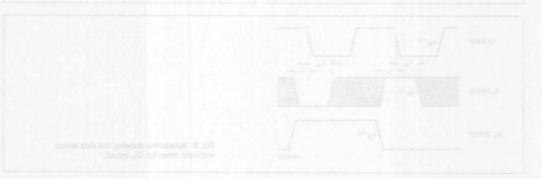
Fig. 8 Waveforms showing the data set-up and hold times for D_n inputs.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.







8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER

FEATURES

- Asynchronous 8-bit parallel load
- Synchronous serial input
- Output capability: standard
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT165 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

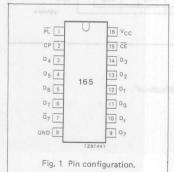
The 74HC/HCT165 are 8-bit parallel-load or serial-in shift registers with complementary serial outputs (Ω_7 and $\overline{\Omega}_7$) available from the last stage. When the parallel load (\overline{PL}) input is LOW, parallel data from the D₀ to D₇ inputs are loaded into the register asynchronously.

When PL is HIGH, data enters the register serially at the D_S input and shifts one place to the right $(Q_0 \rightarrow Q_1 \rightarrow Q_2)$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_S input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable (\overline{CE}) input. The pin assignment for the CP and \overline{CE} inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input \overline{CE} should only take place while CP HIGH for predictable operation. Either the CP or the \overline{CE} should be HIGH before the LOW-to-HIGH transition of \overline{PL} to prevent shifting the data when \overline{PL} is activated.

APPLICATIONS

Parallel-to-serial data conversion



		CONDITIONS	TYF	LINUT		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT	
^t PHL [/] ^t PLH	propagation delay CP to Q7, Q7 PL to Q7, Q7 D7 to Q7, Q7	C _L = 15 pF V _{CC} = 5 V	16 15 11	14 17 11	ns ns ns	
f _{max}	maximum clock frequency	S IN-TITIES OF	56	48	MHz	
CI	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	35	35	pF	

VCC = supply voltage in V

$$GND = 0 \text{ V}; T_{amb} = 25 \,^{\circ}\text{C}; t_r = t_f = 6 \text{ ns}$$

Notes

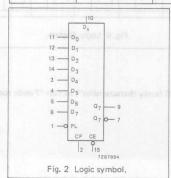
- 1. CPD is used to determine the dynamic power dissipation (PD in μ W):
 - $PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$ where:
 - fi = input frequency in MHz CL = output load capacitance in pF
 - f_0 = output frequency in MHz $\Sigma (C_L \times V_{CC}^2 \times f_0)$ = sum of outputs
- 2. For HC the condition is V₁ = GND to V_{CC}
- For HCT the condition is $V_1 = GND$ to $V_{CC} = 1.5 \text{ V}$

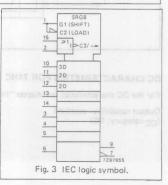
PACKAGE OUTLINES

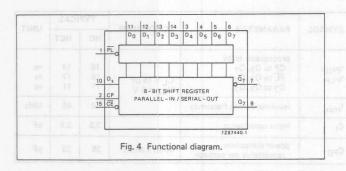
- 16-lead DIL; plastic (SOT38Z).
- 16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO. SYMBOL		NAME AND FUNCTION				
1	PL	asynchronous parallel load input (active LOW)				
7	₫7	complementary output from the last stage				
9	07	serial output from the last stage				
2	CP	clock input (LOW-to-HIGH edge-triggered)				
8	GND	ground (0 V)				
10	Ds	serial data input				
11, 12, 13, 14, 3, 4, 5, 6	D ₀ to D ₇	parallel data inputs				
15	CE	clock enable input (active LOW)				
16	Vcc	positive supply voltage				







FUNCTION TABLE

OPERATING MODES	INPUTS				Qn REGISTERS		OUTPUTS		
	PL	CE	СР	Ds	D ₀ -D ₇	ο ₀	01-06	07	<u>ā</u> 7
parallel load	v Lic	X	X	X	L	L H	L - L H - H	L H	H
serial shift	Н	L	†	l h	X	L H	q0-q5 q0-q5	96 96	₹ 46 46
hold "do nothing"	Н	Н	X	X	Х	90	91-96	97	97

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

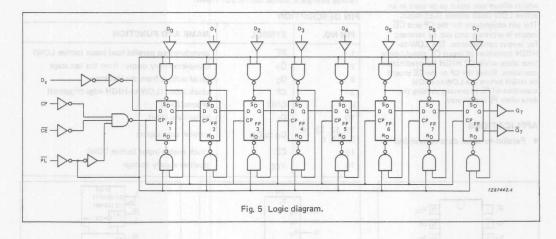
L = LOW voltage level

I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition

X = don't care

↑ = LOW-to-HIGH clock transition



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					Tamb	(°C)					TEST COND	ITIONS
0.44004	y specifications.		ni navi	g al f. N	74H	C	et logal	al insvi		Treater	additional qu	
SYMBOL	PARAMETER	10	+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFOR	MS
		min.	typ.	max.	min.	max.	min.	max.		- GI	UNIT LO	
tPHL/ tPLH	propagation delay $\overline{\text{CE}}$, CP to Ω_7 , $\overline{\Omega}_7$		52 19 15	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 6	n0 0 10
tPHL/	propagation delay PL to Ω ₇ , Ω̄ ₇		50 18 14	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 7	30 38
^t PHL/ ^t PLH	propagation delay D ₇ to Ω_7 , $\overline{\Omega}_7$		36 13 10	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 8	
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6	
tW	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6	
tw	parallel load pulse width; LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
^t rem	removal time PL to CP, CE	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7	
^t su	set-up time D _S to CP, CE	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9	
t _{su}	set-up time CE to CP; CP to CE	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9	
^t su	set-up time D _n to PL	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10	
^t h	hold time D _s to CP, CE D _n to PL	5 5 5	6 2 2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 9	
^t h	hold time CE to CP CP to CE	5 5 5	-17 -6 -5		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 9	
f _{max}	maximum clock pulse frequency	6 30 35	17 51 61		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

						UNIT LOA	INPUT
					2.0 4.5 8.0	0.35 0.35 0.65	D _n D _s CP
					2:0 4.6 6.0	0.65 0.65	CE PL

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	\/				T _{amb} (°C)					TEST CONDITIONS	
					74H0	т	7		UNIT	V	WAVEFORMS	
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
	4.000	min.	typ.	max.	min.	max.	min.	max.		1		
t _{PHL} / —	propagation delay CE, CP to Q ₇ , Q ₇		17	34		43		51	ns	4.5	Fig. 6	
^t PHL/ ^t PLH	propagation delay \overline{PL} to Ω_7 , $\overline{\Omega}_7$		20	40		50		60	ns	4.5	Fig. 7	
tPHL/	propagation delay D_7 to Q_7 , \overline{Q}_7	revadi Videln, t acion e	14	28		35	to e clock nd the	42	ns	4.5	Fig. 8	
t _{THL} / t _{TLH}	output transition time	sas Juli	7	15		19		22	ns	4.5	Fig. 6	
tw	clock pulse width HIGH or LOW	16	6		20		24		ns	4.5	Fig. 6	
tw	parallel load pulse width; LOW	20	9		25		30		ns	4.5	Fig. 7	
^t rem	removal time PL to CP, CE	20	8	las "L	25		30	1	ns	4.5	Fig. 7	
tsu	set-up time D _S to CP, CE	20	2		25		30	17	ns	4.5	Fig. 9	
t _{su}	set-up time CE to CP; CP to CE	20	7	B soil	25		30	1	ns	4.5	Fig. 9	
t _{su}	set-up time D _n to PL	20	10		25		30	sugni s delevs	ns	4.5	Fig. 10	
thunni xxx	hold time D _S to CP, CE; D _n to PL	7	L1		9		11		ns	4.5	Fig. 9	
^t h	hold time CE to CP, CP to CE	0	-7		0		0		ns	4.5	Fig. 9	
fmax at	maximum clock pulse frequency	26	44		21		17	1	MHz	4.5	Fig. 6	

AC WAVEFORMS

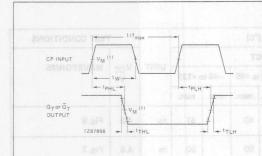


Fig. 6 Waveforms showing the clock (CP) to output $(Q_7 \text{ or } \overline{Q}_7)$ propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

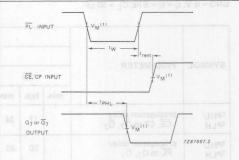


Fig. 7 Waveforms showing the parallel load (\overline{PL}) pulse width, the parallel load to output (Ω_7 or $\overline{\Omega}_7$) propagation delays, the parallel load to clock (\overline{CP}) and clock enable (\overline{CE}) removal time.

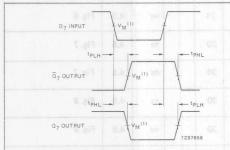


Fig. 8 Waveforms showing the data input (D_n) to output $(Q_7$ or $\overline{Q}_7)$ propagation delays when \overline{PL} is LOW.

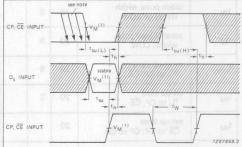


Fig. 9 Waveforms showing the set-up and hold times from the serial data input (D_s) to the clock (CP) and clock enable $(\overline{\mathbb{CE}})$ inputs, from the clock enable input $(\overline{\mathbb{CE}})$ to the clock input (CP) and from the clock input (CP) to the clock enable input $(\overline{\mathbb{CE}})$.

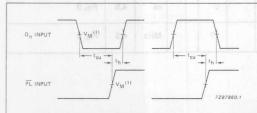


Fig. 10 Waveforms showing the set-up and hold times from the data inputs (D_n) to the parallel load input (PL).

Note to Figs 6 and 7

The changing to output assumes internal Q_6 opposite state from Q_7 .

Note to Fig. 9

 $\overline{\text{CE}}$ may change only from HIGH-to-LOW while CP is LOW.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER

FEATURES

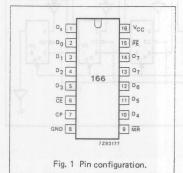
- Synchronous parallel-to-serial applications
- Synchronous serial data input for easy expansion
- · Clock enable for "do nothing" mode
- Asynchronous master reset
- For asynchronous parallel data load see "165"
- Output capability: standard
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT166 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT166 are 8-bit shift registers which have a fully synchronous serial or parallel data entry selected by an active LOW parallel enable (PE) input. When PE is LOW one set-up time prior to the LOW-to-HIGH clock transition, parallel data is entered into the register. When PE is HIGH, data is entered into the internal bit position Q₀ from serial data input (Ds), and the remaining bits are shifted one place to the right $(Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positivegoing clock transition.

This feature allows parallel-to-serial converter expansion by tying the Ω_7 output to the D $_8$ input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable (CE) input. The pin assignment for the CP and CE inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input CE should only take place while CP is HIGH for predictable operation. A LOW on the master reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.



	2.0.445752	CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER MINISTER	CONDITIONS	нс	нст	ONT	
^t PHL [/] ^t PLH	propagation delay <u>CP</u> to Q ₇ <u>MR</u> to Q ₇	C _L = 15 pF - V _{CC} = 5 V	15 14	20 19	ns ns	
fmax	maximum clock frequency		63	50	MHz	
CI	input capacitance	THE TUO-LAIST	3.5	3.5	pF	
CPD	power dissipation capacitance per package	notes 1 and 2	41	41	pF	

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x VCC^2 x f_i + Σ (CL x VCC^2 x f_o) where:

f; = input frequency in MHz f_O = output frequency in MHz CLU = output load capacitance in pF VCC = supply voltage in V

 Σ (C_L x V_{CC}² x f₀) = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

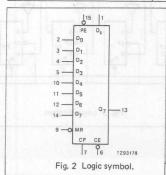
PACKAGE OUTLINES

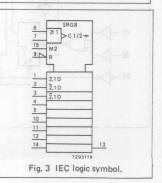
16-lead DIL; plastic (SOT38Z).

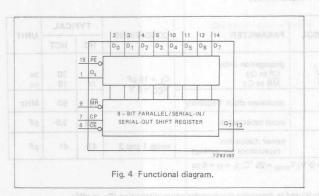
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	Ds	serial data input
2, 3, 4, 5, 10, 11, 12, 14	D ₀ to D ₇	parallel data inputs
6	CE	clock enable input (active LOW)
7	CP	clock input (LOW-to-HIGH edge-triggered)
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active LOW)
13	Q ₇	serial output from the last stage
15	PE	parallel enable input (active LOW)
16	Vcc	positive supply voltage







FUNCTION TABLE

Registration of the Park Registration of the P	1300	graci	INPL	JTS		Q _n R	EGISTER	OUTPUT
OPERATING MODES	PE	CE	СР	Ds	D ₀ -D ₇	α ₀	Q ₁ -Q ₆	07
parallel load	1	1 1	1	X	l - l h - h	L H	L - L H - H	L H
serial shift	h h	1	↑	l h	X - X X - X	L H	q0- q5 q0- q5	96 96
hold "do nothing"	X	h	X	X	X - X	90	91-96	97

H = HIGH voltage level

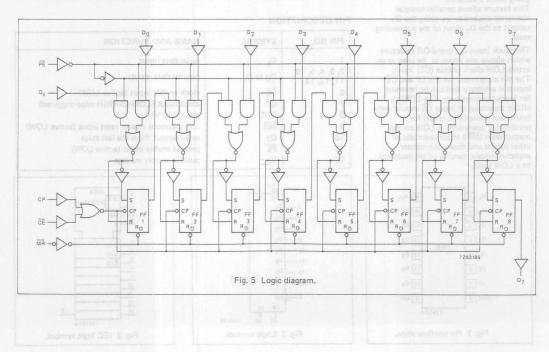
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition X = don't care

↑ = LOW-to-HIGH CP transition





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

			-	110	T _{amb} (°C)					TEST CONDITIONS	
01/140.01					74HC				UNIT	- 60		
SYMBOL	PARAMETER		+25		-401	to +85	-40t	-40 to +125		VCC		
		min.	typ.	max.	min.	max.	min.	max.		.0		
tPHL/	propagation delay CP to Q ₇		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
^t PHL	propagation delay MR to Q7	J. k	47 17 14	160 32 27		200 40 34	10% -	240 48 41	ns	2.0 4.5 6.0	Fig. 8	
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7	
tW	clock pulse width HIGH or LOW	80 16 14	17 6 5	33085, 3	100 20 17	Stine	120 24 20	pidV1	ns	2.0 4.5 6.0	Fig. 7	
tw	master reset pulse width LOW	100 20 17	25 9 7		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8	
^t rem	removal time MR to CP	0 0 0	-19 -7 -6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 8	
t _{su}	set-up time D _n , CE to CP	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9	
t _{su}	set-up time PE to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8	
^t h	hold time D _n , CE to CP	2 2 2	-8 -3 -2		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 8	
^t h	hold time PE to CP	0 0 0	-28 -10 -8		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 9	
f _{max}	maximum clock pulse frequency	6.0 30 35	19 57 68		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D ₀ to D ₇	0.35
Ds	0.35
CP	0.80
CE	0.80
MR	0.40
PE	0.60

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} ((°C)					TEST CONDITIONS
	PARAMETER				74HC	т			UNIT	N. 1	WALKERDAM
	put (LOW CE), the glock enab	PO EU	+25		-40 t		-40 to +125		ONT	V _{CC}	WAVEFORMS
arts est	ond the parellel enable input ock (GP).	min.	typ.	max.	min.	max.	min.	max.		AT -	
tPHL/	propagation delay CP to Q ₇		23	40		50		60	ns	4.5	Fig. 7
^t PHL	propagation delay MR to Q ₇	O .	22	40		50	44	60	ns	4.5	Fig. 8
t _{THL} /	output transition time		7	15		19		22	ns	4.5	Fig. 7
tW	clock pulse width	20	9		25		30		ns	4.5	Fig. 7
tw	master reset pulse width LOW	25	11		31		38		ns	4.5	Fig. 8
^t rem	removal time MR to CP	0	-7		0	1	0		ns	4.5	Fig. 8
t _{su}	set-up time D _n , CE to CP	16	8		20		24		ns	4.5	Fig. 9
t _{su}	set-up time PE to CP	30	15		38		45		ns	4.5	Fig. 8 Mayor GA or st
^t h	hold time D _n , CE to CP	0	-3		0		0		ns	4.5	Fig. 9
^t h	hold time PE to CP	0	-13		0		0		ns	4.5	Fig. 9
f _{max}	maximum clock pulse width	25	45		20		17		MHz	4.5	Fig. 7

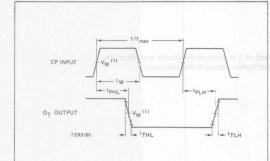


Fig. 7 Waveforms showing the clock (CP) to output (Q₇) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

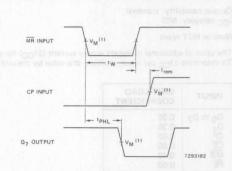


Fig. 8 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q7) propagation delay and the master reset to clock (CP) removal time.

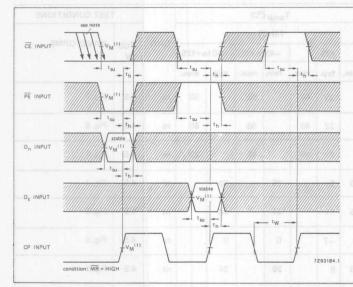


Fig. 9 Waveforms showing the set-up and hold times from the serial data input (D_s) , the data inputs (D_n) , the clock enable input $(LOW \ \overline{CE})$, the clock enable input \overline{CE} and the parallel enable input to the clock (CP).

Note to Fig. 7

The changing to output assumes internal Q_6 opposite state from Q_7 .

Note to Figs 7, 8 and 9

The number of clock pulses required between the tPLH and tPHL measurements can be determined from the function table.

Note to Fig. 9

CE may change only from HIGH-to-LOW while CP is LOW.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

QUAD D-TYPE FLIP-FLOP; POSITIVE-EDGE TRIGGER; 3-STATE

FEATURES

- · Gated input enable for hold (do nothing) mode
- Gated output enable control
- Edge-triggered D-type register
- Asynchronous master reset
- · Output capability: bus driver
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT173 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT173 are 4-bit parallel load registers with clock enable control, 3-state buffered outputs (Q_0 to Q_3) and master reset (MR).

When the two data enable inputs (E1 and E2) are LOW, the data on the Dn inputs is loaded into the register synchronously with the LOW-to-HIGH clock (CP) transition. When one or both En inputs are HIGH one set-up time prior to the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and clock enable inputs are fully edge-triggered and must be stable only one set-up time prior to the LOW-to-HIGH clock transition.

The master reset input (MR) is an active HIGH asynchronous input. When MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-state output buffers are controlled by a 2-input NOR gate. When both output enable inputs (\overline{OE}_1 and \overline{OE}_2) are LOW, the data in the register is presented to the Qn outputs. When one or both \overline{OE}_n inputs are HIGH, the outputs are forced to a high impedance OFF-state. The 3-state output buffers are completely independent of the register operation; the \overline{OE}_n transition does not affect the clock and reset operations.

	FUNCTION TABLE		TYF		
SYMBOL	PARAMETER MARAMETER	CONDITIONS	НС	нст	UNIT
^t PHL [/] ^t PLH	propagation delay CP to Q _n MR to Q _n	C _L = 15 pF V _{CC} = 5 V	17 13	17 17	ns ns
f _{max}	maximum clock frequency		88	88	MHz
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	20	pF

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD \times VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

f; = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$ 2. For HC the condition is VI = GND to VCC

For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 V$

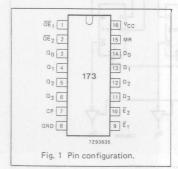
PACKAGE OUTLINES

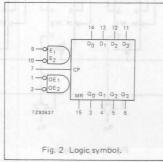
16-lead DIL; plastic (SOT38Z).

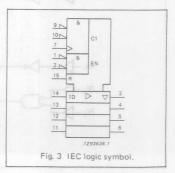
16-lead mini-pack; plastic (SO16; SOT109A).

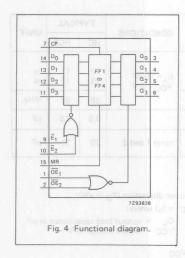
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	OE ₁ , OE ₂	output enable input (active LOW)
3, 4, 5, 6	Q ₀ to Q ₃	3-state flip-flop outputs
7	CP	clock input (LOW-to-HIGH, edge-triggered)
8	GND	ground (0 V)
9, 10	$\overline{E}_1, \overline{E}_2$	data enable inputs (active LOW)
14, 13, 12, 11	D ₀ to D ₃	data inputs
15	MR	asynchronous master reset (active HIGH)
16	Vcc	positive supply voltage









FUNCTION TABLE

PROBLEM PART A PART OF THE PAR		1	OUTPUTS			
REGISTER OPERATING MODES	MR	СР	Ē ₁	E ₂	Dn	Q _n (register)
reset (clear)	Н	Х	X	X	X	e Edga-trigge a Asvaelusva
parallel load	L	† †	ngent I	apd:	h	Output can IcdHortegor
hold (no change)	L	X	h X	X	X	q _n q _n

3-STATE BUFFER	INPL	OUTPUTS					
OPERATING MODES	Q _n (register)	ŌE ₁	ŌE ₂	00	01 0		03
read v + D > 200 x 100 x	Hoge (offer to	L	L	L	L	L
disabled A TRANSPORT DESCRIPTION OF THE PROPERTY OF THE PROPER	X	H	Х	Z	Z	Z	Z

H = HIGH voltage level

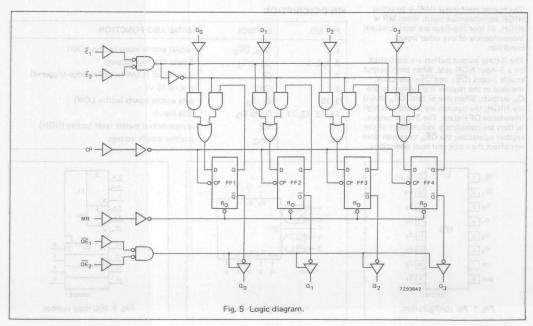
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

 I = LOW voltage level
 I = LOW volta one set-up time prior to the LOW-to-HIGH CP transition

X = don't care

Z = high impedance OFF-state

↑ = LOW-to-HIGH CP transition



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC and an arrange of the book from a not (2016) internal vigous messaling landitions to such art

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

W I					T _{amb} (°C)				THE	TEST CONDIT	TIONS
01/14001	OADAMETED.				74H				UNIT	Vcc	WAVEFORMS	
SYMBOL	PARAMETER		+25 -40		-40	to +85 -40 to +125		ONT	V	0.40	25,15	
		min.	typ.	max.	min.	max.	min.	max.			OP 0:25 CP 1:00	
tPHL/	propagation delay CP to Q _n		55 20 16	175 35 30		220 44 37		265 53 45	ns and	2.0 4.5 6.0	Fig. 6	
^t PHL	propagation delay MR to Q _n		44 16 13	150 30 26	(01) de	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
t _{PZH} / t _{PZL}	3-state output enable time $\overline{\text{OE}}_n$ to Ω_n	123	52 19 15	150 30 26	or Bla	190 38 33	85	225 45 38	ns	2.0 4.5 6.0	Fig. 8	JOBNIYS
^t PHZ/	3-state output disable time $\overline{\text{OE}}_n$ to Ω_n	G	52 19 15	150 30 26	08	190 38 33	0 40	225 45 38	ns	2.0 4.5 6.0	Fig. 8	18 101 /THd;
tTHL/ tTLH	output transition time	j b	14 5 4	60 12 10	44	75 15 13	8 0	90 18 15	ns	2.0 4.5 6.0	Fig. 6]Hd;
tw	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6	
tw	master reset pulse width; HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	PLZ THE
^t rem	removal time MR to CP	60 12 10	-8 -3 -2	2	75 15 13	S	90 18 15	ai	ns	2.0 4.5 6.0	Fig. 7	M ₃
t _{su}	set-up time E _n to CP	100 20 17	33 12 10	Bt	125 25 21		150 30 26	0 -01 - ST	ns	2.0 4.5 6.0	Fig. 9	W
t _{su}	set-up time D _n to CP	60 12 10	17 6 5	16	75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 9	os!
th	hold time E _n to CP	0 0 0	-17 -6 -5	N.	0 0		0 0 0	12	ns	2.0 4.5 6.0	Fig. 9	ns ₃
th	hold time D _n to CP	1 1 1	-11 -4 -3	0	1 1 1	0	1 1 1 &	- 0	ns	2.0 4.5 6.0	Fig. 9	H H
fmax	maximum clock pulse frequency	6.0 30 35	26 80 95	15	4.8 24 28		4.0 20 24	0E	MHz	2.0 4.5 6.0	Fig. 6	×am²

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. ZIR3 DARAHO 3A To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LO	
OE ₁ , OE ₂	0.50	
MR	0.60	
$\overline{E}_1, \overline{E}_2$	0.40	
Dn	0.25	
CP	1.00	

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	2.0 4.5 Fig. 7		122		- 0.	T _{amb} (°C)				yalati	TEST CONDITIONS	14.115
	0.0		88			74HC	Т	90 -8				na ol Am	13.9-3
SYMBOL	PARAMETER 0.5		100	+25	9	-40	to +85	-40 t	o +125	UNIT	V _{CC}		
	0.8		min.	typ.	max.	min.	max.	min.	max.			Bran Hao	124
tPHL/	propagation delay CP to Q _n	en.	88	20	40	35	50	8 2	60	ns	4.5		
^t PHL	propagation delay MR to Qn	an	8	20	37		46	10 4	56	ns	4.5		HIT
tPZH/	3-state output enab	le time		20	35	01	44	1	53 (8	ns	4.5	Fig. 8	
tPHZ/	3-state output disale OE _n to Q _n	ole time		19	30	100	38		45	ns	4.5	Fig. 8	ÄÀ
tTHL/ tTLH	output transition ti	me		5	12		15		19	ns	4.5	Fig. 6	W
t _W	clock pulse width HIGH or LOW	ah.	16	7	90	20	71	24	12	ns	4.5	Fig. 6	men
tw	master reset pulse width; HIGH		15	6	81	19		22	001	ns	4.5	Fig. 7	
^t rem	removal time MR to CP		12	-2	20	15	2	18	71	ns	4.5	Fig. 7	132
t _{su}	set-up time En to CP	80	22	13		28		33	12 6	ns	4.5	Fig. 9	un
t _{su}	set-up time D _n to CP	an	12	7	0	15	0	18		ns	4.5	Fig. 9	
th	hold time En to CP		0	-6	0	0	0	0	- 0	ns	4.5	Fig. 9	
^t h	hold time D _n to CP	26	0	-3		0		0		ns	4.5	Fig. 9	ri
f _{max}	maximum clock pu	ilse	30	80	20	24	2	20	6 0.a 8 08	MHz	4.5	Fig. 6	remi

AC WAVEFORMS

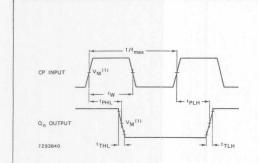


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

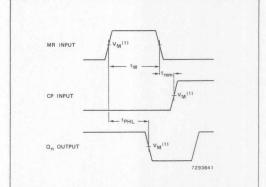


Fig. 7 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_{Π}) propagation delays and the master reset to clock (CP) removal time.

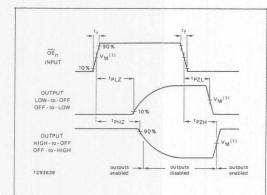


Fig. 8 Waveforms showing the 3-state enable and disable times.

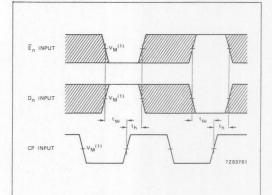


Fig. 9 Waveforms showing the data set-up and hold times from input $(\overline{E}_n,\,D_n)$ to clock (CP).

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_1 = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_1 = GND$ to 3 V.

Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS

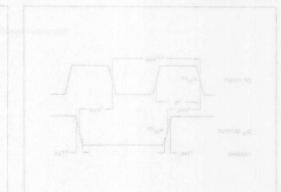


Fig. 6. Waveforms showing the clock ICP! to output (Ω_n) propagation delays, the clock outse validith, dis output transition times and the maximum clock pulse frequency.

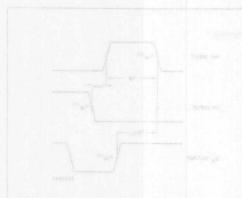


Fig. 7. Waveforms showing the master reset (MR) pulse width the master reset to output (O_{Ω}) propagation delays and the master reset to clock (CP) removal time.

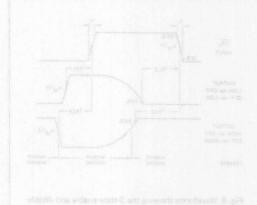


Fig. 8 Waveforms showing the 3-state enable and disable times.



Note to Fig. 9

The shaded steat indicate when the input is permitted to change for predictable output performance.

(1) FIG. : $V_M = 50\%$; $V_1 = 6ND$ to V_{CI} HOT: $V_M = 1.3 M$; $V_1 = 6ND$ to $3 V_2$

HEX D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

FEATURES

- Six edge-triggered D-type flip-flops
- Asynchronous master reset
- · Output capability: standard
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT174 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT174 have six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time prior to the LOW-to-HIGH clock transition, is transferred to the corresponding output of the flip-flop.

A LOW level on the \overline{MR} input forces all outputs LOW, independently of clock or data inputs.

The device is useful for applications requiring true outputs only and clock and master reset inputs that are common to all storage elements.

			TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	нс	нст	Olvii	
^t PHL [/]	propagation delay CP to Qn MR to Qn	C _L = 15 pF V _{CC} = 5 V	17 13	18 17	ns ns	
f _{max}	maximum clock frequency	HA I GA	99	69	MHz	
CI	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	17	17	pF	

$$GND = 0 V; T_{amb} = 25 \,^{\circ}C; t_r = t_f = 6 \text{ ns}$$

Motes

- 1. CPD is used to determine the dynamic power dissipation (P_D in μW):
 - $PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$ where:
 - fi = input frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V
- fo = output frequency in MHz
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}

 For HCT the condition is V_I = GND to V_{CC} 1.5 V

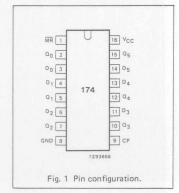
PACKAGE OUTLINES

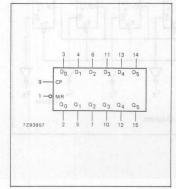
16-lead DIL; plastic (SOT38Z).

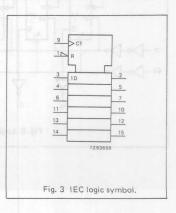
16-lead mini-pack; plastic (SO16; SOT109A).

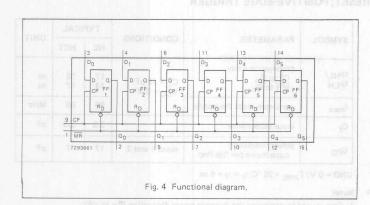
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1 nonlars	MR	asynchronous master reset (active LOW)
2, 5, 7, 10, 12, 15	Q ₀ to Q ₅	flip-flop outputs
3, 4, 6, 11, 13, 14	D ₀ to D ₅	data inputs
8	GND	ground (0 V)
9	CP	clock input (LOW-to-HIGH, edge-triggered)
16	Vcc	positive supply voltage









FUNCTION TABLE

OPERATING MODES -		INPUTS		OUTPUTS
or charma modes	MR	СР	D _n	Qn
reset (clear)	A 91 - 32	×	X	For HCT the or
load "1"	Н	1	Sh Tos	Head DIH. clares
load "0"	Н	1	(0106) pinta	rg ,xdag-inim baal-i L

H = HIGH voltage level

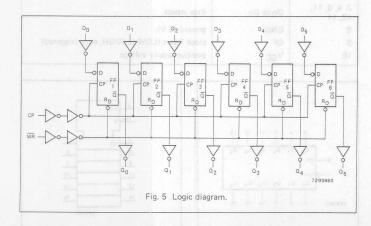
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

X = don't care

↑ = LOW-to-HIGH CP transition



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

					T _{amb} (°C)				T	TEST CONDITIONS	
CVMDOI	DADAMETED				74H	С			UNIT	\/	WAVEFORMS	
SYMBOL	PARAMETER		+25		-40	-40 to +85 -40		-40 to +125		V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/	propagation delay CP to Q _n		55 20 16	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 6 17 = 11 V 0 = OI	
^t PHL	propagation delay MR to Q _n		44 16 13	150 30 26	(a) e	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
t _{THL} / t _{TLH}	output transition time	125	19 7 6	75 15 13	F CT D	95 19 16	28 m -q	110 22 19	ns	2.0 4.5 6.0	Fig. 6	
tw	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6	
tw	master reset pulse width; LOW	80 16 14	12 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
^t rem	removal time MR to CP	5 5 5	-11 -4 -3	98	5 5 5	5	5 5 5	aı	ns	2.0 4.5 6.0	Fig. 7	
t _{su}	set-up time D _n to CP	60 12 10	6 2 2	30	75 15 13	20	90 18 15	1 88	ns	2.0 4.5 6.0	Fig. 8	
th	hold time D _n to CP	3 3 3	-6 -2 -2	20	3 3 3	K I	3 3 3	a at	ns	2.0 4.5 6.0	Fig. 8	
f _{max}	maximum clock pulse frequency	6 30 35	30 90 107	ō	5 24 28	8.	4 20 24		MHz	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D _n	0.25
CP	1.30
MR	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

	2.0	The as			T _{amb} (°C)	DIE A	1			TEST CONDITIONS	3
SYMBOL	PARAMETER	26 3 8	B E		74HC	Т	8 30 3 26	T.	UNIT	Vcc	WAVEFORMS	
STIVIBUL		01	+25		-40 to +85		-40 to +125		ONT	V	WAVEIOINIS	
	4.5 Fig. 6	min.	typ.	max.	min.	max.	min.	max.		tiga troit	ans ti Yuqiuo	
t _{PHL} /	propagation delay CP to Q _n	en i	21	35	0	44		53	ns	4.5	Fig. 6	
^t PHL	propagation delay MR to Ω _n		20	35	0	44	5	53	ns	4.5	Fig. 7	
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6	VV
t _W	clock pulse width HIGH or LOW	16	7	3 -	20	8 1	24		ns	4.5	Fig. 6	mar
t _W	master reset pulse width; LOW	20	7	30	25		30	8 08	ns	4.5	Fig. 7	
t _{rem}	removal time MR to CP	12	-3	E	15	5	18	10 2	ns	4.5	Fig. 7	
t _{su}	set-up time D _n to CP	16	4	8	20	8	24		ns	4.5	Fig. 8	d
th	hold time D _n to CP	5	-3	is in	5	21	5	5 - CE	ns	4.5	Fig. 8	Xam
f _{max}	maximum clock pulse frequency	30	63		24		20		MHz	4.5	Fig. 6	

AC WAVEFORMS

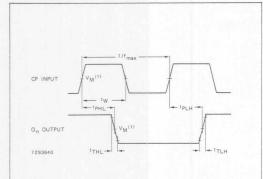


Fig. 6 Waveforms showing the clock (CP) to output (Ω_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

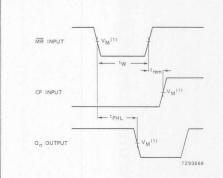


Fig. 7 Waveforms showing the master reset $(\overline{\rm MR})$ pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

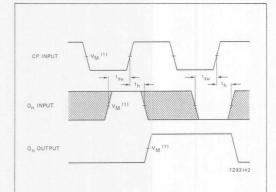


Fig. 8 Waveforms showing the data set-up and hold times for the data input $(\ensuremath{\mathsf{D}}_n).$

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

AC WAVEFORM

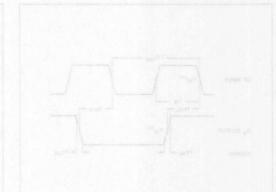


Fig. 6. Veveforms showing the clock ICP) to output (Ω_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.



 $F|_0$? Waveforms showing the master reset (\overline{MR}) pulse width the master reset to output $|\Omega_{\alpha}\rangle$ propagation delays and the master reset moders ($|\Omega_{\gamma}\rangle$ propagation delays and the

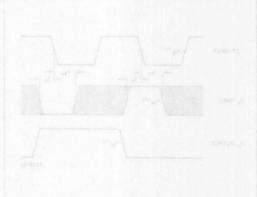


Fig. 8. Waveforers showing the data set up and hold times for the data input (\mathbb{D}_n) .

8 pill or arei

Ins shaded great indicate when the input is parmitted to charge for predictable output performance.

HC : VM = 50%; Vr = 6NB to Vcc.

QUAD D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

FEATURES

Four edge-triggered D flip-flops

Output capability: standard

I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT175 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT175 have four edge-triggered, D-type flip-flops with individual D inputs and both Q and \overline{Q} outputs

The common clock (CP) and master reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

All Q_n outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{\text{MR}}$ input.

The device is useful for applications where both the true and complement outputs are required and the clock and master reset are common to all storage elements.

0)////001	DADAMETER	CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNII	
[†] PHL	propagation delay \underline{CP} to Ω_n , $\overline{\Omega}_n$ \underline{MR} to Ω_n	C _L = 15 pF V _{CC} = 5 V	17 15	16 19	ns ns	
^t PLH	propagation delay CP to Ω_n , $\overline{\Omega}_n$ MR to $\overline{\Omega}_n$	V _{CC} = 5 V	17 15	16 16	ns ns	
fmax	maximum clock frequency		83	54	MHz	
Cl	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	32	34	pF	

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

 $PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$ where:

fi = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_CC

For HCT the condition is $V_1 = GND$ to VCC - 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1 2, 7, 10, 15 3, 6, 11, 14 4, 5, 12, 13	\overline{MR} Q_0 to Q_3 \overline{Q}_0 to \overline{Q}_3 \overline{Q}_0 to \overline{Q}_3	master reset input (active LOW) flip-flop outputs complementary flip-flop outputs data inputs
8 9 16	GND CP VCC	ground (0 V) clock input (LOW-to-HIGH, edge-triggered) positive supply voltage

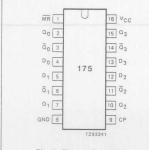
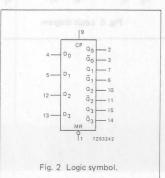
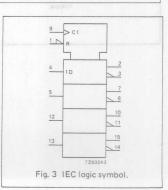
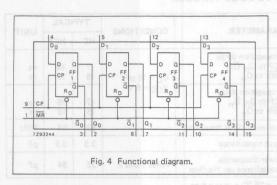


Fig. 1 Pin configuration.







FUNCTION TABLE

ODED A TIMO MODES	onitso	INPUTS	3	OUTPUTS		
OPERATING MODES	MR	СР	Dn	Q _n	$\bar{\mathbf{Q}}_{\mathbf{n}}$	
reset (clear)	grade =	×	X	LIN	Н	
load "1"	Н	1	h	Н	L	
load "0"	H ^{V d}	1 7 30	17 01	PETV	Н	

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the
LOW-to-HIGH CP transition

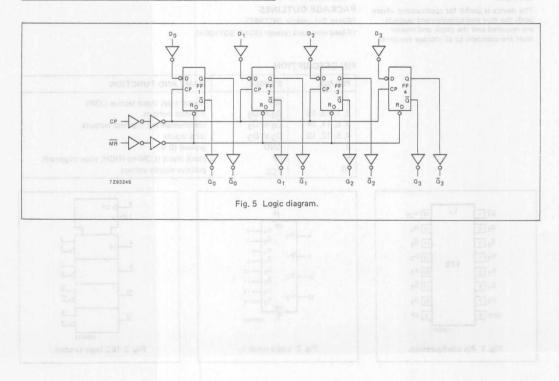
1 = I OW voltage level

L = LOW voltage level

1 = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

1 = LOW-to-HIGH CP transition

X = don't care



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; tr = tf = 6 ns; CL = 50 pF

				T _{amb} (°C)				TEST CONDIT		
				74HC				LINUT			
PARAMETER		+25		-40 t	to +85	-40 t	o +125	UNII	V CC		
	min.	typ.	max.	min.	max.	min.	max.				
propagation delay CP to Ω_n , $\overline{\Omega}_n$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6	0:
propagation delay MR to Ω _n , Ω _n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8	
output transition time	128	19 7 6	75 15 13	TOH - or 04	95 19 16	-25.	110 22 19	ns	2.0 4.5 6.0	Fig. 6	NA.
clock pulse width HIGH or LOW	80 16 14	22 8 6	m .W	100 20 17	to co	120 24 20	ei nim	ns	2.0 4.5 6.0	Fig. 6	itio
master reset pulse width	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	1119
removal time MR to CP	5 5 5	-33 -12 -10		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8	1,19
set-up time D _n to CP	80 16 14	3 1 1		100 20 17		120 24 20		ns	2.0 4.5 6.0		HT
hold time CP to D _n	25 5 4	2 0 0	E	30 6 5	5	40 8 7	20	ns	2.0 4.5 6.0	Fig. 7	W
maximum clock pulse frequency	6.0 30 35	25 75 89	a	4.8 24 28	a	4.0 20 24	2	MHz	2.0 4.5 6.0	Fig. 6	man
	Propagation delay MR to Q _n , Q̄ _n output transition time clock pulse width HIGH or LOW master reset pulse width LOW removal time MR to CP set-up time D _n to CP hold time CP to D _n maximum clock pulse	min. propagation delay CP to Qn, Qn propagation delay MR to Qn, Qn output transition time clock pulse width HIGH or LOW master reset pulse width LOW removal time MR to CP set-up time Dn to CP hold time CP to Dn maximum clock pulse 6.0 30	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	PARAMETER +25 min. typ. max. propagation delay CP to Qn, Qn propagation delay MR to Qn, Qn output transition time clock pulse width HIGH or LOW master reset pulse width LOW removal time MR to CP set-up time Dn to CP hold time CP to Dn maximum clock pulse min. typ. max. 175 183 1830 194 26 19 75 15 6 13 80 19 16 7 14 6 80 19 16 7 14 6 7 14 6 80 19 16 7 14 6 7 14 6 7 14 6 7 14 6 7 14 6 7 14 6 7 14 6 7 14 6 7 14 6 7 14 6 7 14 6 7 14 6 7 14 6 7 14 6 7 14 6 7 14 6 7 14 6 7 14 6 7 14 6 7 16 7 17 80 80 19 16 7 14 10 7 10 80 11 11 11 11 11 11 11 11	PARAMETER +25	Heat Heat	PARAMETER +25	PARAMETER +25	PARAMETER 125	PARAMETER 1	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
MR	1.00
CP	0.60
Dn	0.40

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	0.8	- 81			Tamb (°C)	05 9				TEST CONDITION	IS
	2.0 n 4.5 J. Storie				74HC	т			UNIT	N/CC	WAVEFORMS	
SYMBOL	PARAMETER	+25		-40 to +85		-40 to +125		UNII	V _{CC}	WAVEFORING		
	2,0 ns 4:5 Elo B	min.	typ.	max.	min.	max.	min.	max.		rizbi	clasts galse w	-
t _{PHL} /	propagation delay CP to Q_n , \overline{Q}_n		19	33	6	41		50	ns	4.5	Fig. 6	
^t PHL	propagation delay MR to Q _n		22	38		48		57	ns	4.5	Fig. 8	
^t PLH	propagation delay \overline{MR} to $\overline{\Omega}_n$		19	35		44	12	53	ns	4.5	Fig. 8	ms
t _{THL} /	output transition time		7 0	15		19		22	ns	4.5	Fig. 6	
tw	clock pulse width HIGH or LOW	20	12	30	25		30	5 25	ns	4.5	Fig. 6	
^t W	master reset pulse width LOW	20	11	50 1-1	25	8	30	0 5	ns	4.5	Fig. 8	
^t rem	removal time MR to CP	5	-10	200	5	4 97 99	5	5.0 2 30 7 35 8	ns	4.5	Fig. 8	
t _{su}	set-up time D _n to CP	16	5		20		24		ns	4.5	Fig. 7	
th	hold time CP to D _n	5	0		5		5		ns	4.5	Fig. 7	
f _{max}	maximum clock pulse frequency	25	49		20		17		MHz	4.5	Fig. 6	

AC WAVEFORMS

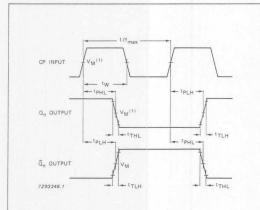


Fig. 6 Waveforms showing the clock (CP) to outputs $(\Omega_n, \overline{\Omega}_n)$ propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

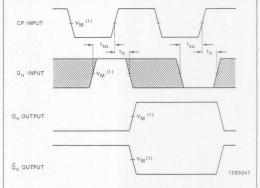


Fig. 7 Waveforms showing the data set-up and hold times for the data input (D_n) .

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

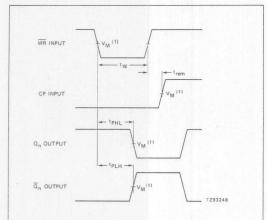
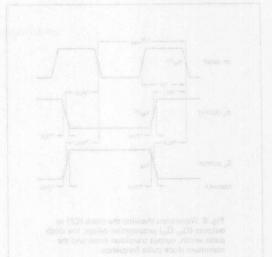


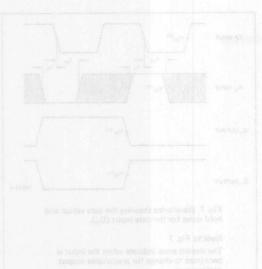
Fig. 8 Waveforms showing the master reset (\overline{MR}) pulse width, the master reset to outputs (Q_n, \overline{Q}_n) propagation delays and the master reset to clock (CP) removal time.

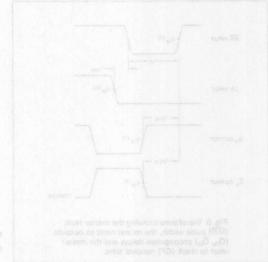
Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

AC WAVEFORM







ts More to AC waveforces

(1) HO : V_M = 50%; V) = 5NO to V_{GC}

(2) HOT: V_M = 1.3.V; V_I = 5ND to V_{GC}

4-BIT ARITHMETIC LOGIC UNIT

FEATURES

- Full carry look-ahead for high-speed arithmetic operation on long words
- Provides 16 arithmetic operations: add, subtract, compare, double, plus 12 others
- Provides all 16 logic operations of two variables:
 EXCLUSIVE-OR, compare, AND, NAND, NOR, OR plus 10 other logic operations
- Output capability: standard,
 A=B open drain
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT181 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT181 are 4-bit high-speed parallel Arithmetic Logic Units (ALU). Controlled by the four function select inputs (So to S3) and the mode control input (M), they can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands (see function table). When the mode control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When M is LOW. the carries are enabled and the "181" performs arithmetic operations on the two 4-bit words. The "181" incorporates full internal carry look-ahead and provides for

SYMBOL	PARAMETER	(DYNCO) MON	TYF	UNIT	
	PARAMETER ON MIS	CONDITIONS	нс	нст	I DINTE
t _{PHL} /	propagation delay \overline{A}_n or \overline{B}_n to $A=B$ C_n to C_{n+4}	C _L = 15 pF V _{CC} = 5 V	28 17	30 21	ns ns
CI	input capacitance	n a simple riogor	3.5	3.5	pF
CPD	power dissipation capacitance per L package	notes 1 and 2	90	92	pF

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

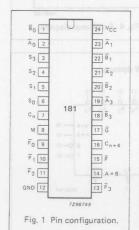
f; = input frequency in MHz f_O = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

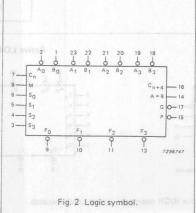
2. For HC the condition is VI = GND to VCC For HCT the condition is VI = GND to VCC - 1.5 V

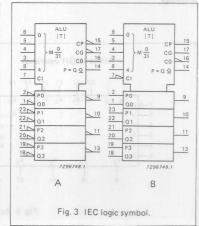
PACKAGE OUTLINES

24-lead DIL; plastic (SOT101A). 24-lead mini-pack; plastic (SO24; SOT137A).



(continued on next page)





GENERAL DESCRIPTION (Cont'd)

either ripple carry between devices using the C_{n+4} output, or for carry look-ahead between packages using the carry propagation (\overline{P}) and carry generate (\overline{G}) signals. \overline{P} and \overline{G} are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the carry output (C_{n+4}) signal to the carry input (C_n) of the next unit.

For high-speed operation the device is used in conjunction with the "182" carry look-ahead circuit. One carry look-ahead package is required for each group of four "181" devices. Carry look-ahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The comparator output (A=B) of the device goes HIGH when all four function outputs (F_0 to F_3) are HIGH and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. A=B is an open collector output and can be wired-AND with other A=B outputs to give a comparison for more than 4 bits. The open drain output A=B should be used with an external pull-up resistor in order to establish a logic HIGH level. The A=B signal can also be used with the C_n+4 signal to indicate A > B and A < B.

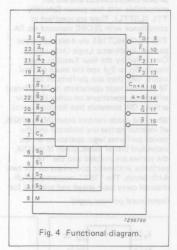
The function table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 22, 20, 18	\overline{B}_0 to \overline{B}_3	operand inputs (active LOW)
2, 23, 21, 19	Ao to A3	operand inputs (active LOW)
6, 5, 4, 3	So to S3	select inputs
7 sonetibed	Cn	carry input
8	M	mode control input
9, 10, 11, 13	Fo to F3	function outputs (active LOW)
12	GND	ground (0 V)
14	A=B	comparator output
15	P	carry propagate output (active LOW)
16	Cn+4	carry output
17	G	carry generate output (active LOW)
24	Vcc	positive supply voltage

Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no under-flow and no carry is generated when there is underflow.

As indicated, the "181" can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands.



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Active LOW operands

Fig. 5 Active HIGH operands -active LOW operands.

FUNCTION TABLES

MOD	E SEL	ECT IN	PUTS	ACTIVE HIGH	I INPUTS AND OUTPUTS
s ₃	s ₂	s ₁	s ₀	LOGIC (M=H)	ARITHMETIC** (M=L; C _n =H)
L L L	L L L	LHH	L H L H	Ā Ā + B ĀB logical 0	A A + B A + B minus 1
	H H H	L H H	L H L H	AB B A ⊕ B AB	A plus AB (A + B) plus AB A minus B minus 1 AB minus 1
H H H	L L L	LLHH	L H L H	A + B A ⊕ B B AB	A plus AB A plus B (A + B) plus AB AB minus 1
H H H	H H H	наг	L H L H	logical 1 A + B A + B A	A plus A* (A + B) plus A (A + B) plus A A minus 1

MOD	DE SELI	ECT IN	PUTS	ACTIVE LOW	INPUTS AND OUTPUTS			
s ₃	s ₂	S ₁	S ₁ S ₀ LOGIC (M=H)			S ₁ S ₀		ARITHMETIC** (M=L; C _n =L)
L L L	L L L	LHH	L H L H	ABABA + B	A minus 1 AB minus 1 AB minus 1 minus 1			
L L L	H H H	L H H	L H L	A + B B A ⊕ B A + B	A plus $(A + \overline{B})$ AB plus $(A + \overline{B})$ A minus B minus 1 $A + \overline{B}$			
H H H H	L L L	LHH	L H L H	ĀB A ⊕ B B A + B	A plus (A + B) A plus B AB plus (A + B) A + B			
H H H	H H H	LHH	ГНГН	logical 0 AB AB A	A plus A* AB plus A AB plus A A			

Notes to the function tables

* Each bit is shifted to the next more significant position.
** Arithmetic operations expressed in 2s complement notation.

H = HIGH voltage level L = LOW voltage level

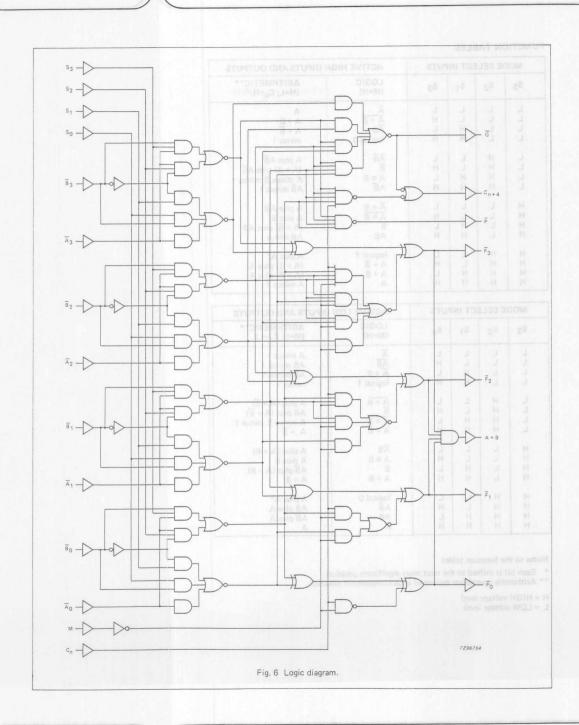


TABLE 1 SUM MODE TEST

_					
Function i	nputs	$S_0 = S_3$	= 4.5 V, I	$M = S_1 =$	$S_2 = 0 \ V$

and the second second	-	TA INPUTS	OTHER INP	JT, SAME BIT	OTHER DA	TA INPUTS	OUTPUT UNDER TEST	
PARAMETER	INPUT	UNDER TEST	Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND	OUTPUT UN	IDER TEST
t _{PLH} /	Āi	establing \$, Ca	B _i A	none	remaining Ā and B	Cn	F _i A	JH9 JHJ9
t _{PLH} / t _{PHL}	Bi	remaining 8, Cm	Ā _i	none and	remaining Ā and B	C _n	F _i	PLH PLH
tpLH/	Āi	nomaining A and E, C _R	B _i snon	none	none snon	remaining A and B, C _n	P	HTIS STH,
t _{PLH} / t _{PHL}	B _i	remaining A and B. C _n	Ā _i soon	none shop	none	remaining A and B, C _n	P B	\H.14 1189
t _{PLH} /	Ā _i	remaining A and	none shore	B _i snon	remaining B	remaining Ā, C _n	G A	PELHA PHIL
t _{PLH} /	Bi	printerras	none	Āi	remaining B	remaining Ā, C _n	G	Ver.25
t _{PLH} /	Āi	8.00	none	Bi	remaining B	remaining Ā, C _n	C _{n+4}	J#19
t _{PLH} /	Bi	E. Ca	none	Āi	remaining B	remaining Ā, C _n	C _{n+4}	72 o
t _{PLH} /	Cn	S. Cn	none	none	all Ā	all B	any F or C _{n+4}	727
	Creed	A and B	shon	ande	18		i A	JH ₂

		TA INPUTS	

TABLE 2 DIFFERENTIAL MODE TEST

Function inputs $S_1 = S_2 = 4.5 \text{ V}, M = S_0 = S_3 = 0 \text{ V}$

	TA INPLITE		OTHER INPL	JT, SAME BIT	OTHER DA	TA INPUTS	OUTDUT UNDER TEST	
PARAMETER	INPUT	UNDER TEST	Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND	OUTPUT UNDER TEST	
t _{PLH} /	Āi	C ₁	none and	B _i	remaining A	remaining B, C _n	Fi A MUST	
t _{PLH} / t _{PHL}	Bi	C _m	Ā _i amama	none snon	remaining Ā	remaining B, C _n	Fi a YELIS	
t _{PLH} / t _{PHL}	Ā _i ¬	remeining A and B, C ₂	none _{enon}	B _i seco	none	remaining A and B, C _n	P A MJ9	
t _{PLH} / t _{PHL}	B _i	recenting A and B, C _n	Ā _i enon	none saon	none	remaining A and B, C _n	P B HJR	
t _{PLH} / t _{PHL}	Ā _i B	remaining Ā. C _n	B _i 8	none	none enon	remaining A and B, C _n	G A 1419	
t _{PLH} / t _{PHL}	Bi	A, Ca	none	Āi	none	remaining Ā and B, C _n	G 2H3	
t _{PLZ} /	Āi	fluiuswa:	none	Bi	remaining Ā	remaining B, C _n	A=B	
t _{PLZ} /	Bi	B.Hs	Ā _i	none	remaining Ā	remaining B, C _n	A=B	
t _{PLH} /	Āi		Bi	none	none	remaining A and B, C _n	C _{n+4}	
t _{PLH} /	\overline{B}_{i}		none	Āi	none	remaining A and B, C _n	C _{n+4}	
t _{PLH} /	Cn		none	none	all A_ and B	none	any F or C _{n+4}	

TABLE 3 LOGIC MODE TEST

Function inputs $M = S_1 = S_2 = 4.5 \text{ V}, S_0 = S_3 = 0 \text{ V}$

PARAMETER	INPUT UNDER TEST	OTHER INPL	JT, SAME BIT	OTHER DA	TA INPUTS	OUTPUT UNDER TEST	
	INFOT ONDER TEST	Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND		
^t PLH [/] ^t PHL	Āi	Bi	none	none	remaining Ā and B, C _n		
tpLH/ tpHL	Bi	Āi	none	none	remaining Ā and B, C _n	F _i	

RATINGS (for A=B output only)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V _O	DC output voltage	-0.5	+7.0	V	
-lok	DC output diode current	xam .nim:	20	mA	for $V_{O} < -0.5 V$
-lo 1 V 0 = N	DC output source or sink current	205	25	mA	for $-0.5 \text{ V} < \text{V}_{0}$

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", except that the V_{OH} values are not valid for open drain output (A=B). They are replaced by I_{OZ} as given below.

Output capability: standard (open drain), excepting $V_{\mbox{\scriptsize OH}}$ $I_{\mbox{\scriptsize CC}}$ category: MSI

Voltages are referenced to GND (ground = 0 V)

V0-52	PARAMETER		T _{amb} (°C)								TEST CONDITIONS		
*Sg=0V:		2.0									Vcc	VIL	OTHER
				+25		-40 to +85		-40 to +125		UNIT	V	do notrep	persis lys
			min.	typ.	max.	min.	max.	min.	max.				
OZ V ZA	HIGH level output leakage current	2,0 4,5 6.0	l land	286 58 48	0.5	230 40 30	5.0	188	10.0	μА	2.0 to 6.0	VIL	note 1 V _O = 0 or 6 V

Note to the DC characteristics

1. The maximum operating output voltage ($V_{O(max)}$) is 6.0 V.

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

			T _{amb} (°C)						V 0 - b	TEST CONDITIONS			
SYMBOL	PARAMETER		74HC							UNIT	V	MODE	OTHER
			+25		-40 to +85		-40 to +125		UNII	V _{CC}	MODE	OTHER	
	> 6V 101		min.	typ.	max.	min.	max.	min.	max.	ETIED HOO	to rouge	0.00	am!-
t _{PHL} //>	propagation delay C _n to C _{n+4}	Am		55 20 16	165 33 28		205 41 35	3119	250 50 43	ns	2.0 4.5 6.0	sum diff	M = 0 V; Fig. 9; Tables 1 and 2
t _{PHL} /	propagation delay C _n to F _n	"anoite:	Minnes	69 25 20	200 40 34	198 18	250 50 43	sverio v	300 60 51	ns	2.0 4.5 6.0	sum diff	M = 0 V; Fig. 9; Tables 1 and 2
^t PHL [/]	propagation delay \overline{A}_n to \overline{G}			72 26 21	210 42 36	56 21	265 53 45	eosige HO	315 63 54	ns	2.0 4.5 6.0	sum	$M = S_1 = S_2 = 0 \text{ V};$ $S_0 = S_3 = 4.5 \text{ V};$ Fig. 7; Table 1
tPHL/ tPLH	propagation delay \overline{B}_n to \overline{G}			77 28 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	sum	$M = S_1 = S_2 = 0 \text{ V};$ $S_0 = S_3 = 4.5 \text{ V};$ Fig. 7; Table 1
tPHL/	propagation delay \overline{A}_n to \overline{G}			76 26 21	215 43 37	(3)	270 54 46		320 65 55	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0 \text{ V};$ $S_1 = S_2 = 4.5 \text{ V};$ Fig. 8; Table 2
^t PHL/	propagation delay \overline{B}_n to \overline{G}		28	77 28 22	240 48 41	8 - co	300 60 51	×8m	360 72 61	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0 \text{ V};$ $S_1 = S_2 = 4.5 \text{ V};$ Fig. 8; Table 2
t _{PHL} /	propagation delay \overline{A}_n to \overline{P}	2	4a, 0	61 22 18	185 37 31	0.3	230 46 39	a.o. i	280 56 48	ns	2.0 4.5 6.0	sum sum	$M = S_1 = S_2 = 0 \text{ V};$ $S_0 = S_3 = 4.5 \text{ V};$ Fig. 7; Table 1
^t PHL [/]	propagation delay \overline{B}_n to \overline{P}			63 23 18	195 39 33		245 49 42	i nav	295 59 50	ns	2.0 4.5 6.0	sum	$M = S_1 = S_2 = 0 \text{ V};$ $S_0 = S_3 = 4.5 \text{ V};$ Fig. 7; Table 1
^t PHL [/]	propagation delay \overline{A}_n to \overline{P}			55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0 \text{ V};$ $S_1 = S_2 = 4.5 \text{ V};$ Fig. 8; Table 2
t _{PHL} /	propagation delay \overline{B}_n to \overline{P}			63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0 \text{ V};$ $S_1 = S_2 = 4.5 \text{ V};$ Fig. 8; Table 2
t _{PHL} /	propagation delay \overline{A}_i to \overline{F}_i			77 28 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	sum	$M = S_1 = S_2 = 0 \text{ V};$ $S_0 = S_3 = 4.5 \text{ V};$ Fig. 7; Table 1
tPHL/	propagation delay $\overline{B_i}$ to $\overline{F_i}$			85 31 25	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	sum	$M = S_1 = S_2 = 0 \text{ V};$ $S_0 = S_3 = 4.5 \text{ V};$ Fig. 7; Table 1
tpHL/	propagation delay \overline{A}_i to \overline{F}_i			77 28 22	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0 \text{ V};$ $S_1 = S_2 = 4.5 \text{ V};$ Fig. 8; Table 2
^t PHL [/]	propagation delay $\overline{B_i}$ to $\overline{F_i}$			83 31 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0 \text{ V};$ $S_1 = S_2 = 4.5 \text{ V};$ Fig. 8; Table 2
^t PHL [/]	propagation delay \overline{A}_i to \overline{F}_i			74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	logic	M = 4.5 V; Fig. 8; Table 3
t _{PHL} /	propagation delay \overline{B}_i to \overline{F}_i			83 30 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	logic	M = 4.5 V; Fig. 8; Table 3

AC CHARACTERISTICS FOR 74HC (Cont'd)

	cations", except that the V _Q	15051	Viims:	meters related to	T _{amb} (°C)	becelo	innet o	NT 18=	aygang L) Jugn	EST COM	NDITIONS
OVMDOL	242445752				74H	С			repres un	and nes	14005	or willing ones to on
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	MODE	OTHER
		min.	typ.	max.	min.	max.	min.	max.	AV 0 = b	tuong) 6	M2 or ba	onersiter om repasic
t _{PHL} /	propagation delay Ā _n to C _{n+4}	MA -	80 29 23	235 47 40	197	295 59 50		355 71 60	ns	2.0 4.5 6.0	sum	$M = S_1 = S_2 = 0 \text{ V};$ $S_0 = S_3 = 4.5 \text{ V};$ Fig. 8; Table 1
t _{PHL} /	propagation delay B _n to C _{n+4}		80 29 23	235 47 40	osem osem	295 59 50	JXSHII	355 71 60	ns	2.0 4.5 6.0	sum	$M = S_1 = S_2 = 0 \text{ V};$ $S_0 = S_3 = 4.5 \text{ V};$ Fig. 8; Table 1
tPHL/	propagation delay Ā _n to C _{n+4}	An	77 28 22	235 47 40	0.8	295 59 50	2.0	355 71 60	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0 \text{ V};$ $S_1 = S_2 = 4.5 \text{ V};$ Fig. 10; Table 2
^t PHL/ ^t PLH	propagation delay B _n to C _{n+4}		85 31 25	255 51 43		320 64 54	0.0 ai	385 77 65	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0 \text{ V};$ $S_1 = S_2 = 4.5 \text{ V};$ Fig. 10; Table 2
^t PZL/ ^t PLZ	propagation delay Ā _n to A=B	ylime	80 29 23	245 49 42	if to t	305 61 52	1 101	370 74 63	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0 \text{ V};$ $S_1 = S_2 = 4.5 \text{ V};$ Fig. 11; Table 2
^t PZL/	propagation delay B _n to A=B		88 32 26	270 54 46		340 68 58		405 81 69	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0 \text{ V};$ $S_1 = S_2 = 4.5 \text{ V};$ Fig. 11; Table 2
t _{PHL} /	propagation delay \overline{A}_n to \overline{F}_n		83 30 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	sum	
t _{PHL} /	propagation delay B _n to F _n		85 31 25	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	sum	$M = S_1 = S_2 = 0 \text{ V};$ $S_0 = S_3 = 4.5 \text{ V};$ Fig. 7; Table 1
t _{PHL} /	propagation delay Ā _n to F _n	CART.	77 28 22	240 48 41	- 12	300 60 51		360 72 61	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0 \text{ V};$ $S_1 = S_2 = 4.5 \text{ V};$ Fig. 8; Table 2
t _{PHL} /	propagation delay B _n to F _n		88 32 26	275 55 47	Life to	345 69 59	akm	415 83 71	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0 \text{ V};$ $S_1 = S_2 = 4,5 \text{ V};$ Fig. 8; Table 2
t _{THL} /	output transition time	en i	19 7 6	75 15 13	£8	95 19 16	42	110 22 19	ns	2.0 4.5 6.0	sion dela	note 1; Figs 7 and 11

Note to the AC characteristics

1. For the open drain output (A=B) only t_{THL} is valid.

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", except that the V_{OH} values are not valid for open drain output (A=B). They are replaced by I_{OZ} as given below.

Output capability: standard (open drain), excepting $V_{\mbox{OH}}$ $I_{\mbox{CC}}$ category: MSI

Voltages are referenced to GND (ground = 0 V)

5V-0=e8					T _{amb} (°C)		68		Т	EST CO	NDITIONS
SYMBOL		27.1	171		74HC		47	28	UNIT	Vcc	VIL	OTHER
.V0=c8		+25		-40 to +85		-40 to +125			V	sleb mort	ipsqotq \Je	
		min.	typ.	max.	min.	max.	min.	max.	R.E.		ten	or 99 to
loz	HIGH level output leakage current	271	355 71 60	0.5	296 80 80	5.0	235 47 40	10.0	μА	2.0 to 6.0	VIL	note 1; V _O = 0 or 6 V

Note to the DC characteristics

1. The maximum operating output voltage ($V_{O(max)}$) is 6.0 V.

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

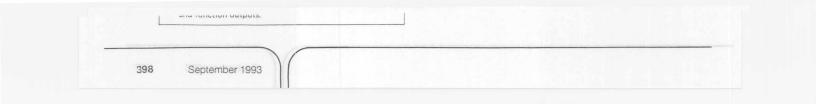
INPUT	UNIT LOAD COEFFICIENT
$\frac{C_n}{\overline{A}_n}, \frac{M}{\overline{B}_n}$	0.50 0.75 1.00

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

						T _{amb} (°C)				Т	EST COM	NDITIONS
SYMBOL	PARAMETER		281	19		74HC	т	14	22	UNIT	Vcc	MODE	OTHER
	= 02 = M = 12 = 12 Hip			+25		-40	to +85	-40 to	+125	Olvii	V	sieb no	Spagong \JH
		0.0	min.	typ.	max.	min.	max.	min.	max.			n	UH Bato
tPHL/	propagation delay C _n to C _{n+4}	2.0	en	25	42	19	53	15	63	ns	4.5	sum diff	M = 0 V; Fig. 9; Tables 1 and 2
t _{PHL} /	propagation delay C_n to \overline{F}_n			28	48		60		72	ns	4.5	sum diff	M = 0 V; Fig. 9; Tables 1 and 2
t _{PHL} /	$\frac{\text{propagation delay}}{\overline{A}_{n} \text{ to } \overline{G}}$			31	54		68		81	ns	4.5	sum	$M = S_1 = S_2 = 0 \text{ V};$ $S_0 = S_3 = 4.5 \text{ V};$ Fig. 7; Table 1
t _{PHL} /	$\frac{\text{propagation delay}}{\overline{B}_n \text{ to } \overline{G}}$			32	54		68		81	ns	4.5	sum	$M = S_1 = S_2 = 0 \text{ V};$ $S_0 = S_3 = 4.5 \text{ V};$ Fig. 7; Table 1
t _{PHL} /	$\frac{\text{propagation delay}}{\overline{A}_n \text{ to } \overline{G}}$			31	54		68		81	ns	4.5	diff	$M = S_0 = S_3 = 0 \text{ V};$ $S_1 = S_2 = 4.5 \text{ V};$ Fig. 8; Table 2
^t PHL [/]	propagation delay \overline{B}_n to \overline{G}			31	54		68		81	ns	4.5	diff	M = S ₀ = S ₃ = 0 V; S ₁ = S ₂ = 4.5 V; Fig. 8; Table 2

	TEST CONDITION				T _{amb} (°C)				1	EST COM	IDITIONS
					74HC	TIAS				.,	MODE	OTHER
SYMBOL	PARAMETER	U -	+25	08-	-40	to +85	-40 t	o +125	UNIT	VCC V	MODE	OTHER
		min.	typ.	max.	min.	max.	min.	max.	m			
t _{PHL} /	propagation delay \overline{A}_n to \overline{P}	in I	23	41	70	51	82	62	ns	4.5	sum	$M = S_1 = S_2 = 0 \text{ V}$ $S_0 = S_3 = 4.5 \text{ V}$; Fig. 7; Table 1
t _{PHL} /	propagation delay	en	24	41	0.7	51	tea.	62	ns	4.5	sum	$M = S_1 = S_2 = 0 \text{ V}$ $S_0 = S_3 = 4.5 \text{ V}$; Fig. 7; Table 1
tPHL/	propagation delay Ā _n to P	an l	23	40	70	50	aa	60	ns	4.5	diff	$M = S_0 = S_3 = 0 \text{ V}$ $S_1 = S_2 = 4.5 \text{ V};$ Fig. 8; Table 2
tPHL/	propagation delay		23	40	ex.	50	88	60	ns	4.5	diff	$M = S_0 = S_3 = 0 \text{ V}$ $S_1 = S_2 = 4.5 \text{ V};$ Fig. 8; Table 2
tPHL/ book	propagation delay Ā _i to F _i	an	33	58	-81	73	at	87	ns	4.5	sum	$M = S_1 = S_2 = 0 \text{ V}$ $S_0 = S_3 = 4.5 \text{ V};$ Fig. 7; Table 1
^t PHL [/] ^t PLH	propagation delay \overline{B}_i to \overline{F}_i		34	58		73		87	ns	4.5	sum	$M = S_1 = S_2 = 0 \text{ V}$ $S_0 = S_3 = 4.5 \text{ V}$; Fig. 7; Table 1
^t PHL/ ^t PLH	propagation delay Ā _i to F _i		33	57		71		86	ns	4.5	diff	$M = S_0 = S_3 = 0 \text{ V}$ $S_1 = S_2 = 4.5 \text{ V}$; Fig. 8; Table 2
^t PHL/ ^t PLH	propagation delay		33	57		71		86	ns	4.5	diff	$M = S_0 = S_3 = 0 \text{ V}$ $S_1 = S_2 = 4.5 \text{ V};$ Fig. 8; Table 2
^t PHL [/] ^t PLH	propagation delay Ā _i to F _i		29	54		68		81	ns	4.5	logic	M = 4.5 V; Fig. 8; Table 3
t _{PHL} /	propagation delay B _i to F _i		33	54		68		81	ns	4.5	logic	M = 4.5 V; Fig. 8; Table 3
^t PHL/ ^t PLH	propagation delay Ā _n to C _{n+4}		30	53		66	Jim'	80	ns	4.5	sum	$M = S_1 = S_2 = 0 \text{ V}$ $S_0 = S_3 = 4.5 \text{ V}$; Fig. 8; Table 1
^t PHL [/]	propagation delay B _n to C _{n+4}		31	53		66	togtuo steneg smit nă	80	ns	4.5	sum	$M = S_1 = S_2 = 0 \text{ V}$ $S_0 = S_3 = 4.5 \text{ V}$; Fig. 8; Table 1
^t PHL [/]	propagation delay An to C _{n+4}	STUDI	30	55		69		83	ns	4.5	diff	$M = S_0 = S_3 = 0 \text{ V}$ $S_1 = S_2 = 4.5 \text{ V}$; Fig. 10; Table 2
^t PHL [/]	propagation delay B _n to C _{n+4}		34	55		69		83	ns	4.5	diff	$M = S_0 = S_3 = 0 \text{ V}$ $S_1 = S_2 = 4.5 \text{ V}$; Fig. 10; Table 2
^t PZL [/]	propagation delay Ā _n to A=B		34	60		75		90	ns	4.5	diff	M = S ₀ = S ₃ = 0 V S ₁ = S ₂ = 4.5 V; Fig. 11; Table 2
t _{PZL} /	propagation delay \overline{B}_{D} to A=B		35	60		75	MARIA	90	ns	4.5	diff	M = S ₀ = S ₃ = 0 V S ₁ = S ₂ = 4.5 V; Fig. 11; Table 2



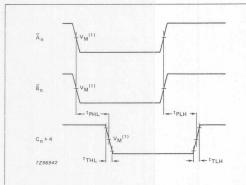


Fig. 10 Propagation delays for operands to carry output.

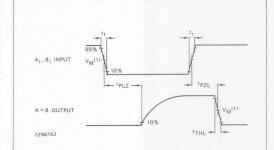
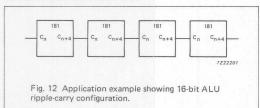


Fig. 11 Waveforms showing the input (A_j, B_j) to output (A=B) propagation delays and output transition time of the open drain output (A=B).

Note to AC waveforms

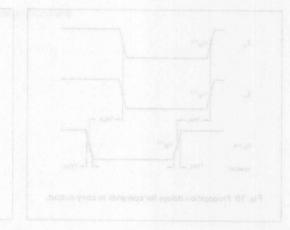
(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION



Note to Fig. 12

A and B inputs and F outputs of "181" are not shown.



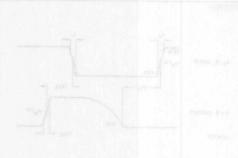


Fig. 11 Wavelarms showing the input IA; B;) to output IA=B) properprior delays and output transition time of the open drain output (A=B).

Note to AC waveforms

(1) HE : VM = 50%; V1 = GND to VCC

NOT: Ver = 1.3 V, VI = GND to 3 V

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Note to Fig. 12

A and 6 inputs and F putputs of "181" are not shown,

LOOK-AHEAD CARRY GENERATOR

FEATURES

- Provides carry look-ahead across a group of four ALU's
- Multi-level look-ahead for high-speed arithmetic operation over long word
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT182 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT182 carry look-ahead generators accept up to four pairs of active LOW carry propagate (P_0, P_1, P_2, P_3) and carry generate (G_0, G_1, G_2, G_3) signals and an active HIGH carry input (Cn). The devices provide anticipated active HIGH carries (Cn+x, Cn+y, Cn+z) across four groups of binary adders.

The "182" also has active LOW carry propagate (P) and carry generate (G) outputs which may be used for further levels of look-ahead.

The logic equations provided at the

$$C_{n+x} = G_0 + P_0C_n$$

$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$

$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$

$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$

The "182" can also be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry look-ahead generator are identical in both cases.

	2.2	CONDITIONS	TYF	UNIT	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNII
^t PHL [/] ^t PLH	propagation delay \overline{P}_{n} to \overline{P} C_{n} to any output \overline{P}_{n} or \overline{G}_{n} to any output	C _L = 15 pF V _{CC} = 5 V	11 17 14	14 21 17	ns ns
CI	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	50	50	pF

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

PD = CPD ×
$$VCC^2$$
 × f_i + Σ (CL × VCC^2 × f_o) where:

$$f_{0}$$
 = output frequency in MHz Σ (C_L x V_{CC}² x f_{0}) = sum of outputs

CL = output load capacitance in pF

2. For HC the condition is VI = GND to VCC For HCT the condition is VI = GND to VCC
$$-1.5$$
 V

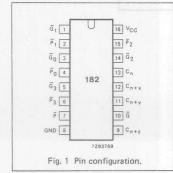
PACKAGE OUTLINES

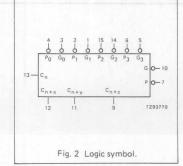
16-lead DIL; plastic (SOT38Z).

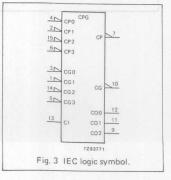
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 1, 14, 5	Go to G3	carry generate inputs (active LOW)
4, 2, 15, 6	Po to P3	carry propagate inputs (active LOW)
7	P	carry propagate output (active LOW)
8	GND	ground (0 V)
9	C _{n+z}	function output
10	G	carry generate output (active LOW)
11	C _{n+y}	function output
12	C _{n+x}	function output
13	Cn	carry input (active HIGH)
16	Vcc	positive supply voltage







13 Cn

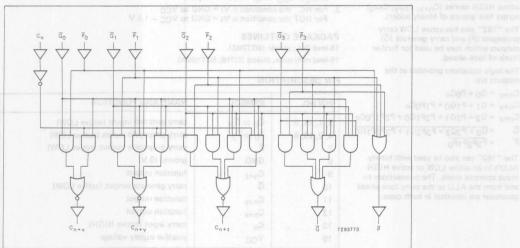
LOOK-AHEAD CARRY GENERATOR

FEATURES

- Provides curry (upit-sheed across
- Multi-level look-afread for high-spread arithmetic operation over long word
 - Output capability: standard
 - o less certagores MSI

DEMERAL DESCRIPTION

The ZARC/NGT182 are high-lighed Sogre CMOS devices and arcoin compatible with pw power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The ZARC/HGT182 carry look-shead generators accept up to hour pains of generators accept up to hour pains of generators accept up to four pains of generators accept up to four pains of some LOW carry propagate (Pg. E1, Pg. 2) and carry propagate (Pg. C1, C2, C3) signals and as active HiGH carry lings.



AS= DOA

C_{n+x} 12 C_{n+y} 11 C_{n+z} 9

(Wu mi _ 97293772 g m)

Fig. 4 Functional diagram.

Fig. 5 Logic diagram.

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FUNCTION TABLE

2015	met	PUTS	OUT	Cross Na	art no	William	Koncz	S	NPUTS	- 11			
P	G	C _{n+z}	C _{n+y}	C _{n+x}	\overline{P}_3	G ₃	P ₂	\overline{G}_2	P ₁	\overline{G}_1	\overline{P}_0	Ū0	Cn
				L L H							H X X L	H H L X	X L X H
		a	L L H H H	70) 28+ et	01-	\$14-01	3	TIV	H X X X L L	H H K X	X H X X X L	X H H X L	X L X H
	36	L OL LS		180 30 28		181	H X X	H H H	X H X	X H H	X X H	X X H	X X X L
	88 90 81	H H		216 48 37		20 18 18	X L L	L X X	X X L	X L X	X X L	X X L	X X X
	Н	H		36	Н	Н	X	X	X	X	8	X	П
	HHH			180 36 31	X X	H H H	H X X	H H	X H X	H	8	X X H	
				179* 34 29 -	X L L	L X X	X L L	X L X	X X L	X L X		X X X L	
H H H	15	73 27 23		170 34 29	X X X	105 14 88	X X H		X H X	Pig.	H X X		
H	7	35		95	H L	22	X L	3	X L	pi9	X		

H = HIGH voltage level L = LOW voltage level X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)				н 1	EST CON	NOITIC	IS
SYMBOL	PARAMETER				74H	С			UNIT	X	WAVEFO	DMC	1
STIMBUL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}			
		min.	typ.	max.	min.	max.	min.	max.		J.			
t _{PHL} /	propagation delay		30 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 6	X H H	LXX
^t PHL [/]	propagation delay C _n to any output		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6	×	XXX
tPHL/ tPLH	propagation delay \overline{P}_n to \overline{G}		47 17 14	145 29 25		180 36 31	H	220 44 38	ns	2.0 4.5 6.0	Fig. 6	×	H
t _{PHL} /	propagation delay P _n to C _{n+n}		47 17 14	145 29 25		180 36 31	X	220 44 38	ns	2.0 4.5 6.0	Fig. 6	X	
tPHL/ tPLH	propagation delay \overline{G}_{n} to C_{n+n}		44 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 6	XXX	
t _{PHL} /	propagation delay \overline{G}_{Π} to \overline{G}	H	41 15 12	135 27 23		170 34 29	×××××××××××××××××××××××××××××××××××××××	205 41 35	ns	2.0 4.5 6.0	Fig. 6		
tTHL/ tTLH	output transition time	1	19 7 6	75 15 13		95 19 16	1	110 22 19	ns	2.0 4.5 6.0	Fig. 6		

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT	
G ₀ , G ₁ , P ₀ , P ₁ , P ₂ G ₃ G ₂ , P ₃ , C _n		
G ₃	0.30	
G ₂ , P ₃ , C _n	1.25	

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

				ran	Tamb (°C)				TEST CONDITIONS		
01/11/01		1	r Pla	1000	74HC							
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/	propagation delay		17	28	501	35		42	ns	4.5	Fig. 6	
tPHL/ tPLH	propagation delay C _n to any output	11	26	43		54		65	ns	4.5	Fig. 6	
tPHL/ tPLH	propagation delay \overline{P}_n to \overline{G}	7.5s	20	33	nwy U.	41,00	1 T 10	50	ns	4.5	Fig. 6	
tPHL/	propagation delay \overline{P}_n to C_{n+n}		20	33		41		50	ns	4.5	Fig. 6	
t _{PHL} /	propagation delay \overline{G}_n to \overline{G}_{n+n} , \overline{G}_n to \overline{G}		18	32		40	1 [48	ns	4.5	Fig. 6	
t _{THL} /	output transition time	1	7	15		19		22	ns	4.5	Fig. 6	

AC WAVEFORMS

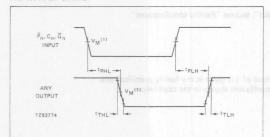


Fig. 6 Waveforms showing the input $(\overline{P}_n,\,C_n,\,\overline{G}_n)$ to any output propagation delays and the output transition times.

12m+1 hun contomationamic ser

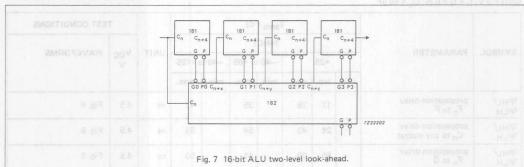
Note to HCT types

The value of additional quiescent supply current (AICC) for a un To determine AICC per input, multiply this value by the unit jou

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_1 = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_1 = GND$ to 3 V.

APPLICATION INFORMATION



ing. / TO-DIE ALO EWO-level TOOK-diffedu

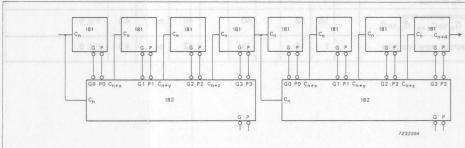
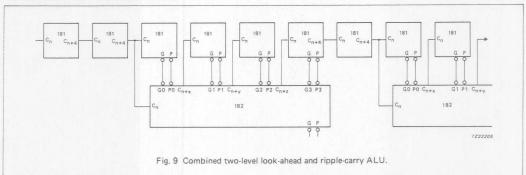
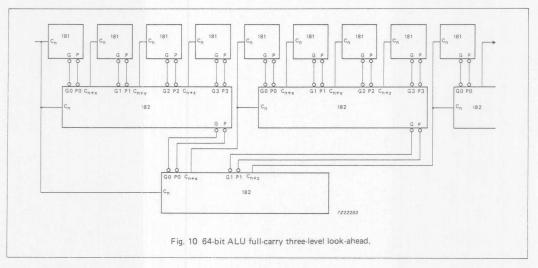


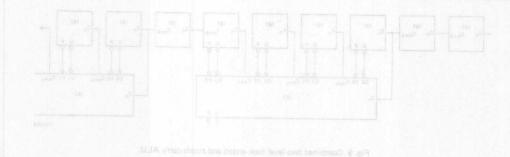
Fig. 8 32-bit ALU two-level look-ahead over 16-bit groups.

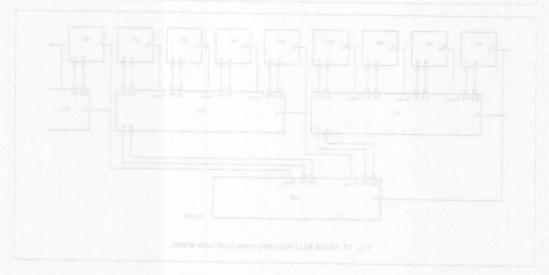
APPLICATION INFORMATION (Cont'd)





Note to Figs 7 to 10
A and B inputs and F outputs of "181" are not shown.





PRESETTABLE SYNCHRONOUS BCD DECADE UP/DOWN COUNTER

FEATURES THE PROPERTY OF THE P

operation.

- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion
- Single up/down control input
- Output capability: standard
- · ICC category: MSI

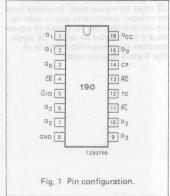
GENERAL DESCRIPTION

The 74HC/HCT190 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT190 are asynchronously presettable up/down BCD decade counters. They contain four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs (Do to Da) is loaded into the counter and appears on the outputs when the parallel load (PL) input is LOW. As indicated in the function table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the count enable (CE) input. When CE is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down (U/D) input signal determines the direction of counting as indicated in the function table. The CE input may go LOW when the clock is in either state, however, the LOW-to-HIGH CE transition must occur only when the clock is HIGH. Also, the $\overline{\rm U}/{\rm D}$ input should be changed only when either CE or CP is HIGH.

(continued on next page)



01/14001	242445752	CONDITIONS	TYF	UNIT	
SYMBOL	PARAMETER	CONDITIONS	НС	нс нст	
t _{PHL} /	propagation delay CP to Q _n	C _L = 15 pF - V _{CC} = 5 V	22	24	ns
fmax	maximum clock frequency	ACC = 2 A	28	30	MHz
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	36	38	pF

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD
$$\times$$
 VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

fi = input frequency in MHz

CL = output load capacitance in pF

fo = output frequency in MHz

VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is VI = GND to VCC For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 V$

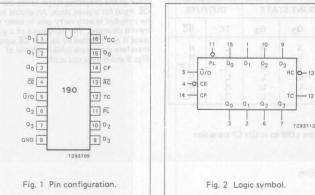
PACKAGE OUTLINES

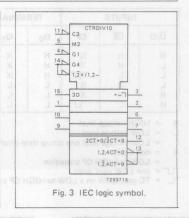
16-lead DIL; plastic (SOT38Z).

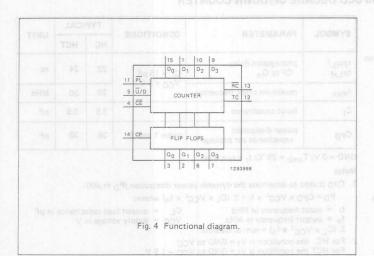
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q ₀ to Q ₃	flip-flop outputs
4	CE	count enable input (active LOW)
5	Ū/D	up/down input
8	GND	ground (0 V)
11	PL	parallel load input (active LOW)
12 90 30000	TC	terminal count output
13	RC	ripple clock output (active LOW)
14	СР	clock input (LOW-to-HIGH, edge triggered)
15, 1, 10, 9	D ₀ to D ₃	data inputs H (print pre-ob) Flori
16	Vcc	positive supply voltage







FUNCTION TABLE

005047111044005			INPUTS			OUTPUTS	
OPERATING MODE	PE PE	Ū/D	CE	СР	D _n	Qn	
parallel load	L L	X	×	X	L M	L H	
count up	tu Huo 1	nuLs ten	mil	1	Xor	count up	
count down	Н	Н	30,1	1	X	count down	
hold (do nothing)	Н	X	н	X	X	no change	

TC AND RC FUNCTION TABLE

	INPUTS		TER	MINAL	OUTPUTS			
Ū/D	CE	СР	00	01	02	03	тс	RC
Н	Н	X	Н	X	X	Н	L	Н
L	Н	X	H	X	X	H	H	Н
L	L		Н	X	X	Н	7	
L	Н	X	L	L	L	L	L	Н
H	Н	X	L	L	L	L	Н	H
H	L		LL	L	97-E 3T	L	7	L

H = HIGH voltage level

L = LOW voltage level

= LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

X = don't care

= LOW-to-HIGH CP transition

T = one LOW level pulse

L = TC goes LOW on a LOW-to-HIGH CP transition

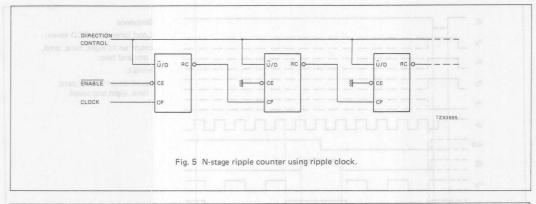
GENERAL DESCRIPTION

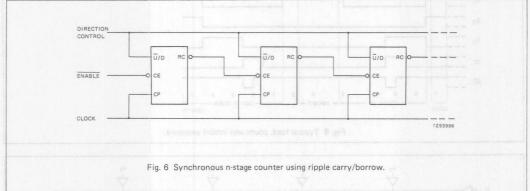
Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock (RC). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "9" in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until U/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the RC output. When TC is HIGH and CE is LOW, the RC output follows the clock pulse (CP). This feature simplifies the design of multistage counters as shown in Figs 5 and 6.

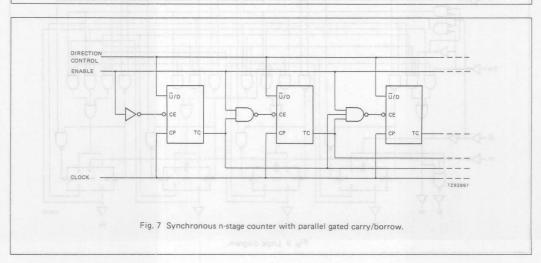
In Fig. 5, each \overline{RC} output is used as the clock input to the next higher stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH on \overline{CE} inhibits the \overline{RC} output pulse as indicated in the function table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This can be a disadvantage of this configuration in some applications.

Fig. 6 shows a method of causing state changes to occur simultraneously in all stages. The \overline{RC} outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. In this configuration the duration of the clock LOW state must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the \overline{RC} output of any package goes HIGH shortly after its CP input goes HIGH there is no such restriction on the HIGH-state duration of the clock.

In Fig. 7, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the CE input for a given stage. An enable must be included in each carry gate in order to inhibit counting. The TC output of a given stage it not affected by its own CE signal therefore the simple inhibit scheme of Figs 5 and 6 does not apply.



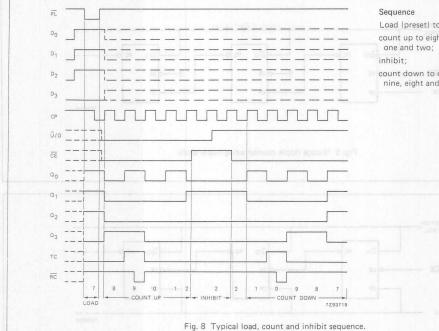


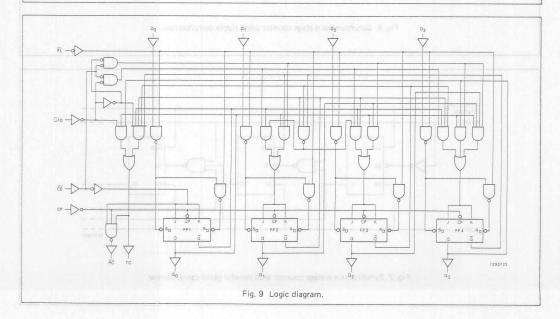




Load (preset) to BCD seven; count up to eight, nine, zero, one and two;

count down to one, zero, nine, eight and seven.





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications.

Output capability: standard

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF 2000 .nim 2000 .nim 2000 .nim 2000 .nim

	100						T _{amb} ((°C)		205			TEST CONDI	TIONS
	Fig. 17	6.0			88		74H	С	87	38			10 or 0\0	UB
SYMBOL	PARAMET	ER			+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFOR	VIS
				min.	typ.	max.	min.	max.	min.	max.			D _H to PL	Lie Lie
t _{PHL} /	propagation CP to Q _n	n delay	80		72 26 21	220 44 37	75 5	275 55 47	39 44 11	330 66 56	ns	2.0 4.5 6.0	Fig. 10 5	
tphl/	propagation CP to TC	n delay	en		83 30 24	255 51 43		320 64 54	-64 -16 -13	385 77 65	ns	2.0 4.5 6.0	Fig. 10 U	
tphl/	propagation CP to RC	n delay	20		44 16 13	150 30 26		190 38 33	3-4-	225 45 38	ns	2.0 4.5 6.0	Fig. 11	
^t PHL/	propagation CE to RC		ěn		33 12 10	130 26 22		165 33 28	-7 -2-	195 39 33	ns	2.0 4.5 6.0	Fig. 11.0	r F
t _{PHL} /	propagation D _n to Ω _n	delay	MH2		63 23 18	220 44 37	484	275 55 47	85 89 80	330 66 56	ns	2.0 4.5 6.0	Fig. 12	fmax.
t _{PHL} /	propagation PL to Ω _n	n delay			63 23 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 13	
t _{PHL} /	propagation U/D to To				44 16 13	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 14	
tphl/	propagation				50 18 14	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 14	
t _{THL} /	output tran	nsition time			19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 15	
tw	clock pulse HIGH or			155 31 26	28 10 8		195 39 33		235 47 40		ns	2.0 4.5 6.0	Fig. 10	
tW	parallel loa LOW	d pulse wid	th	100 20 17	25 9 7		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 15	
t _{rem}	removal tin	ne		35 7 6	8 3 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 15	

AC CHARACTERISTICS FOR 74HC (Continued)

				age ye			T _{amb} (°C)	no young			TEST CONDITIONS		
							74H	С						CC catagory
SYMBOL	PARAMETE	R			+25	May 1	-40	to +85	-40 t	o +125	UNIT	Vcc	WAVEFOR	
				min.	typ.	max.	min.	max.	min.	max.	300	i = jo:	mid = yt = yt	N D = CIVE
zwort t _{su}	set-up time Ū/D to CP			205 41 35	61 22 18		255 51 43	Ŧ	310 62 53		ns	2.0 4.5 6.0	Fig. 17	
t _{su}	set-up time D _n to PL	V 1	HAU	100 20 17	19 7 6	88+	125 25 21	l year	150 30 26	nam .	ns	2.0 4.5 6.0	Fig. 16	JOSMYS
t _{su}	set-up time CE to CP	2.0 4.6	20	140 28 24	39 14 11	98	175 35 30	00	210 42 36		ns	2.0 4.5 6.0	Fig. 17	UH93 HU93
^t h	hold time Ū/D to CP	2.0 8.5	att	0 0 0	-44 -16 -13	20	0 0 0	58	0 0		ns	2.0 4.5 6.0	Fig. 17	/1Hd1
t _h	hold time D _n to PL	2.0	žrt.	0 0 0	-14 -5 -4	88	0 0 0	08	0 0 0		ns	2.0 4.5 6.0	Fig. 16	/ JE(q)
th	hold time CE to CP	2,0 4.6 4.6	en	0 0 0	-19 -7 -6	3	0 0 0	30	0 0 0		ns	2.0 4.5 6.0	Fig. 17	H ld.
f _{max}	maximum cle frequency	ock pulse	100	3.0 15 18	8.3 25 30	38	2.4 12 14	00	2.0 10 12		MHz	2.0 4.5 6.0	Fig. 10	HTd) /THd1

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications.

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

NPUT	UNIT LOA						
O _n	0.5	=101					
DP J/D DE, PL	0.65 1.15	4.3					
JE, PL	1.5	3,1					
	Fig. 11						

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)				TEST CONDITIONS		
					74HC	т				.,	WANTED DATE	
SYMBOL	PARAMETER WORLD STATE	n edr	+25	g at l'ite	-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			AO I THEI	
t _{PHL} /	propagation delay CP to Ω _n		28	48		60		72	ns	4.5	Fig. 10	
t _{PHL} /	propagation delay CP to TC		34	58		73		87	ns	4.5	Fig. 10 90	
^t PHL/ ^t PLH	propagation delay CP to RC		20	35		44		53	ns	4.5	Fig. 11	
t _{PHL} /	propagation delay CE to RC		18	33		41		50	ns	4.5	Fig. 11	
t _{PHL} /	propagation delay D _n to Q _n		24	44		55		66	ns	4.5	Fig. 12	
t _{PHL} / t _{PLH}	propagation delay PL to Q _n		29	49		61		74	ns	4.5	Fig. 13	
t _{PHL} /	propagation delay U/D to TC		24	45		56		68	ns	4.5	Fig. 14	
tPHL/	propagation delay U/D to RC		26	45		56		68	ns	4.5	Fig. 14	
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 15	
t _W	clock pulse width HIGH or LOW	25	10		31		38		ns	4.5	Fig. 10	
t _W	parallel load pulse width LOW	22	12		28		33		ns	4.5	Fig. 15	
t _{rem}	removal time PL to CP	7	1		9		11		ns	4.5	Fig. 15	
t _{su}	set-up time Ū/D to CP	42	25		53		63		ns	4.5	Fig. 17	
^t su	set-up time D _n to PL	20	10		25		30		ns	4.5	Fig. 16	
t _{su}	set-up time CE to CP	31	18		39		47		ns	4.5	Fig. 17	
t _h	hold time Ū/D to CP	0	-18		0		0		ns	4.5	Fig. 17	
^t h	hold time D _n to PL	0	-6		0		0		ns	4.5	Fig. 16	
^t h	hold time CE to CP	0	-10		0		0		ns	4.5	Fig. 17	
fmax	maximum clock pulse frequency	16	27		13		11		MHz	4.5	Fig. 10	

AC WAVEFORMS

U/D INPUT

TC OUTPUT

RC OUTPUT

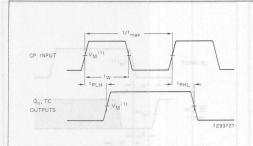


Fig. 10 Waveforms showing the clock (CP) to output $(\Omega_{\rm n})$ propagation delays, the clock pulse width and the maximum clock pulse frequency.

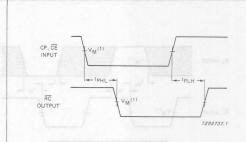


Fig. 11 Waveforms showing the clock and count enable inputs (CP, $\overline{\text{CE}}$) to ripple clock output ($\overline{\text{RC}}$) propagation delays .

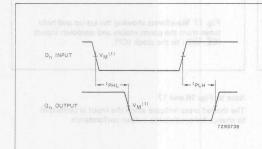


Fig. 12 Waveforms showing the input (D_n) to output (Q_n) propagation delays.

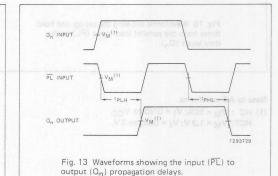
→ tPLH

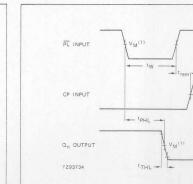
+ TPHL |

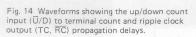
+ tpHI

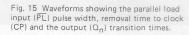
tPLH |

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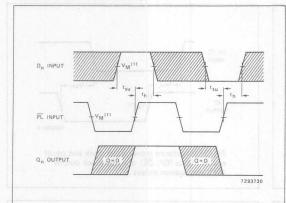


Fig. 16 Waveforms showing the set-up and hold times from the parallel load input (\overline{PL}) to the data input $(D_n).$

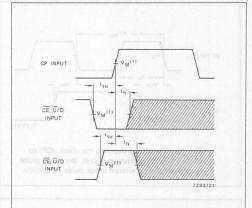


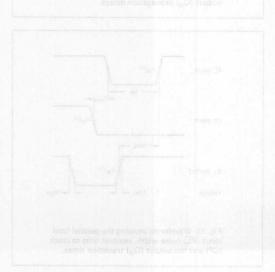
Fig. 17 Waveforms showing the set-up and hold times from the count enable and up/down inputs $(\overline{CE},\overline{U}/D)$ to the clock (CP).

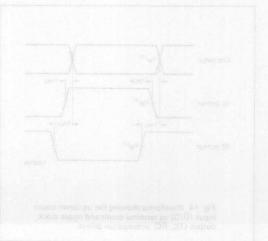
Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

Note to Figs 16 and 17

The shaded areas indicate when the input is permitted to change for predictable output performance.





PRESETTABLE SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER

FEATURES THEOREM LANGUED

- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion
- Single up/down control input
- Output capability: standard
- Icc category: MSI

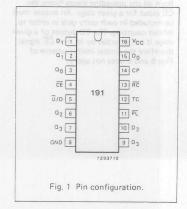
GENERAL DESCRIPTION

The 74HC/HCT191 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT191 are asynchronously presettable 4-bit binary up/down counters. They contain four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs (D₀ to D₃) is loaded into the counter and appears on the outputs when the parallel load (PL) input is LOW. As indicated in the function table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the count enable (CE) input. When CE is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down $(\overline{\mathsf{U}}/\mathsf{D})$ input signal determines the direction of counting as indicated in the function table. The CE input may go LOW when the clock is in either state, however, the LOW-to-HIGH CE transition must occur only when the clock is HIGH. Also, the $\overline{\rm U}/{\rm D}$ input should be changed only when either CE or CP is HIGH.

(continued on next page)



OVMBOL	DADAMETED	CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT	
tPHL/ tPLH	propagation delay CP to Qn	C _L = 15 pF - V _C C = 5 V	22	22	ns	
f _{max}	maximum clock frequency	- ACC - 2 A	36	36	MHz	
CI	input capacitance		3.5	3.5	pF	
C _{PD}	CP to Q _n	notes 1 and 2	31	33	рF	

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x
$$VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

f; = input frequency in MHz

 f_0 = output frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$ 2. For HC the condition is VI = GND to VCC For HCT the condition is $V_I = GND$ to VCC - 1.5 V

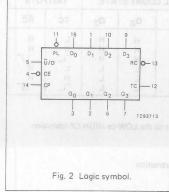
PACKAGE OUTLINES

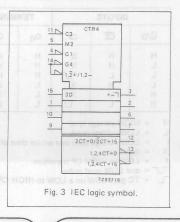
16-lead DIL; plastic (SOT38Z).

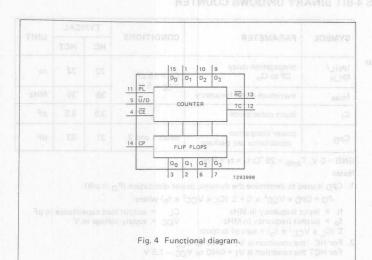
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q ₀ to Q ₃	flip-flop outputs
4	CE	count enable input (active LOW)
5	Ū/D	up/down input
8	GND	ground (0 V)
11	PL	parallel load input (active LOW)
12	TC	terminal count output
13	RC	ripple clock output (active LOW)
14	CP	clock input (LOW-to-HIGH, edge triggered)
15, 1, 10, 9	D ₀ to D ₃	data inputs
16	Vcc	positive supply voltage







FUNCTION TABLE

OPERATING MODE	231		INPUTS			OUTPUTS	
(WOJ syn	PL	Ū/D	CE	СР	Dn	Qn	
parallel load	L L	X	X	X	H	L H	
count up	LI	inal count	I L	1	X	count up	
count down (WOJ svil		Hola's	ggp	1	X	count down	
hold (do nothing)	Н	X	Н	X	X	no change	

TC AND RC FUNCTION TABLE

	INPUTS		TER	MINAL	OUTPUTS			
Ū/D	CE	СР	ο ₀	01	02	Ο3	тс	RC
Н	Н	X	Н	Н	Н	Н	L	Н
L	Н	X	Н	Н	Н	Н	Н	Н
L	L		Н	Н	Н	Н	L	T
L	Н	X	L	L	L	L	L	H
H	H	X	L	L	L	L	Н	Н
H	L	75	L	L	Later Later	L	- 7 5	

H = HIGH voltage level

L = LOW voltage level

= LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

X = don't care

= LOW-to-HIGH CP transition

T = one LOW level pulse

L = TC goes LOW on a LOW-to-HIGH CP transition

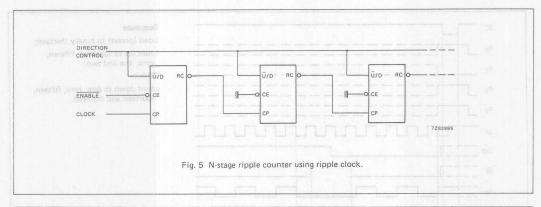
GENERAL DESCRIPTION

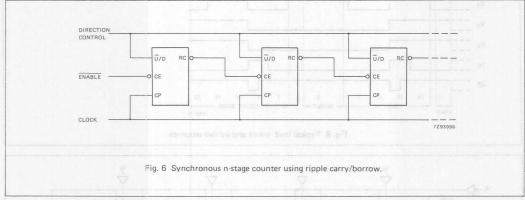
Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock (RC). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "15" in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until U/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the RC output. When TC is HIGH and CE is LOW, the RC output follows the clock pulse (CP). This feature simplifies the design of multistage counters as shown in Figs 5 and 6.

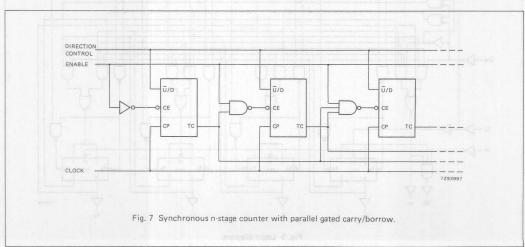
In Fig. 5, each RC output is used as the clock input to the next higher stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH on CE inhibits the RC output pulse as indicated in the function table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This can be a disadvantage of this configuration in some applications.

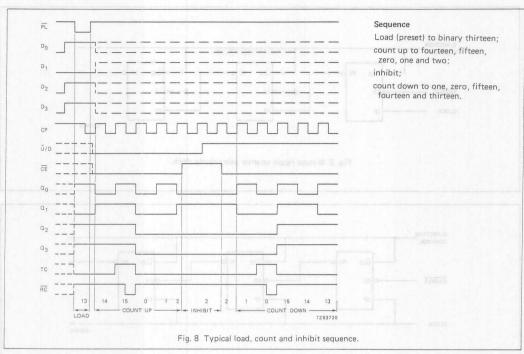
Fig. 6 shows a method of causing state changes to occur simultaneously in all stages. The \overline{RC} outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. In this configuration the duration of the clock LOW state must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the \overline{RC} output of any package goes HIGH shortly after its CP input goes HIGH there is no such restriction on the HIGH-state duration of the clock.

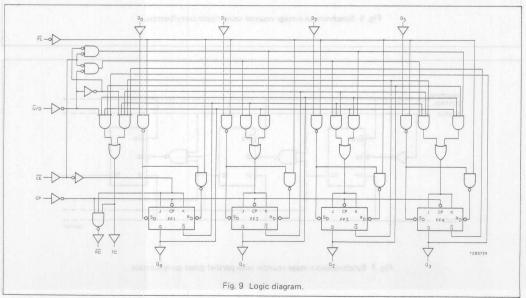
In Fig. 7, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{\text{CE}}$ input for a given stage. An enable must be included in each carry gate in order to inhibit counting. The TC output of a given stage it not affected by its own $\overline{\text{CE}}$ signal therefore the simple inhibit scheme of Figs 5 and 6 does not apply.











DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V; } t_r = t_f = 6 \text{ ns; } C_L = 50 \text{ pF}$

	2.0					T _{amb} (°C)					TEST CONDITIONS	
	4.5 Fig. 17	271	. 7		62	74H	С	B	19			90 of GVU	υŧ
SYMBOL	PARAMETER			+25	et l	-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS	
	4.5 Fig. 18 6.0	-ED	min.	typ.	max.	min.	max.	min.	max.			D _P -to PL	138
t _{PHL} /	propagation delay CP to Q _n	-80		72 26 21	220 44 37	Ð	275 55 47	16 16 13	330 66 56	ns	2.0 4.5 6.0	Fig. 10	138
t _{PHL} /	propagation delay CP to TC	EST		83 30 24	255 51 43		320 64 54	38	395 77 65	ns	2.0 4.5 6.0	Fig. 10	
t _{PHL} /	propagation delay	271		47 17 14	150 30 26		190 38 33	101	225 45 38	ns	2.0 4.5 6.0	Fig. 11	
t _{PHL} /	propagation delay CE to RC	en:		33 12 10	130 26 22		165 33 28	28 10 8	195 39 33	ns	2.0 4.5 6.0	Fig. 11	
t _{PHL} /	propagation delay	HIM.		61 22 18	220 44 37		275 55 47	8	330 66 56	ns	2.0 4.5 6.0	Fig. 12	517
t _{PHL} /	propagation delay			61 22 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 13	
t _{PHL} /	propagation delay Ū/D to TC			44 16 13	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 14	
t _{PHL} /	propagation delay U/D to RC			50 18 14	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 14	
t _{THL} /	output transition time			19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 15	10 10
tw	clock pulse width HIGH or LOW		125 25 21	28 10 8		155 31 26		195 39 33		ns	2.0 4.5 6.0	Fig. 10	
tw	parallel load pulse width LOW		100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 15	
^t rem	removal time PL to CP		35 7 6	8 3 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 15	

AC CHARACTERISTICS FOR 74HC (Continued)

							T _{amb} ((°C)					TEST CONDITIONS			
			74HC									C campory: MSI				
SYMBOL	PARAMETER			+25			-40 to +85 -40 to) to +1:	25	UNIT	VCC	WAVEFORMS		
				min.	typ.	max.	min.	max.	min	. ma	ax.	34	(II) = (JD	(3n 8 = 12 = 11)	V 0 = QW	
t _{su}	set-up time Ū/D to CP			205 41 35	50 18 14		255 51 43	na ^T	310 62 53			ns	2.0 4.5 6.0	Fig. 17		
t _{su}	set-up time D _n to PL	¥		100 20 17	19 7 6	- 28 m .at	125 25 21	4 .8	150 30 26	140 140 - 140	simi.	ns	2.0 4.5 6.0	Fig. 16		
t _{su}	set-up time CE to CP	2.0	20	140 28 24	44 16 13	ō	175 35 30	0	210 42 36	18		ns	2.0 4.5 6.0	Fig. 17	PLH PLH	
^t h	hold time U/D to CP	2.0	20	0 0	-39 -14 -11	0	0 0 0	9	0 0 0	20		ns	2.0 4.5 6.0	Fig. 17	VJH9 HJ8	
th	hold time D _n to PL	2.0 4.5 6.0	100	0 8	-11 -4 -3	0	0 0 0	0	0 0 0	147		ns	2.0 4.5 6.0	Fig. 16	Varia Har	
^t h	hold time CE to CP	2.0 4.5 6.0	201	0 0	-28 -10 -8	a	0 0 0	0	0 0 0	0000		ns	2.0 4.5 6.0	Fig. 17	VIH9	
f _{max}	maximum clo	ock pulse	an	4.0 20 24	11 33 39	9	3.2 16 19		2.6 13 15	18 22 81		MHz	2.0 4.5 6.0	Fig. 10	NJHP NJHP	
															H1s	

DC	CH	IARA	CTER	ISTICS	FOR	74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD	ı.T					
D _p	0.5	3 5					
D _n CP U/D CE, PL	0.65 1.15	8.6					
CE, PL	1.5	4.3					

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)		TEST CONDITIONS				
SYMBOL	BARAMETER	74HCT								\/	WAVEFORMS	
	PARAMETER SOME SOME SOME SOME SOME SOME SOME SOME	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORING	
		min.	typ.	max.	min.	max.	min.	max.			OACUTINU	
tPHL/	propagation delay CP to Ω _n		26	48		60		72	ns	4.5	Fig. 10	
t _{PHL} /	propagation delay CP to TC		32	51		64		77	ns	4.5	Fig. 10 68.0	
t _{PHL} /	propagation delay CP to RC		19	35		44		53	ns	4.5	Fig. 11	
t _{PHL} /	propagation delay CE to RC		19	33		41		50	ns	4.5	Fig. 11	
t _{PHL} /	propagation delay D _n to Q _n		22	44		55		66	ns	4.5	Fig. 12	
tPHL/ tPLH	propagation delay PL to Q _n		27	46		58		69	ns	4.5	Fig. 13	
tPHL/	propagation delay U/D to TC		23	45		56		68	ns	4.5	Fig. 14	
t _{PHL} /	propagation delay Ū/D to RC		24	45		56		68	ns	4.5	Fig. 14	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 15	
t _W	clock pulse width HIGH or LOW	16	9		20		24		ns	4.5	Fig. 10	
t _W	parallel load pulse width LOW	22	11		28		33		ns	4.5	Fig. 15	
t _{rem}	removal time PL to CP	7	1		9		11		ns	4.5	Fig. 15	
t _{su}	set-up time Ū/D to CP	41	20	4.7	51		62		ns	4.5	Fig. 17	
t _{su}	set-up time D _n to PL	20	9		25		30		ns	4.5	Fig. 16	
t _{su}	set-up time CE to CP	30	18		38		45		ns	4.5	Fig. 17	
th	hold time Ū/D to CP	0	-18		0		0		ns	4.5	Fig. 17	
th	hold time D _n to PL	0	-5		0		0		ns	4.5	Fig. 16	
^t h	hold time CE to CP	0	-10		0		0		ns	4.5	Fig. 17	
fmax	maximum clock pulse frequency	20	33		16		13		MHz	4.5	Fig. 10	

AC WAVEFORMS

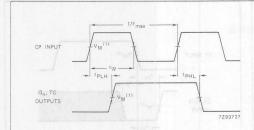


Fig. 10 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

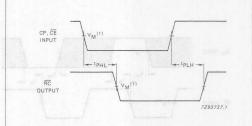


Fig. 11 Waveforms showing the clock and count enable inputs (CP, $\overline{\text{CE}}$) to ripple clock output ($\overline{\text{RC}}$) propagation delays.

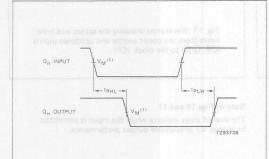


Fig. 12 Waveforms showing the input (D_n) to output (Q_n) propagation delays.

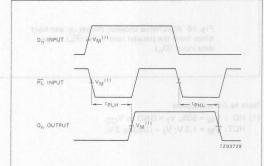


Fig. 13 Waveforms showing the input (\overline{PL}) to output (Q_n) propagation delays.

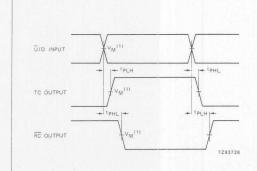


Fig. 14 Waveforms showing the up/down count input (\overline{U}/D) to terminal count and ripple clock output (TC, $\overline{RC})$ propagation delays.

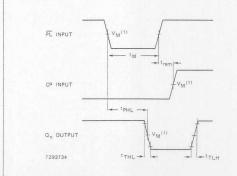


Fig. 15 Waveforms showing the parallel load input (\overline{PL}) pulse width, removal time to clock (CP) and the output (Q_{η}) transition times.

AC WAVEFORMS (Continued)

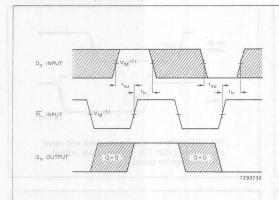


Fig. 16 Waveforms showing the set-up and hold times from the parallel load input (\overline{PL}) to the data input (D_n) .

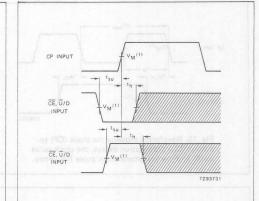
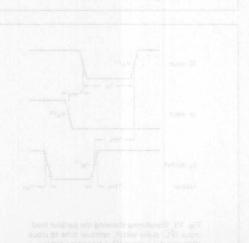


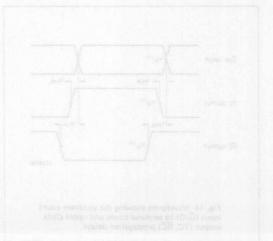
Fig. 17 Waveforms showing the set-up and hold times from the count enable and up/down inputs $(\overline{CE}, \overline{U}/D)$ to the clock (CP).

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3$ V; $V_I = GND$ to 3 V. Note to Figs 16 and 17
The shaded areas indica

The shaded areas indicate when the input is permitted to change for predictable output performance.





PRESETTABLE SYNCHRONOUS BCD DECADE UP/DOWN COUNTER

FEATURES

- · Synchronous reversible counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Output capability: standard
- · Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT192 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT192 are synchronous BCD up/down counters. Separate up/down clocks, CP11 and CPD respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CP11 clock is pulsed while CPD is held HIGH, the device will count up. If the CPD clock is pulsed while CPU is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input (PL).

The "192" contains four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the \mbox{CP}_D input will decrease the count by one, while a similar transition on the \mbox{CP}_U input will advance the count by one.

(continued on next page)

CYMAROL	DADAMETED	(baunimos) ino	TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	нс	нст	dany go	
^t PHL [/]	propagation delay CP _D , CP _U to Q _n	CL = 15 pF	20	20	ns	
f _{max}	maximum clock frequency	V _{CC} = 5 V	40	45	MHz	
CI	input capacitance	a activating clock s counts.	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	24	28	pF	

GND = 0 V;
$$T_{amb}$$
 = 25 °C; t_r = t_f = 6 ns

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

 $PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$ where:

f; = input frequency in MHz f_O = output frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

 Σ (C_L × V_{CC}² × f_O) = sum of outputs

2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} -1.5 V

PACKAGE OUTLINES

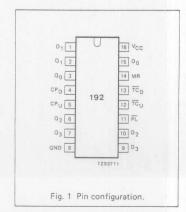
16-lead DIL; plastic (SOT38Z).

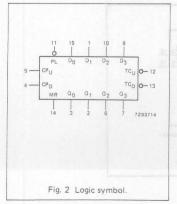
16-lead mini-pack; plastic (SO16; SOT109A).

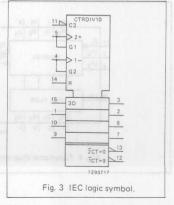
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q ₀ to Q ₃	flip-flop outputs
4	CPD	count down clock input*
5	CPU	count up clock input*
8	GND	ground (0 V)
11 ×	PL	asynchronous parallel load input (active LOW)
12	TCU	terminal count up (carry) output (active LOW)
13 X	TCD	terminal count down (borrow) output (active LOW)
14	MR	asynchronous master reset input (active HIGH)
15, 1, 10, 9	D ₀ to D ₃	data inputs
16 (9) (1000)	V _{CC}	positive supply voltage

* LOW-to-HIGH, edge triggered







GENERAL DESCRIPTION (Continued)

One clock should be held HIGH while counting with the other, otherwise the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal count up (\overline{TC}_U) and terminal count down (\overline{TC}_D) outputs are normally HIGH. When the circuit has reached the maximum count state of 9, the next HIGH-to-LOW transition of CP_U will cause \overline{TC}_U to go LOW.

TCU will stay LOW until CPU goes HIGH again, duplicating the count up clock.

Likewise, the $\overline{\text{TC}}_D$ output will go LOW when the circuit is in the zero state and the CPD goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a

multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D₀ to D₃) is loaded into the counter and appears on the outputs (Q₀ to Q₃) regardless of the conditions of the clock inputs when the parallel load (PL) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q₀ to Q₃) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

FUNCTION TABLE

005047111041005	INPUTS INPUTS INPUTS IN INPUTS IN INFO									OUTPUTS TO SECOND TO						
OPERATING MODE	MR	PL	CPU	CPD	D ₀	D ₁	D ₂	D ₃	00	01	02	03	TCU	TCD		
reset (clear)	H	X	X	L H	X	×	X	X	L	ol letter	ed Sno	L	H H	L H		
parallel load	L		X X L H	L H X	L H H	L X X	L X X	L a H 8 H	LXI. Digital		L = D _n = D _n	subilitar la Lourn nontrol u triuce	H H H H H H H H H H H H H H H H H H H	Hollo Hollo Hollo Hyelo		
count up (seri) output (seri qu fruo)	tufnoo j	Н	1	Н	X	X	X	X	mb	cour	nt up		H*	Н		
count down	L	н	Н	1	X	X	X	X	HEN	count	down	in that	Н	H**		

H = HIGH voltage level

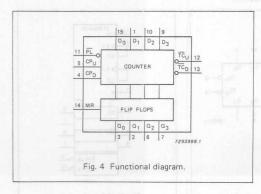
L = LOW voltage level

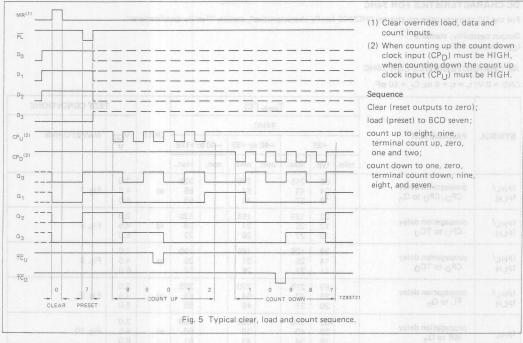
X = don't care

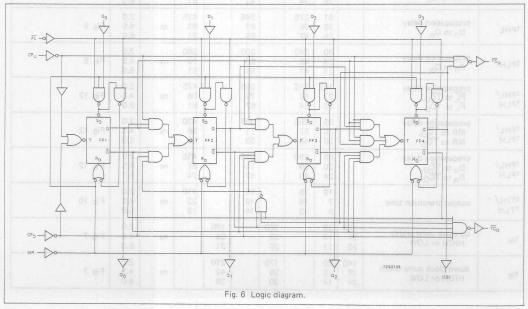
↑ = LOW-to-HIGH clock transition

* TCU = CPU at terminal count up (HLLH)

** TCD = CPD at terminal count down (LLLL)







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

		-			Tamb	(°C)					TEST CONDITIONS
CVMDOL	food (present) to BCD seven;				74H	0			LINUT		WAYEEODMC
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	VCC	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
^t PHL/	propagation delay CP _U , CP _D to Ω _n		66 24 19	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 7
^t PHL/	propagation delay CP _U to TC _U		33 12 10	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
^t PHL/	propagation delay CPD to TCD		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
^t PHL/	propagation delay PL to Q _n	cicus	69 25 20	215 43 37	nuco -	270 54 46	1	325 65 55	ns	2.0 4.5 6.0	Fig. 9
^t PHL	propagation delay MR to Ω _n	зола	63 23 18	200 40 34	baat ,	250 50 43	Type	300 60 51	ns	2.0 4.5 6.0	Fig. 10
^t PHL	propagation delay D _n to Q _n		91 33 26	275 55 47		345 69 59	Ÿ	415 83 71	ns	2.0 4.5 6.0	Fig. 9
t _{PLH}	propagation delay D _n to Q _n		80 29 23	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 9
t _{PHL} /	propagation delay PL to TCU, PL to TCD		102 37 30	315 63 54		395 79 67	JE	475 95 81	ns	2.0 4.5 6.0	Fig. 12
tPHL/	propagation delay MR to TC _D , MR to TC _D		96 35 28	285 57 48		355 71 60	F 644	430 86 73	ns	2.0 4.5 6.0	Fig. 12
t _{PHL} /	propagation delay $D_n \text{ to } \overline{TC}_U$, $D_n \text{ to } \overline{TC}_D$		83 30 24	290 58 49	10	365 73 62	P	435 87 74	ns	2.0 4.5 6.0	Fig. 12
THL/	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 10
tw	up clock pulse width HIGH or LOW	120 24 20	39 14 11		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 7
tw	down clock pulse width HIGH or LOW	140 28 24	50 18 14		175 35 30		210 42 36		ns	2.0 4.5 6.0	Fig. 7

AC CHARACTERISTICS FOR 74HC (Continued)

					T _{amb} (°C)			70		TEST CONDIT	TIONS
	TEST CONDIT				74H0	Da ^T			UNIT		WAVEFOR	AC
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNII	V _{CC}	WAVEFORM	JOSMY
	V	min.	typ.	max.	min.	max.	min.	max.				
tw	master reset pulse width	80 16 14	22 8 6	m23	100 20 17	is Xs	120 24 20	nies.	ns	2.0 4.5 6.0	Fig. 10	/THIS
tw	parallel load pulse width	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9	PLH PLH PLH
^t rem	removal time PL to CP _U , CP _D	50 10 9	3 1 1 1		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 9	H18
^t rem	removal time MR to CP _U , CP _D	50 10 9	0 0		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10	144
t _{su}	set-up time D _n to PL	80 16 14	22 8 6		100 20 17		120 24 20	E	ns	2.0 4.5 6.0	Fig. 11 note: CPU = CPD =	
th	hold time D _n to PL	0 0	-14 -5 -4		0 0		0 0	8	ns do	2.0 4.5 6.0	Fig. 11	/ 1148 1473g
^t h	hold time CP _U to CP _D , CP _D to CP _U	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 13	HUS HUS
^f max	maximum up, down clock pulse frequency	4.0 20 24	12 36 43		3.2 16 19		2.6 13 15		MHz	2.0 4.5 6.0	Fig. 7	HJ1 JJEII

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications.

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D _n	0.35
CP _U , CP _D	1.40
PL	0.65
MR	1.05

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V; } t_r = t_f = 6 \text{ ns; } C_L = 50 \text{ pF}$

					Tamb	°C)	1817			TEST CONDITIONS		
	UNIT VCC WAVEFORI				74HC	Т			LINUT		WAYEEODME	
SYMBOL	PARAMETER	,R80	+25	ery Jes	-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS	
	2.0	min.	typ.	max.	min.	max.	min.	max.	rish	w astuc	Jeson notesim	
tPHL/ tPLH	propagation delay CP _U , CP _D to Q _n		23	43		54		65	ns	4.5	Fig. 7	
t _{PHL} /	propagation delay CPU to TCU		16	30		38		45	ns	4.5	Fig. 8	
tPHL/	propagation delay CP _D to TC _D		17	30		38		45	ns	4.5	Fig. 8	
t _{PHL} /	propagation delay PL to Q _n		28	46		58		69	ns	4.5	Fig. 9	
^t PHL	propagation delay MR to Q _n		24	40		50		60	ns	4.5	Fig. 10	
tPHL/	propagation delay D _n to Q _n		36	62	1.0	78		93	ns	4.5	Fig. 9	
tPHL/	propagation delay PL to TCD, PL to TCD		36	64		80	6.0	96	ns	4.5	Fig. 12	
t _{PHL} /	propagation delay MR to \overline{TC}_{D} , MR to \overline{TC}_{D}		36	64		80		96	ns	4.5	Fig. 12	
^t PHL/ ^t PLH	propagation delay D_n to \overline{TC}_U , D_n to \overline{TC}_D		33	58		73		87	ns	4.5	Fig. 12	
t _{THL} / t _{TLH}	output transition time		7	15	9	19	HILLIA	22	ns	4.5	Fig. 10	
tw	up, down clock pulse width HIGH or LOW	25	14		31		38		ns	4.5	Fig. 7	
tw	master reset pulse width HIGH	16	6		20		24		ns	4.5	Fig. 10 TTTARANA	
t _W	parallel load pulse width LOW	20	10		25	in Isaaalla te	30	mi cun	ns	4.5	Fig. 9	
^t rem	removal time PL to CPU, CPD	10	1		13		15		ns	4.5	Fig. 9	
t _{rem}	removal time MR to CP _U , CP _D	10	2	ng el t i sie armi	13	rinu s 1	15	a) Insti d sultiv	ns	4.5	Fig. 10	
t _{su}	set-up time D _n to PL	16	8		20		24		ns	4.5	Fig. 11 note: CP _U = CP _D = HIGH	
^t h	hold time D _n to PL	0	-6		0		0		ns	4.5	Fig. 11 az. 0	
^t h	hold time CP _U to CP _D , CP _D to CP _U	20	9		25		30		ns	4.5	Fig. 13	
max	maximum up, down clock pulse frequency	20	41		16		13		MHz	4.5	Fig. 7	

AC WAVEFORMS

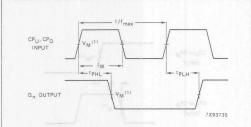


Fig. 7 Waveforms showing the clock (CPU, CPD) to output (Qn) propagation delays, the clock pulse width and the maximum clock pulse frequency.

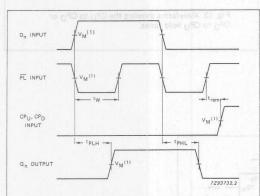
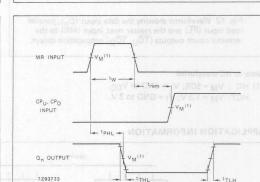


Fig. 9 Waveforms showing the parallel load input (PL) and data (D_n) to Q_n output propagation delays and PL removal time to clock input (CPU, CPD).



CPU, CPD

INPUT

 $\overline{\mathsf{TC}}_\mathsf{U}, \overline{\mathsf{TC}}_\mathsf{D}$

OUTPUT

Fig. 10 Waveforms showing the master reset input (MR) pulse width, MR to $Q_{\rm n}$ propagation delays, MR to ${\sf CP_U}$, ${\sf CP_D}$ removal time and output transition times.

- THL

Fig. 8 Waveforms showing the clock (CPU, CPD) to terminal count output $(\overline{TC}_U, \overline{TC}_D)$ propagation delays.

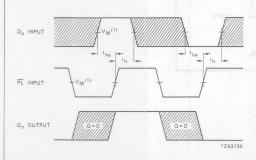


Fig. 11 Waveforms showing the data input (Dn) to parallel load input (PL) set-up and hold times.

Note to Fig. 11

The shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS (Continued)

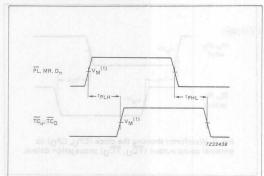


Fig. 12 Waveforms showing the data input (D_n), parallel load input (PL) and the master reset input (MR) to the terminal count outputs (\overline{TC}_D , \overline{TC}_D) propagation delays.

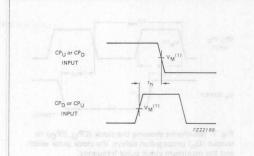
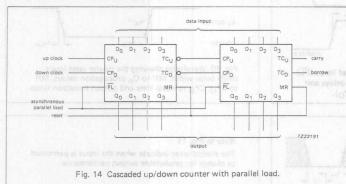


Fig. 13 Waveforms showing the CP_{U} to CP_{D} or CP_{D} to CP_{U} hold times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

APPLICATION INFORMATION



March 1988

PRESETTABLE SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER

FEATURES

- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Output capability: standard
- I_{CC} category: MSI

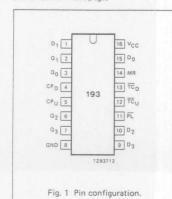
GENERAL DESCRIPTION

The 74HC/HCT193 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT193 are 4-bit synchronous binary up/down counters. Separate up/down clocks, CPU and CPD respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CPU clock is pulsed while CPD is held HIGH, the device will count up. If the CPD clock is pulsed while CPU is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input (PL).

The "193" contains four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CPU input will advance the count by one.

(continued on next page)



0.44001		ИСПОЛЕНИИ	TYF	PICAL	явия
SYMBOL	PARAMETER sustantium	CONDITIONS	нс	нст	UNIT
t _{PHL} / t _{PLH}	propagation delay CPD, CPU to Qn	C _L = 15 pF	20	20	ns
fmax	maximum clock frequency	V _{CC} = 5 V	45	47	MHz
CI CI	input capacitance	is denieshing crock	3.5	3.5	pF
C _{PD} to a	power dissipation capacitance per package	notes 1 and 2	24	26	pF

GND = 0 V; $T_{amb} = 25 \,^{\circ}\text{C}$; $t_r = t_f = 6 \, \text{ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD
$$\times$$
 VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

fo = output frequency in MHz

fi = input frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is VI = GND to VCC For HCT the condition is VI = GND to VCC - 1.5 V

PACKAGE OUTLINES

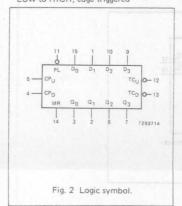
16-lead DIL; plastic (SOT38Z).

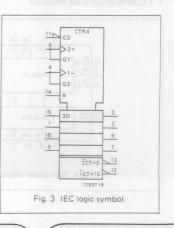
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q ₀ to Q ₃	flip-flop outputs
4	CPD	count down clock input*
5	CPU	count up clock input*
8	GND	ground (0 V)
11	PL	asynchronous parallel load input (active LOW)
12	TCII	terminal count up (carry) output (active LOW)
13	TCD	terminal count down (borrow) output (active
		LOW)
14	MR	asynchronous master reset input (active HIGH)
15, 1, 10, 9	D ₀ to D ₃	data inputs
16	Vcc	positive supply voltage

* LOW-to-HIGH, edge triggered





GENERAL DESCRIPTION

One clock should be held HIGH while counting with the other, otherwise the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal count up (\overline{TC}_U) and terminal count down (\overline{TC}_D) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of CP_U will cause \overline{TC}_U to go LOW.

TCU will stay LOW until CPU goes HIGH again, duplicating the count up clock.

Likewise, the TC_D output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a

multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (Dn to D3) is loaded into the counter and appears on the outputs (Q0 to Q3) regardless of the conditions of the clock inputs when the parallel load (PL) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Qn to Q3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

FUNCTION TABLE

ODED ATIMO MODE				INPL	JTS				36		OU	TPUT:	S blad eq	
OPERATING MODE	MR	PL	CPU	CPD	D ₀	D ₁	D ₂	D ₃	00	01	02	03	TCU	TCD
reset (clear)	H	×	×	L H	X	X	X	×	L	L _{id}	s Lasc	AL bo	H ad	L
parallel load	L C	alland brillion stagger	X X L H	L H X	L 10 H H	L H H	L H H	L B H H	TIL	LLHH	LLHH	LLHH	H H L H	LHHH
count up	anuos ti	Н	1	Н	X	X	Х	X	700	cour	t up	El weste	Н*	Н
count down	L	Н	Н	1	X	X	X	X	Hai	count	down	reriz ric	Н	H**

H = HIGH voltage level

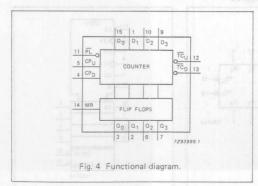
L = LOW voltage level

X = don't care

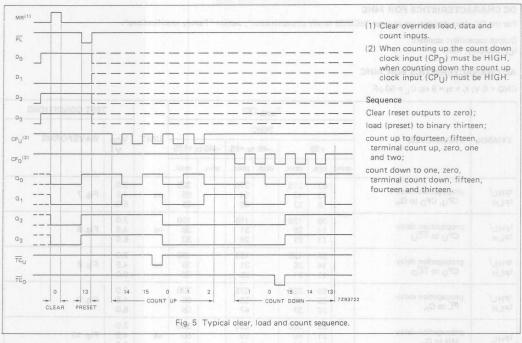
↑ = LOW-to-HIGH clock transition

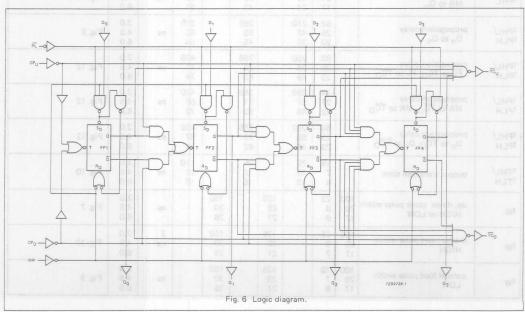
* TCU = CPU at terminal count up (HHHH)

** TCD = CPD at terminal count down (LLLL)









DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

	Char (reset outputs to zero				T _{amb} (°C)					TEST CONDITION	IS
inec	minir yramid of (feesing) book			-	74H		-					
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	to +125	UNIT	V _{CC}	WAVEFORMS	
	and two;	min.	typ.	max.	min.	max.	min.	max.				
^t PHL/	propagation delay CP _U , CP _D to Q _n		63 23 18	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 7	10
^t PHL/ ^t PLH	propagation delay CP _U to TC _U		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8	20
^t PHL [/]	propagation delay CP _D to TC _D		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8	107
^t PHL/ ^t PLH	propagation delay	COST (69 25 20	220 44 37	0 1000	275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 9	
^t PHL	propagation delay MR to Ω _n	.906.	58 21 17	200 40 34	u bsol	250 50 43	Typiq	300 60 51	ns	2.0 4.5 6.0	Fig. 10	
^t PHL/ ^t PLH	propagation delay D _n to Q _n		69 25 20	210 42 36		265 53 45	Å	315 63 54	ns	2.0 4.5 6.0	Fig. 9	
t _{PHL} /	propagation delay PL to TC _U , PL to TC _D		80 29 23	290 58 49		365 73 62		435 87 74	ns	2.0 4.5 6.0	Fig. 12	jei i
^t PHL/	propagation delay MR to TC _U , MR to TC _D		74 27 22	285 57 48		355 71 60		430 86 73	ns	2.0 4.5 6.0	Fig. 12	
^t PHL [/]	propagation delay D_n to \overline{TC}_U , D_n to \overline{TC}_D		80 29 23	290 58 49	J.C	365 73 62		435 87 74	ns	2.0 4.5 6.0	Fig. 12	
t _{THL} /	output transition time		19 7 6	75 15 13	10	95 19 16	T.	110 22 19	ns	2.0 4.5 6.0	Fig. 10	
t _W	up, down clock pulse width HIGH or LOW	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7	
tw	master reset pulse width HIGH	100 20 17	25 9 7		125 25 21		150 30 26		2 ns	2.0 4.5 6.0	Fig. 10	860
tw	parallel load pulse width LOW	100 20 17	19 7 6		125 25 21	7	150 30 26		ns	2.0 4.5 6.0	Fig. 9	

					T _{amb} (°C)			11 110	DO = In	TEST CONDITIONS
	TEST CONDIT				74H0	Tar			LIBILT	,,	WAVEFORMS
SYMBOL	PARAMETER		+25		-40	to +85	-40 to	o +125	UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
^t rem	removal time PL to CP _U , CP _D	50 10 9	8 3 2	att and	65 13 11	in Jes	75 15 13	e inim	ns	2.0 4.5 6.0	Fig. 9
^t rem	removal time MR to CP _U , CP _D	50 10 9	0 0 0		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t _{su}	set-up time D _n to PL	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 11 note: CPU = CPD = HIGH
^t h	hold time D _n to PL	0 0	-14 -5 -4		0 0 0		0 0 0	\$	ns	2.0 4.5 6.0	Fig. 11
^t h	hold time CP _U to CP _D , CP _D to CP _U	80 16 8	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 13
f _{max}	maximum up, down clock pulse frequency	4.0 20 24	13.5 41 49		3.2 16 19		2.6 13 15	8	MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications.

Output capability: standard

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

0.35 1.40 0.65 1.05

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

					Tamb	(°C)					TEST CONDITIONS
	UNIT VOE WAVEFORM	125			74HC	т				A	PARAMETE
SYMBOL	PARAMETER	.XEI	+25	ime	-40	to +85	-40 t	to +125	UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			erns levoreso
t _{PHL} /	propagation delay CP _U , CP _D to Q _n		23	43		54		65	ns	4.5	Fig. 7
^t PHL/	propagation delay CPU to TCU		15	27		34		41 0	ns	4.5	Fig. 8
tPHL/ tPLH	propagation delay CPD to TCD		15	27	0	34	173	41	ns	4.5	Fig. 8
t _{PHL} /	propagation delay PL to Ω _n		26	46		58	14	69	ns	4.5	Fig. 9
^t PHL	propagation delay MR to Q _n		22	40		50	10.00	60	ns	4.5	Fig. 10
t _{PHL} /	propagation delay D _n to Ω _n		27	46	0	58		69	ns	4.5	Fig. 9
tPHL/	propagation delay PL to TCD		31	55	- 8	69	las	83	ns	4.5	Fig. 12
t _{PHL} /	propagation delay MR to \overline{TC}_{D} , MR to \overline{TC}_{D}		29	55		69		83	ns	4.5	Fig. 12
tPHL/ tPLH	propagation delay D_n to \overline{TC}_U , D_n to \overline{TC}_D		32	58		73		87	ns	4.5	Fig. 12
t _{THL} /	output transition time	segs y	7	15	tics", I	19	Hy cha	22	ns	4.5	Fig. 10
tW	up, down clock pulse width HIGH or LOW	25	11		31		38		ns	4.5	Fig. 7 1314 - 1300-1314
tw	master reset pulse width HIGH	20	7, 10	rig al 1	25	tinu e 1	30	A) Insk	ns	4.5	Fig. 10
tw	parallel load pulse width LOW	20	8		25		30		ns	4.5	Fig. 9
^t rem	removal time PL to CP _U , CP _D	10	2		13		15		ns	4.5	Fig. 9
^t rem	removal time MR to CP _U , CP _D	10	0		13		15		ns	4.5	Fig. 10 40 0
t _{su}	set-up time D _n to PL	16	8		20		24		ns	4.5	Fig. 11 note: CP _U = CP _D = HIGH
^t h	hold time D _n to PL	0	-6		0		0		ns	4.5	Fig. 11
^t h	hold time ${\sf CP}_{\sf U}$ to ${\sf CP}_{\sf D}$, ${\sf CP}_{\sf D}$ to ${\sf CP}_{\sf U}$	16	7		20		24		ns	4.5	Fig. 13
max	maximum up, down clock pulse frequency	20	43		16		13		MHz	4.5	Fig. 7

AC WAVEFORMS

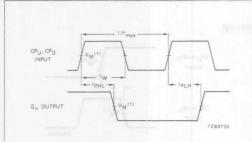


Fig. 7 Waveforms showing the clock (CP $_{\rm U}$, CP $_{\rm D}$) to output (Q $_{\rm n}$) propagation delays, the clock pulse width and the maximum clock pulse frequency.

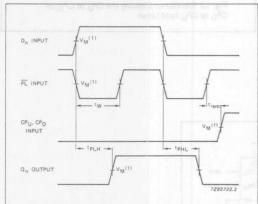


Fig. 9 Waveforms showing the parallel load input (PL) and data (D_n) to Q_n output propagation delays and \overline{PL} removal time to clock input (CP_U , CP_D).

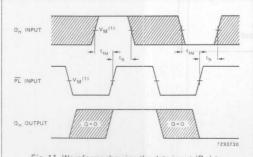


Fig. 11 Waveforms showing the data input (D $_{n})$ to parallel load input ($\overline{PL})$ set-up and hold times.

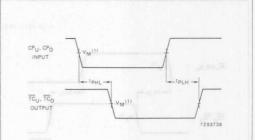


Fig. 8 Waveforms showing the clock (CPU, CPD) to terminal count output (\overline{TC}_U , \overline{TC}_D) propagation delays.

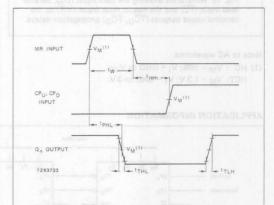


Fig. 10 Waveforms showing the master reset input (MR) pulse width, MR to \mathbf{Q}_{n} propagation delays, MR to $\mathbf{CP}_{U},\,\mathbf{CP}_{D}$ removal time and output transition times.

Note to Fig. 11

The shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS (Cont'd)

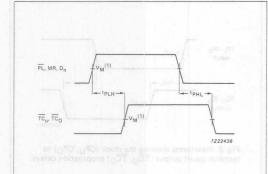


Fig. 12 Waveforms showing the data input (D $_{n}$), parallel load input (PL) and the master reset input (MR) to the terminal count outputs (\overline{TC}_{U} , \overline{TC}_{D}) propagation delays.

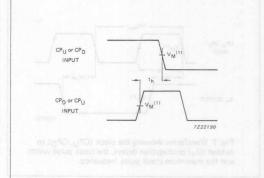
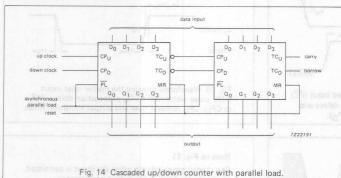


Fig. 13 Waveforms showing the CPU to CPD or CPD to CPU hold times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

APPLICATION INFORMATION



4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

FEATURES TO THE STATE OF THE ST

- · Shift-left and shift-right capability
- Synchronous parallel and serial data
- · Easily expanded for both serial and parallel operation
- Asynchronous master reset
- Hold ("do nothing") mode
- Output capability: standard
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT194 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The functional characteristics of the 74HC/HCT194 4-bit bidirectional universal shift registers are indicated in the logic diagram and function table. The registers are fully synchronous.

The "194" design has special features which increase the range of application. The synchronous operation of the device is determined by the mode select inputs (S₀, S₁). As shown in the mode select table, data can be entered and shifted from left to right $(Q_0 \rightarrow Q_1 \rightarrow Q_2, etc.)$ or,

right to left $(\ensuremath{\mbox{Q}}_3 \rightarrow \ensuremath{\mbox{Q}}_2 \rightarrow \ensuremath{\mbox{Q}}_1,\,\mbox{etc.})$ or parallel data can be entered, loading all 4 bits of the register simultaneously. When both So and S1 are LOW, existing data is retained in a hold ("do nothing") mode. The first and last stages provide D-type serial data inputs (DSR, DSL) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode select and data inputs are edgetriggered, responding only to the LOWto-HIGH transition of the clock (CP). Therefore, the only timing restriction is that the mode control and selected data (continued on next page)

MR 1	0	16 V _{CC}
D _{SR} 2	1	15 00
D ₀ 3		14 01
D ₁ 4		13 Q ₂
D ₂ 5	194	12 03
D ₃ 6		11 CP
D _{SL} 7		10 S ₁
GND 8		g S ₀
7	72931	37

	and the second second	CONDITIONS	TYP	UNIT		
SYMBOL	PARAMETER	CONDITIONS	НС	нст		
tPHL/	propagation delay CP to Q _n	1.101.91	14	15	ns	
^t PHL	MR to Q _n	C _L = 15 pF V _{CC} = 5 V	11	15	ns	
f _{max}	maximum clock frequency	50 50 52 1	102	77	MHz	
CI	input capacitance	90	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	40	40	pF	

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

f; = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

fo = output frequency in MHz $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is VI = GND to VCC For HCT the condition is $V_I = GND$ to VCC - 1.5 V

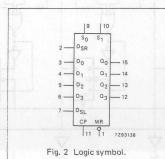
PACKAGE OUTLINES

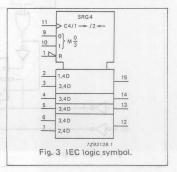
16-lead DIL; plastic (SOT38Z).

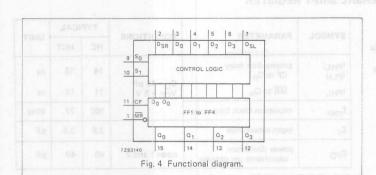
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1 2 3, 4, 5, 6 7	MR DSR D0 to D3 DSL GND	asynchronous master reset input (active LOW) serial data input (shift right) parallel data inputs serial data input (shift left) ground (0 V)
9, 10 11	S ₀ , S ₁ CP	mode control inputs clock input (LOW-to-HIGH edge-triggered)
15, 14, 13, 12 16	Q ₀ to Q ₃	parallel outputs positive supply voltage







FUNCTION TABLE

0050471110440050				INPL	JTS			OUTPUTS				
OPERATING MODES	СР	MR	S ₁	s ₀	DSR	DSL	Dn	Ω0	01	02	03	
reset (clear)	X	L	X	X	X	X	X	L	L	L	L	
hold ("do nothing")	X	Н	1.0	ŏj⁄ ∘	X	X	×	90	91	92	q3	
shift left	†	Н	h h	1	X	l h	×	91 91	92 92	q3	L H	
shift right	↑ ↑	Н	1	h h	h	X	X	L H	90 90	91 91	92 92	
parallel load	1	Н	h	h	X	X	dn	d ₀	d ₁	d ₂	d ₃	

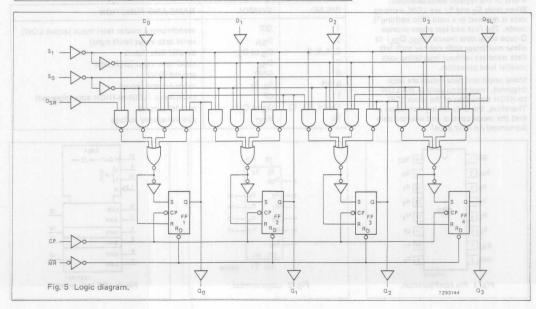
GENERAL DESCRIPTION (Cont'd.)

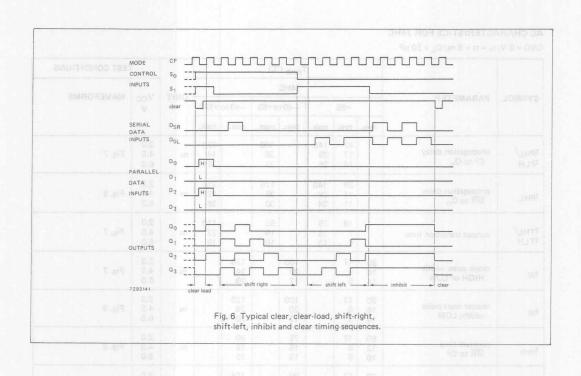
inputs must be stable one set-up time prior to the positive transition of the clock pulse.

The four parallel data inputs (D_0 to D_3) are D-type inputs. Data appearing on the D_0 to D_3 inputs, when S_0 and S_1 are HIGH, is transferred to the Q_0 to Q_3 outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous master reset ($\overline{\rm MR}$) overrides all other input conditions and forces the Q0 outputs LOW.

The "194" is similar in operation to the "195" universal shift register, with added features of shift-left without external connections and hold ("do nothing") modes of operation.

- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
- L = LOW voltage level
- = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
- q,d= lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition
- X = don't care
- ↑ = LOW-to-HIGH CP transition





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	1000		See 1		T _{amb} (°C)			100	JURDAG	TEST CONDITIONS
OVMDOL	DADAMETED			-	74HC				UNIT	Vcc	WAVEFORMS
SYMBOL	PARAMETER		+25		-40 1	to +85	-40 to	0 +125	wets	V	WAVETONING
- 200		min.	typ.	max.	min.	max.	min.	max.	ngQ	JANES ATA	
^t PHL [/] ^t PLH	propagation delay CP to Q _n		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
^t PHL	propagation delay MR to Q _n		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
^t THL [/] ^t TLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
tw	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17	- high i	120 24 20		ns	2.0 4.5 6.0	Fig. 7
tw	master reset pulse width; LOW	80 16 14	17 6 5	beal-re	100 20 17	elo ligoir	120 24 20	FR	ns	2.0 4.5 6.0	Fig. 8
^t rem	removal time MR to CP	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t _{su}	set-up time D _n to CP	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 9
^t su	set-up time S ₀ , S ₁ to CP	80 16 12	22 8 6	noites	100 20 17	(NATOE)	120 24 20	NOS fair	ns	2.0 4.5 6.0	Fig. 10 State of s
t _{su}	set-up time DSR, DSL to CP	70 14 12	19 7 6		90 18 15		105 21 18		ns	2.0 4.5 6.0	Tegory: Mist
^t h	hold time D _n to CP	0 0 0	-14 -5 -4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 9
th	hold time S ₀ , S ₁ to CP	0 0 0	-11 -4 -3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 10
th	hold time DSR, DSL to CP	0 0 0	-17 -6 -5		0 0 0		0 0 0		ns	2.0 4.5 6.0	
f _{max}	maximum clock pulse frequency	6.0 30 35	31 93 111		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOA		an					
D _n D _{SR} , D _{SL} CP MR	0.15 0.15 0.50	4.6						
S _n	0.45	8.8						

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V; } t_r = t_f = 6 \text{ ns; } C_L = 50 \text{ pF}$

					T _{amb} (°C)					TEST CONDITIONS	
					74HC	T	777				WAVEFORMS	
SYMBOL	PARAMETER		+25	ipal ()	-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			300	
tPHL/ tPLH	propagation delay CP to Q _n		18	32		40		48	ns	4.5	Fig. 7	
^t PHL	p <u>rop</u> agation delay MR to Q _n		18	32		40		48	ns	4.5	Fig. 8 10 120 12	
^t THL/ ^t TLH	output transition time		7	15		19		22	ns	4.5	Fig. 7	
tW	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 7	
tw	master reset pulse width; LOW	16	7		20		24		ns	4.5	Fig. 8	
^t rem	removal time MR to CP	12	6		15		18		ns	4.5	Fig. 8	
t _{su}	set-up time D _n to CP	14	7		18		21		ns	4.5	Fig. 9	
t _{su}	set-up time S ₀ , S ₁ to CP	20	10		25		30		ns	4.5	Fig. 10	
t _{su}	set-up time DSR, DSL to CP	14			18		21		ns	4.5	Fig. 9	
^t h	hold time D _n to CP	0	-7		0		0		ns	4.5	Fig. 9	
^t h	hold time S ₀ , S ₁ to CP	0	-5		0		0		ns	4.5	Fig. 10	
th	hold time D _{SR} , D _{SL} to CP	0	-7		0		0		ns	4.5	Fig. 9	
f _{max}	maximum clock pulse frequency	30	70		24		20		MHz	4.5	Fig. 7	

AC WAVEFORMS

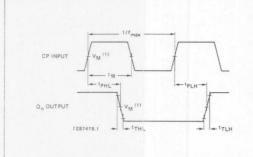


Fig. 7 Waveforms showing the clock (CP) to output (Q_{Π}) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

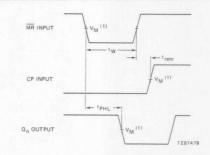


Fig. 8 Waveforms showing the master reset (\overline{MR}) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

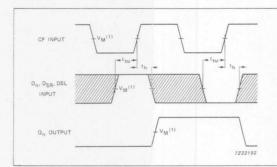


Fig. 9 Waveforms showing the set-up and hold times from the data inputs (D $_{\rm D}$, D $_{\rm SR}$ and D $_{\rm SL}$) to the clock (CP).

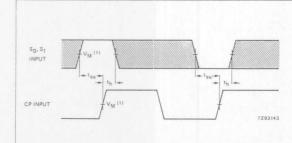


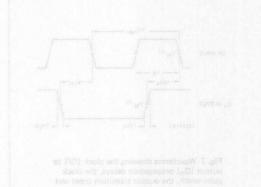
Fig. 10 Waveforms showing the set-up and hold times from the mode control inputs (S_n) to the clock input (CP).

Note to Figs 9 and 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

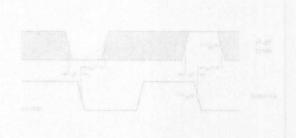
Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_1 = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_1 = GND$ to 3 V.









4-BIT PARALLEL ACCESS SHIFT REGISTER

FEATURES TENEDERGE MARRIED

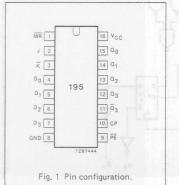
- Asynchronous master reset
- J, K, (D) inputs to the first stage
- Fully synchronous serial or parallel data transfer
- Shift right and parallel load capability
- Complement output from the last stage
- Output capability: standard
- · Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT195 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT195 performs serial, parallel, serial-to-parallel or parallel-toserial data transfer at very high speeds. The "195" operates on two primary modes: shift right $(Q_0 \rightarrow Q_1)$ and parallel load, which are controlled by the state of the parallel load enable (PE) input. Serial data enters the first flip-flop (Q0) via the J and \overline{K} inputs when the \overline{PE} input is HIGH and shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The J and K inputs provide the flexibility of the JR type input for special applications and by tying the pins together, the simple D-type input for general applications. The "195" appears as four common clocked D flip-flops when the PE input is I OW.

After the LOW-to-HIGH clock transition, data on the parallel inputs (D0 to D3) is transferred to the respective Q0 to Q3 outputs. Shift left operation (Q3 \rightarrow Q2) can be achieved by tying the Qn outputs to the Dn-1 inputs and holding the PE input LOW.

(continued on next page)



01/14001	242445750	CONDITIONS	TYP	LINUT		
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT	
tPHL/ tPLH	propagation delay CP to Q _n	CL = 15 pF VCC = 5 V	15	15	ns	
f _{max}	maximum clock frequency		57	57	MHz	
CI	input capacitance	HYMY	3.5	3.5	pF	
PD power dissipation capacitance per package		notes 1 and 2	105	105	pF	

Note

- 1. CPD is used to determine the dynamic power dissipation (P_D in μ W): PD = CPD × VCC² × f₁ + Σ (CL × VCC² × f₀) where:
 - f; = input frequency in MHz
- CL = output load capacitance in pF
- f_O = output frequency in MHz $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs
- VCC = supply voltage in V MOTTOMUF
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1,5 V

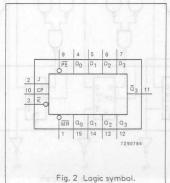
PACKAGE OUTLINES

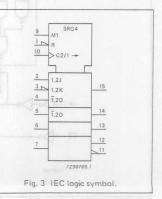
16-lead DIL; plastic (SOT38Z).

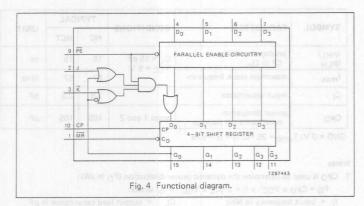
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1 2 3 4,5,6,7 8 9	MR J K Do to D3 GND PE CP	master reset input (active LOW) first stage J-input (active HIGH) first stage K-input (active LOW) parallel data inputs ground (0 V) parallel enable input (active LOW) clock input (LOW-to-HIGH edge-triggered)
15, 14, 13, 12 16	Q3 Q0 to Q3 VCC	inverted output from the last stage parallel outputs positive supply voltage







FUNCTION TABLE TO VIOLET TO V

0050471110440050		1	NPU	TS			OUTPUTS					
OPERATING MODES	MR	СР	PE	J	K	Dn	00	Q ₁	02	03	Q3	
asynchronous reset	L	X	X	X	X	X	E88	1200	L	р р	Н	
shift, set first stage	Н	1	h	h	h	X	Н	90	91	92	q 2	
shift, reset first stage	Н	1	h	1	1	X	L	90	91	92	92	
shift, toggle first stage	Н	1	h	h	1	X	<u>q</u> 0	90	91	92	q 2	
shift, retain first stage	Н	1	h	1	h	X	90	90	91	92	<u>q</u> 2	
parallel load	Н	1	1	X	X	dn	do	d1	d ₂	d3	d ₃	

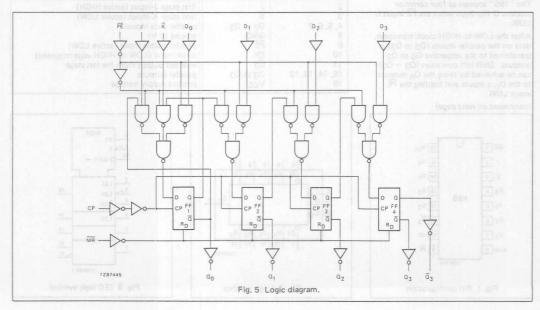
GENERAL DESCRIPTION

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition.

There is no restriction on the activity of the J, \overline{K} , D_n and $P\overline{E}$ inputs for logic operation other than the set-up and hold time requirements. A LOW on the asynchronous master reset (\overline{MR}) input sets all Q outputs LOW, independent of any other input condition.

APPLICATIONS

- Serial data transfer
- Parallel data transfer
- Serial-to-parallel data transfer
- Parallel-to-serial data transfer
- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
- L = LOW voltage level
- I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
- q, d = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition
- X = don't care
- = LOW-to-HIGH clock transition



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_1 = 50 \text{ pF}$

					T _{amb} (°C)				Т	EST CONDIT	IONS
			W.		74H				UNIT	Vcc	WAVEFORMS	
SYMBOL	PARAMETER		+25		-40 to +85		-40 to +12		UNIT	V CC	84.0 all ordered lis	
		min.	typ.	max.	min.	max.	min.	max.			00.0	cisitio ne
^t PHL/ ^t PLH	propagation delay CP to Q _n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6	
there and the state of the stat	propagation delay MR to Q _n		41 15 12	150 30 26	57 an	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	A.0 = 0h
tTHL/ tTLH	output transition time	201	19 7 6	75 15 13	TOH	95 19 16	PIC 4	110 22 19	ns	2.0 4.5 6.0	Fig. 6	JOSMY
t _W	clock pulse width HIGH or LOW	80 16 14	17 6 5	in	100 20 17	7 365	120 24 20	t min	ns	2.0 4.5 6.0	Fig. 6	
tw	master reset pulse width	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	UHS HUS
t _{rem}	removal time MR to CP	80 16 14	17 6 5	6	100 20 17		120 24 20		ns _{an}	2.0 4.5 6.0	Fig. 7	TUR
t _{su}	set-up time J to CP	100 20 17	33 12 10	8	125 25 21		150 30 26	20	ns	2.0 4.5 6.0	Figs 8 and 9	W
t _{su}	set-up time K, PE, D _n to CP	80 16 14	25 9 7	8	100 20 17		120 24 20	81	ns	2.0 4.5 6.0	Figs 8 and 9	mur
th	hold time J, K, PE, D _n to CP	3 3 3	-8 -3 -2	8	3 3 3		3 3 3	26	ns	2.0 4.5 6.0	Figs 8 and 9	Ú2
fmax	maximum clock pulse frequency	6 30 35	17 52 62	2	5 24 28	8	4 20 24	16	MHz	2.0 4.5 6.0	Fig. 6	Us

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
PE	0.65
all others	0.35

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		88			T _{amb} (°C)				Т	EST CONDITIONS	
01/14001	2.0 En 6	22		1	74HC	Т	V e		UNIT	N/PU	WAVEFORMS	
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		ritbiw W/G	esiug stadio V	
t _{PHL} /	propagation delay CP to Ω _n		18	32	00	40	1	48	ns	4.5	Fig. 6	
^t PHL	propagation delay MR to Qn		17	35	1 8	44		53	ns	4.5	Fig. 7	
tTHL/ tTLH	output transition time		7	15	0	19		22	ns	4.5	Fig. 6	
tw	clock pulse width HIGH or LOW	20	6 08	T	25		30	100 2	ns	4.5	Fig. 6	
tW	master reset pulse width LOW	16	6		20		24	17	ns	4.5	Fig. 7	
t _{rem}	removal time MR to CP	16	6		20		24	18	ns	4.5	Fig. 7	
t _{su}	set-up time J, K, PE to CP	20	12	8	25		30	2000	ns	4.5	Figs 8 and 9	
t _{su}	set-up time D _n to CP	16	6	9	20		24	8	ns	4.5	Figs 8 and 9	
th	hold time J, K, PE, D _n to CP	3	-5	2	3		3	36	ns	4.5	Figs 8 and 9	
^f max	maximum clock pulse frequency	27	52		22		18		MHz	4.5	Fig. 6	

AC WAVEFORMS

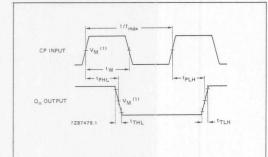


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

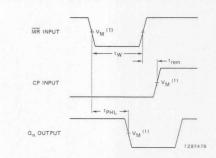


Fig. 7 Waveforms showing the master reset (\overline{MR}) pulse width, the master reset to output (\overline{Q}_n) propagation delays and the master reset to clock (\overline{CP}) removal time

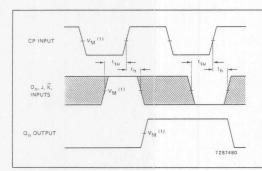


Fig. 8 Waveforms showing the data set-up and hold times for J, \overline{K} and D_n inputs.

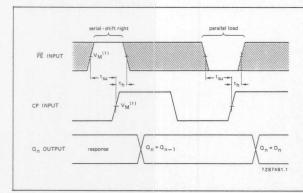


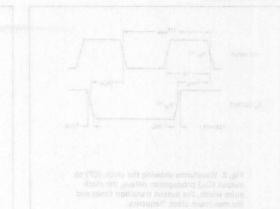
Fig. 9 Waveforms showing the set-up and hold times from the parallel enable input (\overline{PE}) to the clock (CP).

Note to Figs. 8 and 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

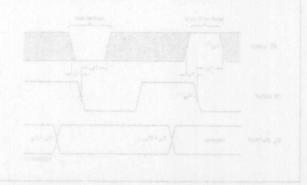
Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.









SUPERSEDES DATA OF APRIL 1988 DUAL NON-RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

FFATURES

- Pulse width variance is typically less than ± 5%
- Pin-out identical to "123"
- Overriding reset terminates output pulse
- nB inputs have hysteresis for improved noise immunity
- Output capability: standard (except for nR_{EXT}/C_{EXT})
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT221 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

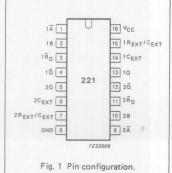
The 74HC/HCT221 are dual nonretriggerable monostable multivibrators. Each multivibrator features an active LOW-going edge input (nA) and an active HIGH-going edge input (nB), either of which can be used as an enable input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the nB inputs allow jitter-free triggering from inputs with slow transition rates, providing the circuit with excellent noise immunity.

Once triggered, the outputs $(nQ, n\overline{Q})$ are independent of further transitions of $n\overline{A}$ and nB inputs and are a function of the timing components. The output pulses can be terminated by the overriding active LOW reset inputs $(n\overline{R}_D)$. Input pulses may be of any duration relative to the output pulse.

Pulse width stability is achieved through internal compensation and is virtually independent of $V_{\rm CC}$ and temperature. In most applications pulse stability will only be limited by the accuracy of the external timing components.

(continued on next page)



SYMBOL	PARAMETER	CONDITIONS	TYF	PASSING.		
	FARAMETER	CONDITIONS	нс	нст	UNIT	
^t PHL ^t PLH	propagation delay nĀ, nB, nRD to nQ, nQ nĀ, nB, nRD to nQ, nQ	C _L = 15 pF VCC = 5 V REXT = 5 kΩ CEXT = 0 pF	29 35	32 36	ns ns	
CI	input capacitance	ylonem yel naggi	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	90	96	pF	

GND = 0 V; Tamb = 25 °C; tr = tf = 6 ns

Notes

- 1. Cpp is used to determine the dynamic power dissipation (P_D in μW):

 P_D = Cp_D × V_{CC}² × f_i + Σ (C_L × V_{CC}² × f_o) + 0.33 × C_EXT ×

 V_{CC}² × f_o + D × 28 × V_{CC} where:
 - f_i = input frequency in MHz f_o = output frequency in MHz
- Σ (C_L x V_{CC}² x f₀) = sum of outputs C_EXT = timing capacitance in pF
- 2. For HC the condition is V_I = GND to V_{CC}
- For HCT the condition is $V_I = GND$ to $V_{CC} 1.5 V$

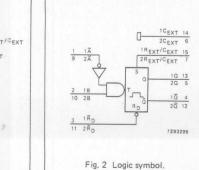
PACKAGE OUTLINES

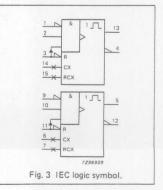
16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1Ā, 2Ā	trigger inputs (negative-edge triggered)
2, 10	1B, 2B	trigger inputs (positive-edge triggered)
3, 11	1RD, 2RD	direct reset inputs (active LOW)
4, 12	10, 20	outputs (active LOW)
7	2REXT/CEXT	external resistor/capacitor connection
8	GND	ground (0 V) work shall be for not 2 mig bins
13, 5	10, 20	outputs (active HIGH)
14,6	1CEXT, 2CEXT	external capacitor connection
15	1REXT/CEXT	external resistor/capacitor connection
16	Vcc	positive supply voltage





CL = output load capacitance in pF

V_{CC} = supply voltage in V D = duty factor in %

GENERAL DESCRIPTION

The output pulse width is defined by the following relationship:

tw = CEXTREXTIn2 tw = 0.7CEXTREXT

Pin assignments for the "221" are identical to those of the "123" so that the "221" can be substituted for those products in systems not using the retrigger by merely changing the value of R_{EXT} and/or C_{EXT} .

FUNCTION TABLE

11	NPUTS	3	OUTPUTS						
$n\overline{R}_{D}$	nĀ	nB	nQ	nΩ					
L	X	X	L L (1)	H H (1)					
X	X		L (1)	H (1)					
H	Ţ	↑ H		7.					
1	L	Н	(2)	7_ (2)					

H = HIGH voltage level L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH level

= HIGH-to-LOW level

= one HIGH-level output pulse



 If the monostable was triggered before this condition was established the pulse will continue as programmed.

2. For this combination the reset input must be LOW and the following sequence must be used: pin 1 (or 9) must be set HIGH or pin 2 (or 10) set LOW; then pin 1 (or 9) must be LOW and pin 2 (or 10) set HIGH. Now the reset input goes from LOW-to-HIGH and the device will be triggered.

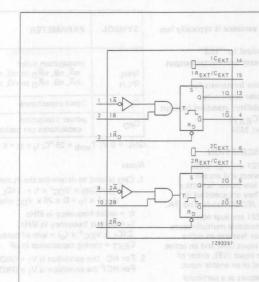
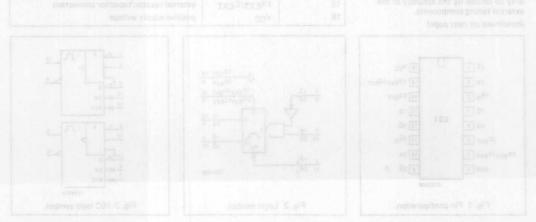
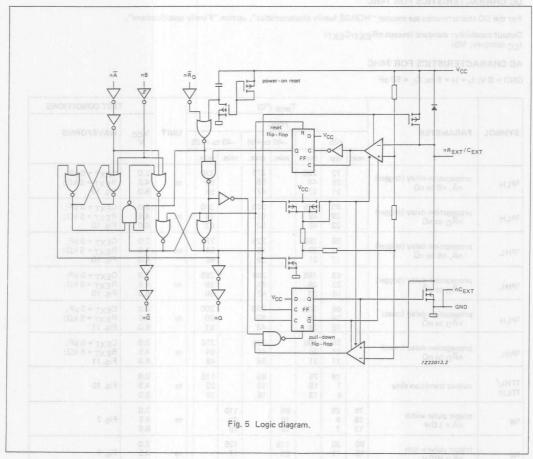


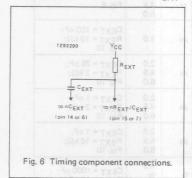
Fig. 4 Functional diagram.





Note

It is recommended to ground pins 6 (2CEXT) and 14 (1CEXT) externally to pin 8 (GND).



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except nR_{EXT}/C_{EXT}) I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	7				Tamb	(°C)		TEST CONDITIONS			
	DARAMETER				74H0	0	- 1		UNIT		WAVEFORMS
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _C C	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
^t PLH	propagation delay (trigger) nĀ, nB to nQ		72 26 21	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	CEXT = 0 pF; $REXT = 5 k\Omega;$ Fig. 10
^t PLH	propagation delay (trigger) nRD to nQ		80 29 23	245 49 42		305 61 52		370 74 63	ns	2.0 4.5 6.0	CEXT = 0 pF; $REXT = 5 k\Omega;$ Fig. 10
^t PHL	propagation delay (trigger) nĀ, nB to nQ		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	CEXT = 0 pF; $REXT = 5 k\Omega;$ Fig. 10
^t PHL	propagation delay (trigger)		63 23 18	195 39 33		245 49 42	7	295 59 50	ns	2.0 4.5 6,0	CEXT = 0 pF; $REXT = 5 k\Omega;$ Fig. 10
^t PLH	propagation delay (reset) nRD to nQ		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	CEXT = 0 pF; REXT = 5 kΩ; Fig. 11
^t PHL	propagation delay (reset) nRD to nQ		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	CEXT = 0 pF; REXT = 5 kΩ; Fig. 11
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 10
tw	trigger pulse width nĀ = LOW	75 15 13	25 9 7	.016	95 19 16	5 Log	110 22 19		ns	2.0 4.5 6.0	Fig. 7
tW	trigger pulse width nB = HIGH	90 18 15	30 11 9		115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig. 7
tw	trigger pulse width nRD = LOW	75 15 13	25 9 7	Baiq	95 19 16	mente	110 22 19	00) 47 5	ns	2.0 4.5 6.0	Fig. 8
tW	output pulse width nQ = LOW nQ = HIGH	630	700	770	602	798	595	805	μs	5.0	C_{EXT} = 100 nF; R_{EXT} = 10 k Ω ; Fig. 10
tW	output pulse width nQ or nQ		140		-		-		ns	2.0 4.5 6.0	C _E XT = 28 pF; R _E XT = 2 kΩ; Fig. 10
t₩	output pulse width nQ or nQ		1.5		-		-		μs	2.0 4.5 6.0	CEXT = 1 nF; $REXT = 2 k\Omega;$ Fig. 10
tw	output pul <u>s</u> e width nQ or nQ		7		-		-		μs	2.0 4.5 6.0	$C_{EXT} = 1 \text{ nF};$ $R_{EXT} = 10 \text{ k}\Omega;$ Fig. 10
tw	pulse width match between circuits in the package		±2		-		-		%	4.5 to 5.5	CEXT = 1000 pF; REXT = 10 kΩ

e en landa		T _{amb} (°C) 74HC								TEST CONDITIONS		
	PARAMETER	+25			-40 to +8		+85 -40 to +12		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		RE	YMBOL PARAMET	
t _{rem}	removal time nRD to nA or nB	100 20 17	30 11 9	n Jose	125 25 21	9 .306	150 30 26	unim	ns	2.0 4.5 6.0	Fig. 9	
REXT	external timing resistor	10 2		1000 1000					kΩ	2.0 5.0	Fig. 12 Fig. 13	
C _{EXT}	external timing capacitor	no limits							pF	2.0 5.0	Fig. 12 Fig. 13	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for nR_{EXT}/C_{EXT}) I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nB	0.30
nĀ	0.50
nRD	0.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	14D 5.0 Fig. 13	T _{amb} (°C)								TEST CONDITIONS		
	pe s.d Fig. 13				74H			sop grti	ind lighterizes. The			
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
^t PLH	propagation delay (trigger) nA, nRD to nQ		30	50		63		75	ns	4.5	CEXT = 0 pF; $REXT = 5 k\Omega;$ Fig. 10	
^t PLH	propagation delay (trigger) nB to nQ		24	42		53		63	ns	4.5	CEXT = 0 pF; $REXT = 5 k\Omega;$ Fig. 10	
^t PHL	propagation delay (trigger) nĀ to nQ		26	44		55		66	ns	4.5	CEXT = 0 pF; REXT = 5 kΩ; Fig. 10	
^t PHL	propagation delay (trigger) nB to $n\overline{\mathbb{Q}}$		21	35		44		53	ns	4.5	CEXT = 0 pF; REXT = 5 kΩ; Fig. 10	
[†] PHL	propagation delay (trigger) $n\overline{R}_D$ to $n\overline{\Omega}$		26	43		54		65	ns	4.5	CEXT = 0 pF REXT = 5 kΩ; Fig. 10	
^t PHL	propagation delay (reset) nRD to nQ		26	43		54		65	ns	4.5	$C_{EXT} = 0 pF;$ $R_{EXT} = 5 k\Omega;$ Fig. 11	
^t PLH	propagation delay (reset) nRD to nQ		31	51		64		77	ns	4.5	CEXT = 0 pF; REXT = 5 kΩ; Fig. 11	

AC CHARACTERISTICS FOR 74HCT

SYMBOL	PARAMETER	ace	or 03	l na	T _{amb} (°C)	20			TEST CONDITIONS		
		XBE	L	rri "xė	74H	СТ	UNIT	Vcc	WAVEFORMS			
STWBOL	O.S		+25		-40	to +85	-40	to +125	Olvii	V	mit levories	
	rs 4.5 Fig. 9	min.	typ.	max.	min.	max.	min.	max.		Ā	or gRn men!	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 10	
tW	trigger pulse width nA = LOW	20	13		25	on'	30		ns	4.5	Fig. 10	
tw	trigger pulse width nB = HIGH	20	13		25		30		ns	4.5	Fig. 10	
tw	pulse width nRD = LOW	22	13	mailtast	28	natasi	33	nut 20M	ns see	4.5	Fig. 8 mans 30 and no	
tW	output pulse width nQ = LOW nQ = HIGH	630	700	770	602	798	595	805	μs	5.0	CEXT = 100 nF; REXT = 10 kΩ; Fig. 10	
t₩	trigger pulse width nQ or nQ	elt erle ti the ti	140	g at f th		inu s vo bsol Jin	i (pp)	Z.) zestu d eulsv s	ns (1999)	4.5	CEXT = 28 pF; REXT = 2 kΩ; Fig. 10	
t₩	trigger pulse width nQ or nQ		1.5		-		-		μs	4.5	CEXT = 1 nF; $REXT = 2 k\Omega;$ Fig. 10	
tw	trigger pulse width nQ or nQ		7		-		-		μs	4.5	CEXT = 1 nF; REXT = 10 k Ω ; Fig. 10	
^t rem	removal time nRp to nA or nB	20	12		25		30		ns aga	4.5	Fig. 9	
REXT	external timing resistor	2		1000	G-1 atr	477	-		kΩ	5.0	Fig. 13	
CEXT	external timing capacitor	no limits								5.0	Fig. 13	

AC WAVEFORMS

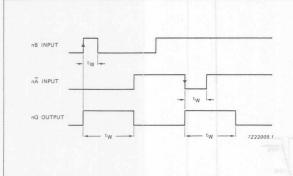


Fig. 7 Output pulse control; $n\overline{R}_D = HIGH$.

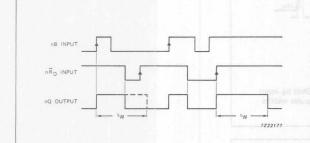
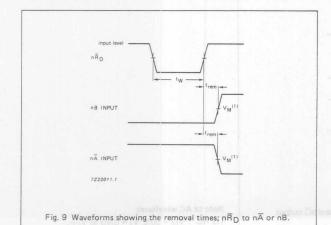
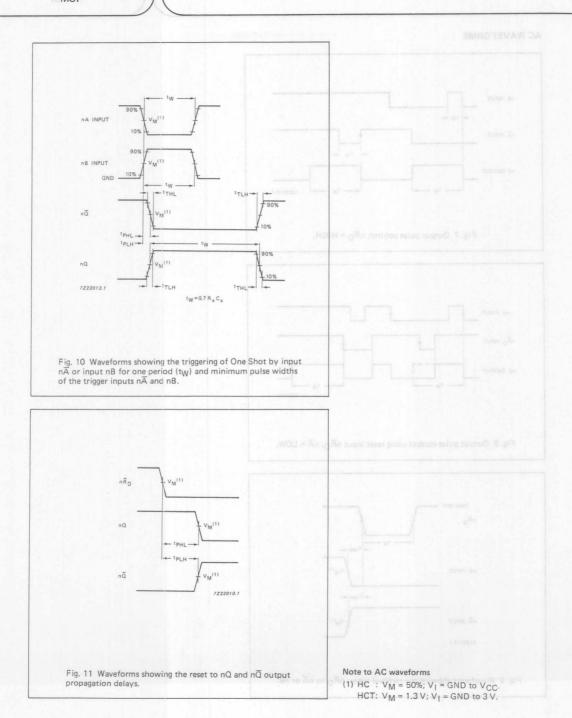
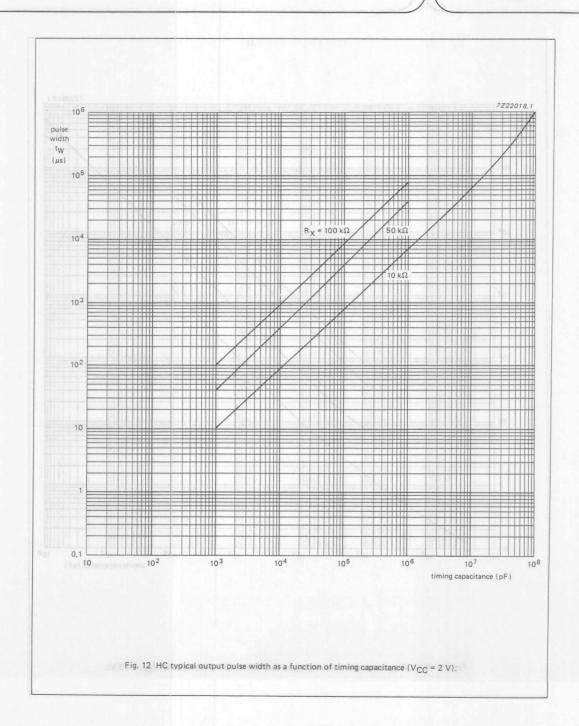
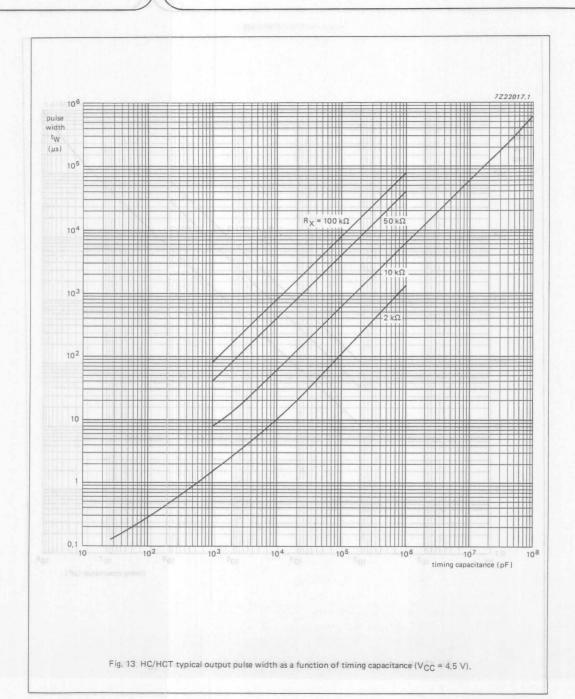


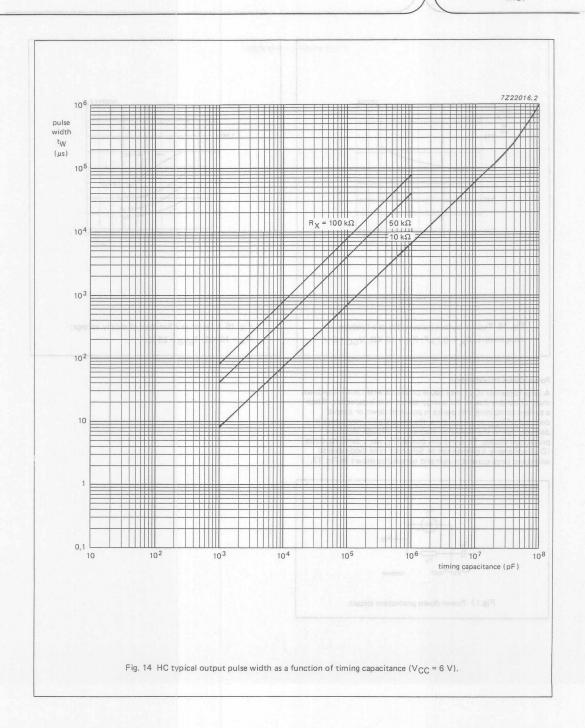
Fig. 8 Output pulse control using reset input $n\overline{R}_D$; $n\overline{A}$ = LOW.











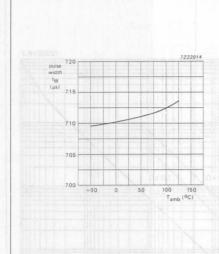


Fig. 15 Typical output pulse width as a function of temperature; $C_X = 0.1 \mu F$; $R_X = 10 K\Omega$; $V_{CC} = 5 V$.

0.9 H HHCT 0.9 C X = 0.001 µF 0.1 µF 0.1 µF 0.1 µF 0.1 µF 0.2 4 6 8 10 VCC (V)

Fig. 16 k factor as a function of supply voltage; $R_X = 10 \text{ K}\Omega$; $T_{amb} = 25 \,^{\circ}\text{C}$.

Power-down consideration

A large capacitor (C_X) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may substain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_X) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Fig. 17.

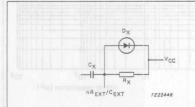


Fig. 17 Power-down protection circuit.

3-TO-8 LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

FEATURES

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active HIGH mutually exclusive outputs
- · Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT237 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT237 are 3-to-8 line decoder/demultiplexers with latches at the three address inputs (A_n). The "237" essentially combines the 3-to-8 decoder function with a 3-bit storage latch. When the latch is enabled (LE = LOW), the "237" acts as a 3-to-8 active LOW decoder. When the latch enable (LE) goes from LOW-to-HIGH, the last data present at the inputs before this transition, is stored in the latches. Further address changes are ignored as long as LE remains HIGH.

The output enable input $\{\overline{E}_1 \text{ and } E_2\}$ controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless \overline{E}_1 is LOW and E_2 is HIGH.

The "237" is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

		CONDITIONS	TYF	PICAL	UNIT
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
^t PHL [/] ^t PLH	propagation delay An to Yn LE to Yn E1 to Yn E2 to Yn	C _L = 15 pF V _{CC} = 5 V	16 19 14 14	19 21 17 17	ns ns ns ns
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	60	63	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

fo = output frequency in MHz VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

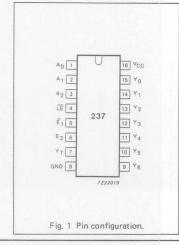
PACKAGE OUTLINES

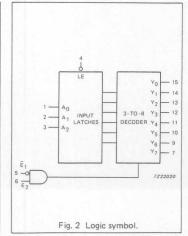
16-lead DIL; plastic (SOT38Z).

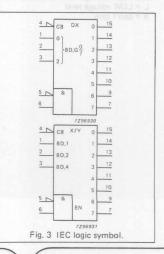
16-lead mini-pack; plastic (SO16; SOT109A).

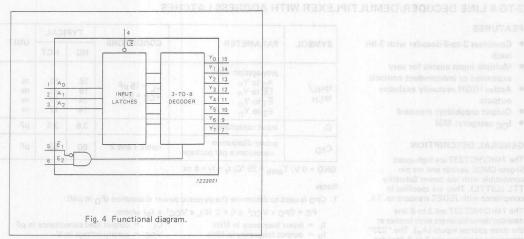
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A ₀ to A ₂	data inputs
4	LE J J J J	latch enable input (active LOW)
5	Ē ₁	data enable input (active LOW)
6	E ₂	data enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	Y ₀ to Y ₇	multiplexer outputs
16	Vcc	positive supply voltage









FUNCTION TABLE

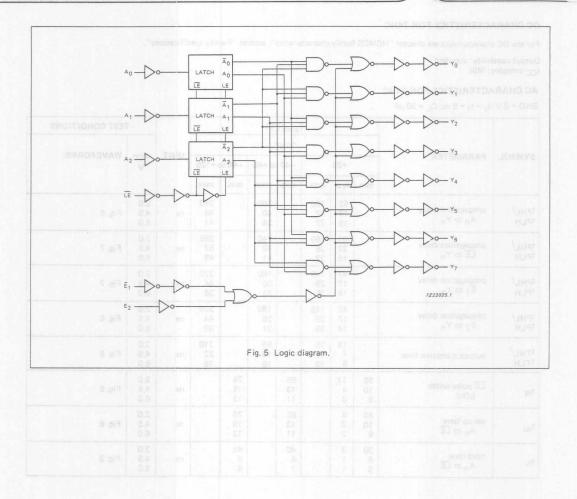
la i		INP	UTS					(TUC	PUT	S		VES
LE	Ē ₁	E ₂	A ₀	A ₁	A ₂	Y ₀	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Н	L	Н	X	X	X				sta	ble			
X	H X	X	X	X	X	HA	L	L	L	L L	L	Lo	L
L L L		HHHH	LHLH	LLHH		HLLL	LHLL	LLHL	L L H			L L L	
		TTTT	LHLH	LLLT	HHHH	L L L				HLLL	LHLL	L H L	TLLI

H = HIGH voltage level

L = LOW voltage level

X = don't care





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

				-0	T _{amb} (°C)	51	i. D			TEST CONDITIONS
		100			74H				LINUT	.,	WANTEODAK
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	VCC	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
tphl/ tplh	propagation delay An to Yn	+0<	52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
tPHL/	propagation delay		61 22 18	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 7
tphl/	propagation delay E ₁ to Y _n		47 17 14	145 29 25		180 36 31	-	220 44 38	ns	2.0 4.5 6.0	Fig. 7
tphl/	propagation delay E ₂ to Y _n		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13	o oigo.	95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
tw	LE pulse width	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 8
t _{su}	set-up time A _n to LE	50 10 9	6 2 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 8
th	hold time A _n to LE	30 6 5	3 1 1		40 8 7		45 9 8		ns	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
An	1.50
E ₁	1.50
E ₂	1.50
LE	1.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

					T _{amb} (°C)					TEST CONDITIONS
					74HC	T T	(S)	100			WAVEFERING
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	0 +125	UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/	propagation delay An to Yn		22	38		48	1	57	ns	4.5	Fig. 6
tPHL/	propagation delay LE to Y _n		25	42		53		63	ns	4.5	Fig. 7
t _{PHL} /	propagation delay E ₁ to Y _n		20	35		44	nit blo selva s	53	ns	4.5	Fig. 7 Walk B gra
tPHL/ tPLH	propagation delay E ₂ to Y _n		20	33		41		50	ns	4.5	Fig. 6
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 6
tw	LE pulse width HIGH	10	5	A GE SIN	13		15	SOUTH STATE	ns	4.5	Fig. 8
t _{su}	set-up time A _n to LE	10	2	HCL	13		15		ns	4.5	Fig. 8
th	hold time An to LE	5	0		5		5		ns	4.5	Fig. 8

AC WAVEFORMS

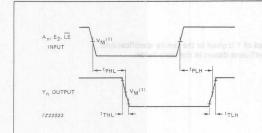


Fig. 6 Waveforms showing the address input (A_n) and enable inputs (E_2, \overline{LE}) to output (Y_n) propagation delays and the output transition times.

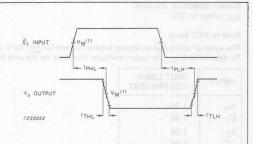


Fig. 7 Waveforms showing the enable input (\overline{E}_1) to output (Y_n) propagation delays and the output transition times,

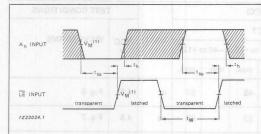


Fig. 8 Waveforms showing the data set-up, hold times for A_n input to \overline{LE} input and the latch enable pulse width.

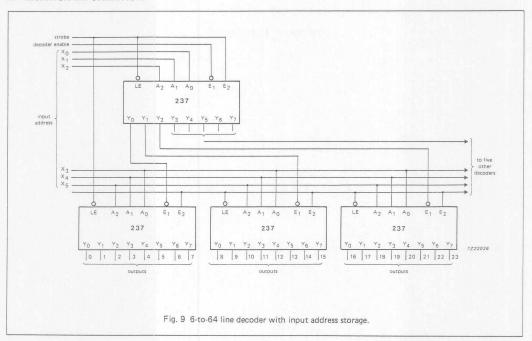
Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

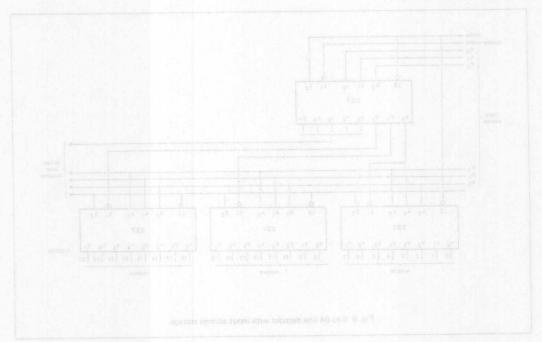
Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3$ V; $V_I = GND$ to 3 V.

APPLICATION INFORMATION



APPLICATION INFORMATION



3-TO-8 LINE DECODER/DEMULTIPLEXER

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active HIGH mutually exclusive outputs
- Output capability: standard
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT238 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

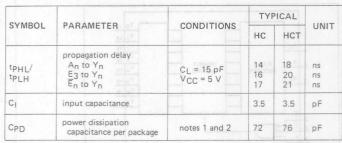
The 74HC/HCT238 decoders accept three binary weighted address inputs (A0, A1, A2) and when enabled, provide 8 mutually exclusive active HIGH outputs (Y_0 to Y_7).

The "238" features three enable inputs: two active LOW (\bar{E}_1 and \bar{E}_2) and one active HIGH (E_3). Every output will be LOW unless \bar{E}_1 and \bar{E}_2 are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the "238" to a 1-of-32 (5 lines to 32 lines) decoder with just four "238" ICs and one inverter.

The "238" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The "238" is identical to the "138" but has non-inverting outputs.



$$GND = 0 \text{ V}; T_{amb} = 25 \,^{\circ}\text{C}; t_r = t_f = 6 \text{ ns}$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD
$$\times$$
 VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is VI = GND to VCC For HCT the condition is VI = GND to VCC - 1.5 V

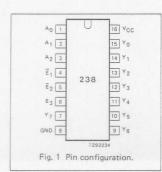
PACKAGE OUTLINES

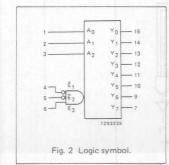
16-lead DIL; plastic (SOT38Z).

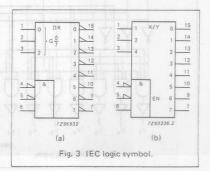
16-lead mini-pack; plastic (SO16; SOT109A).

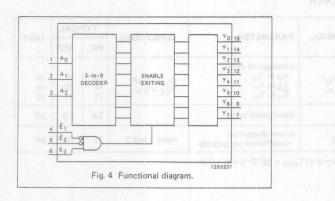
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3 4, 5 6 8	A_0 to A_2 \overline{E}_1 , \overline{E}_2 E_3 GND	address inputs enable inputs (active LOW) enable input (active HIGH) ground (0 V)
15, 14, 13, 12 11, 10, 9, 7 16	Y ₀ to Y ₇	outputs (active HIGH) positive supply voltage





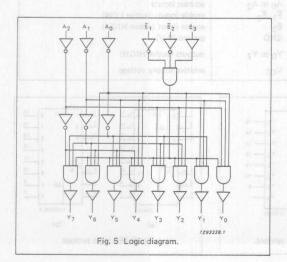




FUNCTION TABLE

	la mi	INF	UTS		NI SIDE	eran.	W 101	0	OUT	PUTS		ni v	INSUE	
Ē1	Ē ₂	E3	A ₀	A1	A ₂	Yo	Y1	Y ₂	Y3	Y4	Y5	Y6	Y7	
H X X	X H X	X X L	X X X	X X X	X X X	LLL	L L	L L	L		L	intro	L L	
LLLL	L L L	нинн	LHLH	L H H	L L L	HLLL	LHLL	L L H L	L L H	L	LLL	L		
L L L	L L L	HHH	L H L H	L H H	H H H	L L L	L L D(4	L L L		HLLL	L H L	L H L	L L L H ₃	H = HIGH L = LOW v X = don't (

H = HIGH voltage level L = LOW voltage level X = don't care





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC and and all and all the book arms and applied the rule videous messaging temperature and applied to suitar and

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_1 = 50 \text{ pF}$

					T _{amb} (°C)				G	TEST CONDITI	ONS
					74HC					FINE	10177500	
SYMBOL	PARAMETER		+25	. 11	-401	to +85	-40 to	o +125	UNIT	V _{CC}	WAVEFORMS	A n n n n
		min.	typ.	max.	min.	max.	min.	max.				
^t PHL/ ^t PLH	propagation delay A _n to Y _n		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6	C CHAR
^t PHL [/]	propagation delay E ₃ to Y _n		52 19 15	160 32 27	(5°) de	200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6	0-41
^t PHL [/]	propagation delay E _n to Y _n	125	50 18 14	155 31 26	+ or 0A	195 39 33	898	235 47 40	ns	2.0 4.5 6.0	Fig. 7	TOBIAS
t _{THL} /	output transition time	El	19 7 6	75 15 13	44	95 19 16	E P	110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7	JHdi
	ns 4,6 Fig. 6	83			44		35 7			yaleb	propagation A ₀ to Y ₀	MIG

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. EXECUTE TO determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
An En	0.70 0.40
E ₃	1.45

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

	4,5 Fig. 6 6.0	en	8			T _{amb} (°C)	9 32			Valsi	TEST CONDITIONS
						74HC	т				.,	WANTEODMO
SYMBOL	PARAMETER	in	71	+25		_40 ·	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS
	0.0		min.	typ.	max.	min.	max.	min.	max.			
^t PHL	propagation delay A _n to Y _n	an	8	21	35	BT	44		53	ns	4.5	Fig. 6
^t PLH	propagation delay A _n to Y _n			17	35		44		53	ns	4.5	Fig. 6
^t PHL	propagation delay E ₃ to Y _n			22	37		46		56	ns	4.5	Fig. 6
^t PLH	propagation delay E ₃ to Y _n			18	37		46		56	ns	4.5	Fig. 6
^t PHL	propagation delay En to Yn			21	35		44		53	ns	4.5	Fig. 7
^t PLH	propagation delay E _n to Y _n			18	35		44		53	ns	4.5	Fig. 7
t _{THL} / t _{TLH}	output transition time			7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

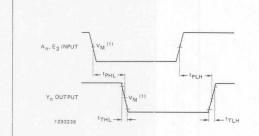


Fig. 6 Waveforms showing the address input (A_n) and enable input (E_3) to output (Y_n) propagation delays and the output transition times.

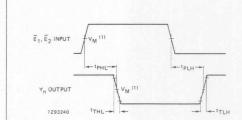


Fig. 7 Waveforms showing the enable input $(\overline{\mathbb{E}}_n)$ to output (Y_n) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

AC WAVEFORING

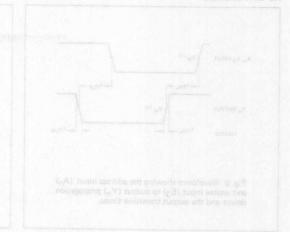




Fig. 7 Waveforms showing the enable input (E_n) to output (V_n) procedured delays and the output transition times.

amendayaya Did no seeds

(1) HC: VM = 50% VI = GND to VCD

OCTAL BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- · Output capability: bus driver
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT240 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT240 are octal inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The "240" is identical to the "244" but has inverting outputs.

FUNCTION TABLE

INP	UTS	OUTPUT
nŌĒ	nAn	nYn
L	L	Н
L	Н	L
H	X	Z

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYF	LIBILT	
		CONDITIONS	нс	нст	UNIT
^t PHL/ ^t PLH	propagation delay 1A _n to 1Y _n ; 2A _n to 2Y _n	C _L = 15 pF V _{CC} = 5 V	9	9	ns
CI	input capacitance	1 11 7	3.5	3.5	pF
C _{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

$$GND = 0 \text{ V; } T_{amb} = 25 \text{ °C; } t_r = t_f = 6 \text{ ns}$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

 $PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$ where:

f_i = input frequency in MHz f_o = output frequency in MHz

1Hz CL = output load capacitance in pF

VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is $V_I = GND$ to V_{CC} For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5$ V

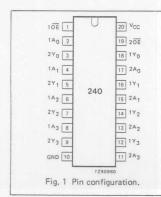
PACKAGE OUTLINES

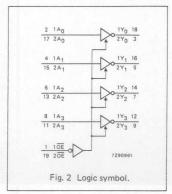
20-lead DIL; plastic (SOT146).

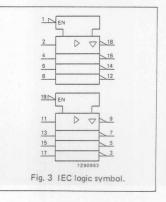
20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

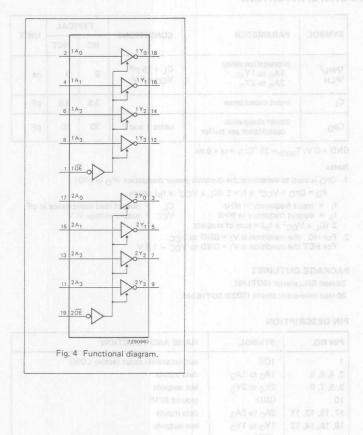
PIN NO.	SYMBOL	NAME AND FUNCTION	
1	10E	output enable input (active LOW)	
2, 4, 6, 8	1A ₀ to 1A ₃	data inputs	
3, 5, 7, 9	2Y ₀ to 2Y ₃	bus outputs	
10	GND	ground (0 V)	
17, 15, 13, 11	2A ₀ to 2A ₃	data inputs	
18, 16, 14, 12	1Y ₀ to 1Y ₃	bus outputs	
19	2 OE	output enable input (active LOW)	
20	Vcc	positive supply voltage	







OCTAL BUFFER/LINE DRIVER! 3-STATE-INVERTING



PEATURES

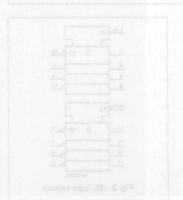
- Ourpur capability: but driver
 - CC category: MS1

SENERAL DESCRIPTION

The "MHC/HCT24D are high-speed S-gate CMDS devices and are pin comparible with low power Schottky TTL (LETTL). They are specified in compliance with JEDEC standard no.7A. The TAHC/HCT24D are octal inversing buffer-line drivers with 3-custe outputs. The 3-state outputs are committed by the AHGH on nOE causes the output and AHGH on nOE causes the outputs to secure a high incredence OFF-state. The "240" is identical to the "244" but The severting outputs.

FLINCTION TABLE

- iewel eostlov HDIH = H
 - rvol eosplov WOLF .
 - ensp 1 nob = 2
- Z = high impedance OPF-state







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", OTTAIN TO ANALYSIS OF

Output capability: bus driver

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	YMBOL PARAMETER		Tamb (°C) washind aulay and					o yiqirlun	TEST CONDITIONS					
SYMBOL				74HC						UNIT	Vcc	WAVEFORMS		
STIVIBUL	FARAIVII	EIEN			+25		-40 t	o +85	-40 to	-40 to +125		V	WAVETONING	
				min.	typ.	max.	min.	max.	min.	max.				nAl ac
tPHL/	propagat 1A _n to 2A _n to	1Yn;	,		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 5	301
tPZH/	3-state or 10E to 20E to	1Yn;	able time		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0		NO = 0 V;
^t PHZ [/] ^t PLZ	3-state or 10E to 20E to	1Yn;	able time		41 15 12	150 30 26	Sema T	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6	Indiava
tTHL/ tTLH	output tr	ransition	18	123 man	14 5 4	60 12 10	- Gia- -	75 15 13	428 .qv1	90 18 15	ns	2.0 4.5 6.0	Fig. 5	

DC CHARACTERISTICS FOR 74HCT virtually notified in notified in the control of the

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", and and reduce a section of the DC characteristics are chapter "HCMOS family characteristics", section "Family specifications", and and reduce a section of the DC characteristics are chapter "HCMOS family characteristics", section "Family specifications", and and reduce a section of the DC characteristics are chapter "HCMOS family characteristics", section "Family specifications", and and reduce a section of the DC characteristics are chapter to the DC cha

Output capability: bus driver

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
1An	1,50
1A _n	1,50
10E	0.70
20E	0.70

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		228		oer	T _{amb} (°C)			nit elde	TEST CONDITION	
4,5 Fig. 6		SE SE		74HCT		81		UNIT	Vcc	WAVEFORMS	
SYMBOL	PARAMETER	00 +25		75	-40 to +85		-40 to +125		Oldii	VCC	
4.5 Fig. 5 6.0		min.	typ.	max.	min.	max.	min.	max.	emiz	VIOLDIERS	
tPHL/	propagation delay 1A _n to 1Y _n ; 2A _n to 2Y _n		11	20		25		30	ns	4.5	Fig. 5
tPZH/ tPZL	3-state output enable time 10E to 1Yn; 20E to 2Yn		13	30		38		45	ns	4.5	Fig. 6
tPHZ/ tPLZ	3-state output disable time 10E to 1Yn; 20E to 2Yn		13	25		31		38	ns	4.5	Fig. 6
t _{THL} /	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

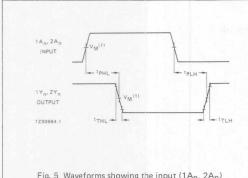


Fig. 5 Waveforms showing the input $(1A_n, 2A_n)$ to output $(1Y_n, 2Y_n)$ propagation delays and the output transition times.

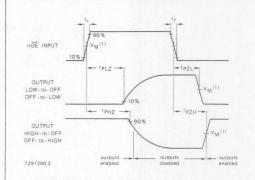
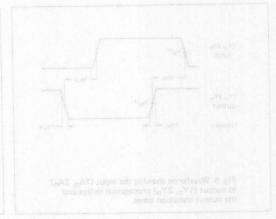


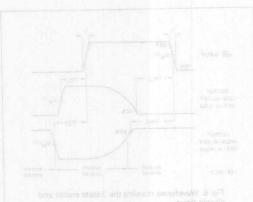
Fig. 6 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

AC WAVEFORM





Note to AC waveform

11) HO: $V_{M} = 50\%$; $V_{I} = GND$ to V_{CD} HCT: $V_{M} = 1.3 V$; $V_{I} = GND$ to SV_{CD}

OCTAL BUFFER/LINE DRIVER; 3-STATE

FEATURES

· Output capability: bus driver

· ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT241 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT241 are octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs 10E and 20E.

FUNCTION TABLES

INP	UTS	OUTPUT
10E	1A _n	1Y _n
L	L	L
L	Н	Н
H	X	Z

INP	UTS	OUTPUT	
20E	2A _n	2Y _n	
H H L	L H X	L H Z	

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYF	UNUT	
		CONDITIONS	нс	нст	UNIT
^t PHL [/] ^t PLH	propagation delay 1A _n to 1Y _n ; 2A _n to 2Y _n	C _L = 15 pF V _{CC} = 5 V	7	11	ns
CI	input capacitance		3.5	3.5	pF
CPD power dissipation capacitance per buffer		notes 1 and 2	30	30	pF

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD \times VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

f; = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

 f_0 = output frequency in MHz $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

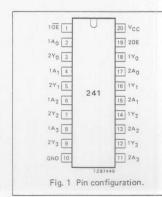
PACKAGE OUTLINES

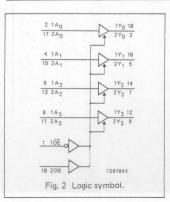
20-lead DIL: plastic (SOT146).

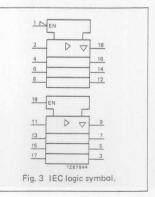
20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	10E	output enable input (active LOW)
2, 4, 6, 8	1A ₀ to 1A ₃	data inputs
3, 5, 7, 9	2Y ₀ to 2Y ₃	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	2A ₀ to 2A ₃	data inputs
18, 16, 14, 12	1Y ₀ to 1Y ₃	bus outputs
19	20E	output enable input (active HIGH)
20	Vcc	positive supply voltage







15 2A₁

13 2A2

11 2A3

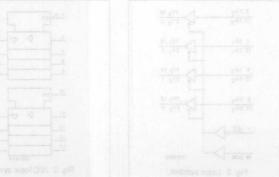
19 20E

nAt				

7287448 UT GMA BMAM Fig. 4 Functional diagram.

1 Y₀ 18

2 Y1 5





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

5,44	T _{amb} (°C)								CAC	TEST COND	ITIONS		
SYMBOL	DADAMETE	- D				74HC					THENT	COEFFE	10401
	PARAMETE	:H		+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFOR	
		min.	typ.	max.	min.	max.	min.	max.					
t _{PHL} /	propagation 1A _n to 1Y ₁ 2A _n to 2Y ₁	n;		25 9 7	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 5	C CHARA
t _{PZH} /	3-state outpo	ut enable time n; n		30 11 9	150 30 26	(5°) A	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6	V 0 - 30
tPHZ/ tPLZ	3-state output 10E to 1Y 20E to 2Y	ut disable time n;	125	39 14 11	150 30 26	TOHA	190 38 33	125	225 45 38	ns	2.0 4.5 6.0	Fig. 6	JOBNYS
t _{THL} / t _{TLH}	output trans	ition time	,XSH	14 5 4	60 12 10	in, m	75 15 13	itt agy	90 18 15	ns	2.0 4.5 6.0	Fig. 5	
	E.g. 5	E.P 98	64			2		S 61				ZA _n to 2Y	HJB

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1An	0.70
2An	0.70
10E	0.70
20E	1.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

	6,8	-86			T _{amb} (°C)				TEST CONDITIONS			
SYMBOL	PARAMETER	74HCT				UNIT	dae to h		/ZH9				
STIVIBUL	PANAMETER	80	+25		-40	to +85	40t	o+125	UNIT	V _{CC}	WAVEFORMS		
	2.0 Ro. 5	min.	typ.	max.	min.	max.	min.	max.	64	nia noki	output trans		
tPHL/	propagation delay 1A _n to 1Y _n ; 2A _n to 2Y _n	al	13	22		28		33	ns	4.5	Fig. 5	TLA T	
^t PZH [/] ^t PZL	3-state output enable time 10E to 1Yn; 20E to 2Yn		15	30		38		45	ns	4.5	Fig. 6		
^t PHZ/ ^t PLZ	3-state output disable time 10E to 1Yn; 20E to 2Yn		18	30		38		45	ns	4.5	Fig. 6		
^t THL/ ^t TLH	output transition time		5	12		15		18	ns	4.5	Fig. 5		

AC WAVEFORMS

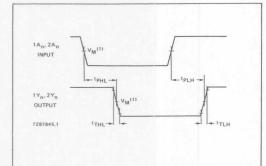


Fig. 5 Waveforms showing the input $(1A_n, 2A_n)$ to output $(1Y_n, 2Y_n)$ propagation delays and the output transition times.

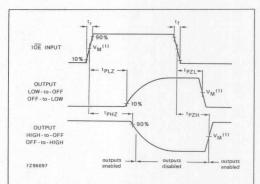


Fig. 6 Waveform showing the 3-state enable and disable times for input $1\overline{\text{OE}}$.

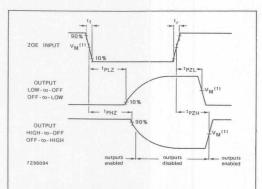
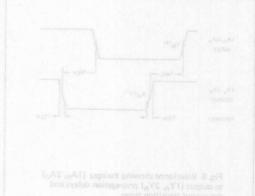


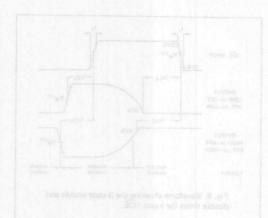
Fig. 7 Waveform showing the 3-state enable and disable times for input 20E.

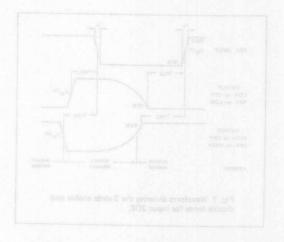
Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.









QUAD BUS TRANSCEIVER; 3-STATE; INVERTING

FEATURES

- Inverting 3-state outputs
- 2-way asynchronous data bus communication
- Output capability: bus driver
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT242 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT242 are quad bus transceivers featuring inverting 3-state bus compatible outputs in both send and receive directions. They are designed for 4-line asynchronous 2-way data communications between data buses.

The output enable inputs (OEA and OEB) can be used to isolate the buses.

The "242" is similar to the "243" but has inverting outputs.

SYMBOL PARAM	DADAMETER	CONDITIONS	TYF	UNIT	
	PARAMETER	CONDITIONS	НС	нст	UNIT
tPHL/ tPLH	propagation delay An to Bn; Bn to An	C _L = 15 pF V _{CC} = 5 V	7	10	ns
C _I stugni	input capacitance	rr 68	3.5	3.5	pF
C _{1/O}	input/output capacitance		10	10	pF
C _{PD}	power dissipation capacitance per transceiver	notes 1 and 2	29	32	pF

GND = 0 V;
$$T_{amb} = 25 \,^{\circ}\text{C}$$
; $t_r = t_f = 6 \, \text{ns}$

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

- fi = input frequency in MHz f_O = output frequency in MHz
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is VI = GND to VCC For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 V$

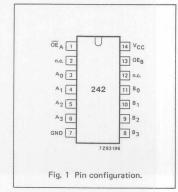
PACKAGE OUTLINES

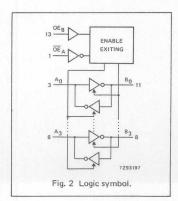
14-lead DIL; plastic (SOT27).

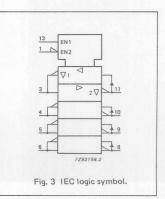
14-lead mini-pack; plastic (SO14; SOT108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	
1	ŌĒĄ	output enable input (active LOW)	
2, 12	n.c.	not connected	
3, 4, 5, 6	A ₀ to A ₃	data inputs/outputs	
7	GND	ground (0 V)	
11, 10, 9, 8	Bo to B3	data inputs/outputs	
13	OEB	output enable input	
14	Vcc	positive supply voltage	







CL = output load capacitance in pF

VCC = supply voltage in V

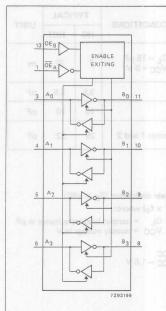


Fig. 4 Functional diagram.

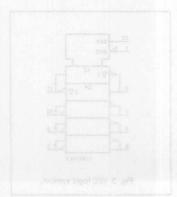
FUNCTION TABLE

INP	UTS	INPUTS	S/OUTPUTS
ŌĒĄ	OEB	An	B _n
L	L ing	inputs	$B = \overline{A}$
Н	L 00	Z	Z
L	Н	Z	Z
H	Н	$A = \overline{B}$	inputs

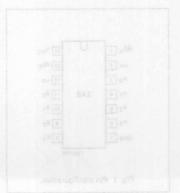
H = HIGH voltage level

L = LOW voltage level

Z = high impedance OFF-state







For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND =0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

		T _{amb} (°C)								TEST CONDITIONS		
	DARAMETER				74HC	;				ENT	COEFFICE	TUPIA
SYMBOL	PARAMETER		+25		-40	-40 to +85		o +125	UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
^t PHL/ ^t PLH	propagation delay A _n to B _n ; B _n to A _n		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 5	C CHAR
t _{PZH} /	3-state output enable time OE _A to A _n or B _n ; OE _B to A _n or B _n		41 15 12	150 30 26	105) 4	190 38 33		225 45 38	ns	2.0 4.5 6.0	Figs 6 and 7	NO - ON
^t PHZ [/]	3-state output disable time OE _A to A _n or B _n ; OE _B to A _n or B _n	357	52 19 15	150 30 26	T018	190 38 33	88	225 45 38	ns	2.0 4.5 6.0	Figs 6 and 7	TORMA
tTHL/	output transition time	,XEC	14 5 4	60 12 10	an an	75 15 13	en q	90 18 15	ns	2.0 4.5 6.0	Fig. 5	YJHS!
											B _m to A _m	HJ9

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT					
An	1.10					
Bn	1.10					
OE _A	1.00					
OE _B	1.00					

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	0.9 0.3 0.3	T _{amb} (°C)						amit a	TEST CONDITIONS		
SYMBOL	PARAMETER 8.4									WAVEFORMS	
		88 +25		-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} /	propagation delay A _n to B _n ; B _n to A _n	AL CL	12	20	21	25	ŠÍT -	30	ns	4.5	Fig. 5
tPZH/ tPZL	3-state output enable time OE _A to A _n or B _n ; OE _B to A _n or B _n		16	34		43		51	ns	4.5	Figs 6 and 7
tPHZ/	3-state output disable time $\overline{\text{OE}}_A$ to A_n or B_n ; OE_B to A_n or B_n		22	35		44		53	ns	4.5	Figs 6 and 7
tTHL/ tTLH	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

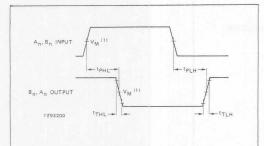


Fig. 5 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

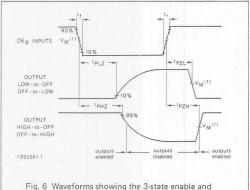


Fig. 6 Waveforms showing the 3-state enable and disable times for input ${\sf OE}_{\sf B}$.

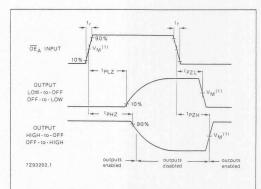
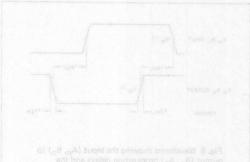
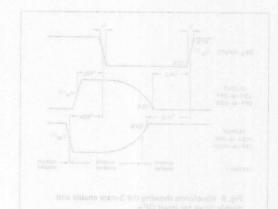


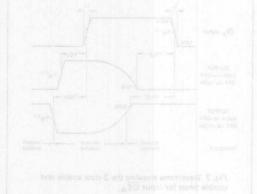
Fig. 7 Waveforms showing the 3-state enable and disable times for input $\overline{\text{OE}}_A.$

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.







QUAD BUS TRANSCEIVER; 3-STATE

- Non-inverting 3-state outputs
- 2-way asynchronous data bus communication
- Output capability: bus driver
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT243 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT243 are quad bus transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions. They are designed for 4-line asynchronous 2-way data communications between data buses.

The output enable inputs ($\overline{\text{OE}}_A$ and OE_B) can be used to isolate the buses.

The "243" is similar to the "242" but has non-inverting (true) outputs.

SYMBOL	PUNCTION TABLE	CONDITIONS	TYF			
STINIBUL	PARAMETER	CONDITIONS	НС	нст	UNIT	
tphL/ propagation delay tpLH An to Bn; Bn to An		C _L = 15 pF V _{CC} = 5 V	6	11	ns	
Cl	input capacitance	11 (2)	3.5	3.5	pF	
C _{1/O}	input/output capacitance		10	10	pF	
C _{PD}	power dissipation capacitance per transceiver	notes 1 and 2	26	34	pF	

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

- f; = input frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V fo = output frequency in MHz
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is $V_I = GND$ to V_{CC} For HCT the condition is $V_I = GND$ to $V_{CC} 1.5$ V

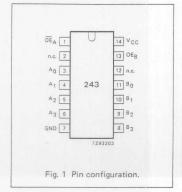
PACKAGE OUTLINES

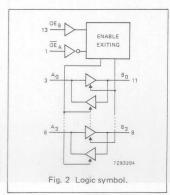
14-lead DIL; plastic (SOT27).

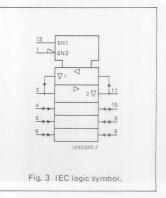
14-lead mini-pack; plastic (SO14; SOT108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1 2, 12 3, 4, 5, 6 7 11, 10, 9, 8 13 14	OE _A n.c. A ₀ to A ₃ GND B ₀ to B ₃ OE _B VCC	output enable input (active LOW) not connected data inputs/outputs ground (0 V) data inputs/outputs output enable input positive supply voltage







FUNCTION TABLE

	INP	UTS	INPUTS/OUTPUTS					
-	ŌĒA	OEB	An	B _n				
-	L H	Lind o	inputs Z	B = A				
	L H	H	Z A = B	Z inputs				

H = HIGH voltage level

L = LOW voltage level

Z = high impedance OFF-state



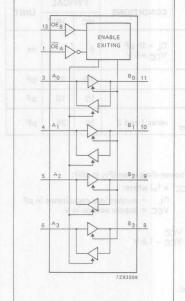
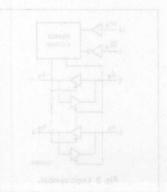


Fig. 4 Functional diagram.







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

Should be selected and specifications of the selection o

							T _{amb} (°C)					TEST CONDIT	IONS
0.410.01							74H				UNIT	Mas	WAVEFORM	IS A
SYMBOL	PARAMETE	:R			+25		-40	to +85	-40	to +125	UNII	VCC	WAVEFORM	15 A 36
		min. typ. max. min. max. min. m		max.			00.1							
t _{PHL} /	propagation A _n to B _n ; B _n to A _n	delay			22 8 6	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	○ Fig. 5 ∃TOA	
tPZH/	3-state outpu OE _A to A _n OE _B to A _n	or Bn;	e time		50 18 14	150 30 26	(p*) dr	190 38 33		225 45 38	ns	2.0 4.5 6.0	Figs 6 and 7	
t _{PHZ} / 21	3-state outpu OE _A to A _n OE _B to A _n	or Bn;	e time	125	61 22 18	165 33 28	+ 07 04	205 41 35	26	250 50 43	ns	2.0 A 4.5 6.0	Figs 6 and 7	TOBMAS
^t THL [/] ^t TLH	output trans		ne an	33	14 5 4	60 12 10	21	75 15 13	2 2	90 18 15	ns	2.0 4.5 6.0	nFig. 5 qorq	H18;

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	COEFFICIENT		
An an	1.10		
Bn	1.10		
OE _A	1.00		
OER	1.00		

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

	ns 4.5 Figs 6 and 7 8.0	82			T _{amb} (°C)	18 31	7		or 8m;	TEST CONDITION	VS
		036			74HC	т			UNIT	id vibati	WAVEFORMS	
SYMBOL	PARAMETER	-08		- 15	-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		No in	North Rang	
tPHL/	propagation delay An to Bn; Bn to An	81	13	22		28		33	ns	4.5	Fig. 5	HUT
tPZH/ tPZL	3-state output enable time OE _A to A _n or B _n ; OE _B to A _n or B _n		18	34		43		51	ns	4.5	Figs 6 and 7	ŀ
tPHZ/ tPLZ	3-state output disable time OE _A to A _n or B _n ; OE _B to A _n or B _n		23	35		44		53	ns	4.5	Figs 6 and 7	
t _{THL} /	output transition time		5	12		15		18	ns	4.5	Fig. 5	

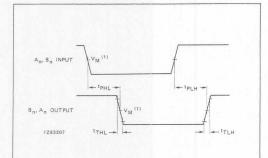


Fig. 5 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

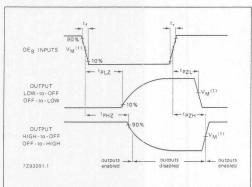


Fig. 6 Waveforms showing the 3-state enable and disable times for input ${\sf OE}_{\sf B}.$

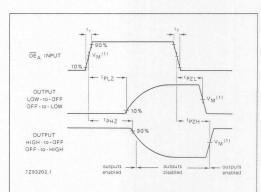
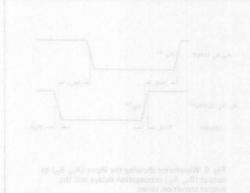


Fig. 7 Waveforms showing the 3-state enable and disable times for input \overline{OE}_A .

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.







OCTAL BUFFER/LINE DRIVER; 3-STATE

FEATURES

- · Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT244 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT244 are octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs 10E and 20E. A HIGH on nOE causes the outputs to assume a high impedance OFF-state.

The "244" is identical to the "240" but has non-inverting outputs.

FUNCTION TABLE

	INP	UTS	OUTPUT	
Ī	nŌĒ	nAn	nYn	
I	L	L	L	
	H	X	Z	

H = HIGH voltage level

L = LOW voltage level X = don't care

Z = high impedance OFF-state

		CONDITIONS	TYF			
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT	
tPHL/ propagation delay 1An to 1Yn; tPLH 2An to 2Yn		C _L = 15 pF V _{CC} = 5 V	9	11	ns	
CI	input capacitance	- 45	3.5	3.5	pF	
CPD power dissipation capacitance per buffer		notes 1 and 2	35	35	pF	

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD \times VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

CL = output load capacitance in pF VCC = supply voltage in V f; = input frequency in MHz

 f_0 = output frequency in MHz

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is VI = GND to VCC

For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 V$

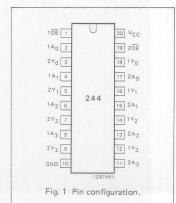
PACKAGE OUTLINES

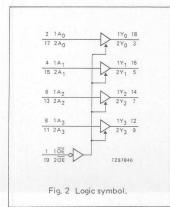
20-lead DIL; plastic (SOT146).

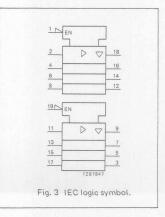
20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	10E	output enable input (active LOW)
2, 4, 6, 8	1A ₀ to 1A ₃	data inputs diagram. Fig. 4. Functional diagram
3, 5, 7, 9	2Y ₀ to 2Y ₃	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	2A ₀ to 2A ₃	data inputs
18, 16, 14, 12	1Y ₀ to 1Y ₃	bus outputs
19	20E	output enable input (active LOW)
20	Vcc	positive supply voltage







8 1A3

1 10E

15 2A₁

13 2A₂

11 2A3

19 20E O

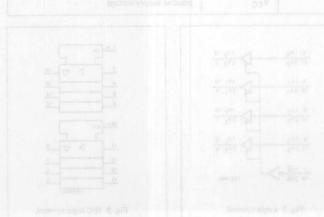
Fig. 4 Functional diagram.

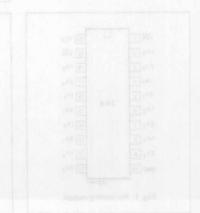
1 Y₀ 18

2 Y1

2 Y 2 7

2 Y3 9





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC and making the book manner of Lopida fraction vigous research books to outside $T_{\rm c} = 0.000$ and $T_{\rm c} = 0.0000$ and $T_{\rm c} = 0.0000$ and $T_{\rm c} = 0.0000$ and

						T _{amb}	(°C)				MBICIEM	TEST CON	IDITIONS
01/44001	DADAMETED			74HC						UNIT	V	WAVEFORMS	
SYMBOL	PARAMETER			+25		-40	-40 to +85		-40 to +125		V _{CC}	0.70	
			min.	typ.	max.	min.	max.	min.	max.			07.G	
tPHL/ tPLH	propagation delay 1A _n to 1Y _n ; 2A _n to 2Y _n			30 11 9	110 22 19		145 28 24		165 33 28	ns	2.0 4.5 6.0		C CHARA
tPZH/	3-state output enable 10E to 1Yn; 20E to 2Yn	e time		36 13 10	150 30 26	dons)	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6	
tPHZ/ tPLZ	3-state output disable 10E to 1Yn; 20E to 2Yn		Siros	39 14 11	150 30 26	SP=	190 38 33	+25	225 45 38	ns	2.0 4.5 6.0	Fig. 6	JOBMYS
t _{THL} /	output transition tin		simi,	14 5 4	60 12 10	rise	75 15 13	-qyz	90 18 15	ns	2.0 4.5 6.0	Fig. 5	less /
					-		- 20	101				ZA _{II} to	H.341

Octal buffler/line driver; 3-state

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. A STOARAHO DA To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1A _n	0.70
2A _n	0.70
1 <u>OE</u>	0.70
2OE	0.70

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

		38	T _{amb} (°C)							TEST CONDITIONS		
	2.0	223		190	74H	T	189		UNIT	Vcc	WAVEFORMS	
SYMBOL	PARAMETER	+25		33	-40 to +85		-40 to +125		ONT	V	PLZ 20E to	
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/ tPLH	propagation delay 1A _n to 1Y _n ; 2A _n to 2Y _n	15	13	22		28	8	33	ns	4.5	Fig. 5	
tPZH/	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$		15	30		38		45	ns	4.5	Fig. 6	
tPHZ/ tPLZ	3-state output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$		15	25		31		38	ns	4.5	Fig. 6	
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 5	

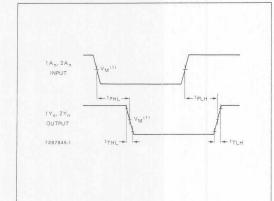


Fig. 5 Waveforms showing th input $(1A_n, 2A_n)$ to output $(1Y_n, 2Y_n)$ propagation delays and the output transition times.

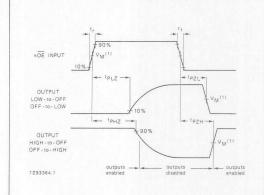
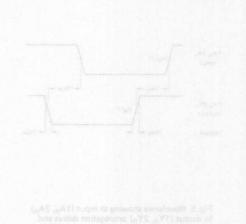
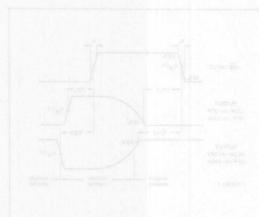


Fig. 6 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.





OCTAL BUS TRANSCEIVER: 3-STATE

FEATURES

- Octal bidirectional bus interface
- Non-inverting 3-state outputs
- · Output capability: bus driver
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT245 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT245 are octal transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The "245" features an output enable (OE) input for easy cascading and a send/receive (DIR) for direction control. OE controls the outputs so that the buses are effectively isolated. The "245" is similar to the "640" but has true (non-inverting) outputs.

FUNCTION TABLE

INF	PUTS	INPUTS	OUTPUTS		
ŌĒ DIR		An	Bn		
L	L	A = B inputs	inputs B = A		
H	X	Z	Z		

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

SYMBOL	DADAMETER	CONDITIONS	TYF	LIBILE		
	PARAMETER	CONDITIONS	нс	нст	UNIT	
tPHL/ propagation delay tPLH A _n to B _n ; B _n to A _n		C _L = 15 pF V _{CC} = 5 V	7	10	ns	
CI	input capacitance	81 00	3.5	3.5	pF	
C _{I/O}	input/output capacitance		10	10	pF	
C _{PD}	power dissipation capacitance per transceiver	notes 1 and 2	30	30	pF	

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x VCC^2 x f_i + Σ (CL x VCC^2 x f_o) where:

f; = input frequency in MHz fo = output frequency in MHz C_L = output load capacitance in pF V_{CC} = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

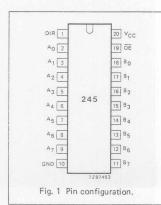
2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} – 1.5 V

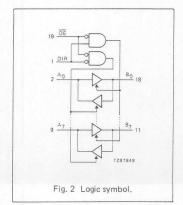
PACKAGE OUTLINE

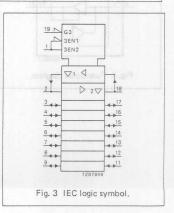
20-lead DIL; plastic (SOT146). 20-mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₇	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B ₀ to B ₇	data inputs/outputs
19	ŌĒ	output enable input (active LOW)
20	Vcc	positive supply voltage







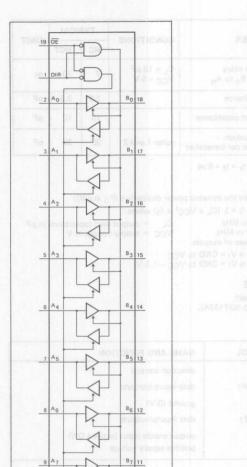






Fig. 4 Functional diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC

ACCHARACTERISTICS FOR 74HC and the property of the property o

		T _{amb} (°C)							TEST CONDITIONS			
	PARAMETER								.,	A, 0.40		
SYMBOL	PARAMETER	+25		-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.			0.90	
tPHL/ tPLH	propagation delay A _n to B _n ; B _n to A _n		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 5	AHD O
tpZH/	3-state output enable time $\overline{\text{OE}}$ to A_n ; $\overline{\text{OE}}$ to B_n signalname DIR		30 11 9	150 30 26	(0°1 dr	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6	
^t PHZ/ ²⁸	3-state output disable time OE to An; OE to Bn signalname DIR	125	41 15 12	150 30 26	40 to 4	190 38 33	25 m - cy	225 45 38	ns	2.0 4.5 6.0	Fig. 6	DEMY
t _{THL} / t _{TLH}	output transition time	8	14 5 4	60 12 10	28	75 15 13	2 2	90 18 15	ns	2.0 4.5 6.0	Fig. 5	UH9 HU9

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

Note to HCT types

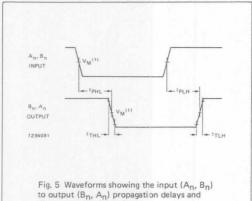
The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

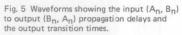
INPUT	UNIT LOAD COEFFICIENT
A _n	0.40
ŌĒ DIR	1.50 0.90

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

	0.8	- 88			T _{amb} (°C)	28	9		TEST CONDITIONS		
OVMDOL	DADAMETED O.S	74HCT						UNIT	Vcc	WAVEFORMS		
SYMBOL PARAMETER	PARAMETER	+25			-40 to +85		-40 to +125		ONT	V	WAVETOTTING	
		min.	typ.	max.	min.	max.	min.	max.		Bid	Ementangia	
^t PHL/ ^t PLH	propagation delay A _n to B _n ; B _n to A _n	01	12	22		28	4 6	33	ns	4.5	Fig. 5	
tpZH/ tpZL	3-state output enable time OE to An; OE to Bn signalname DIR		16	30		38		45	ns	4.5	Fig. 6	
^t PHZ [/] ^t PLZ	3-state output disable time OE to An; OE to Bn signalname DIR		16	30		38		45	ns	4.5	Fig. 6	
t _{THL} /	output transition time		5	12		15		18	ns	4.5	Fig. 5	





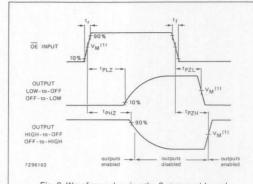
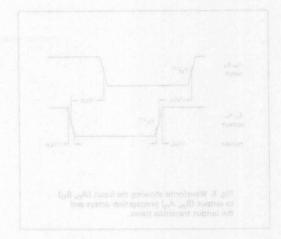
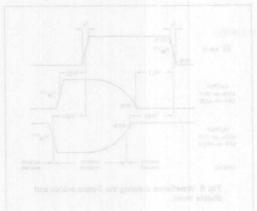


Fig. 6 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.





Note to AC waveforms

(1) HC: V_M = 50%; V₁ = 6ND to V_{CC}

8-INPUT MULTIPLEXER; 3-STATE

FEATURES

- True and complement outputs
- · Both outputs are 3-state for further multiplexer expansion
- Multifunction capability
- Permits multiplexing from n-lines to one line
- Output capability: standard
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT251 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT251 are the logic implementations of single-pole 8-position switches with the state of three select inputs (S_0, S_1, S_2) controlling the switch positions.

Assertion (Y) and negation (\overline{Y}) outputs are both provided.

The output enable input (\overline{OE}) is active LOW. The logic function provided at the output, when activated, is:

- $Y = \overline{OE}.(I_0.\overline{S}_0.\overline{S}_1.\overline{S}_2 + I_1.S_0.\overline{S}_1.\overline{S}_2 +$
 - + I2.So.S1.S2 + I3.So.S1.S2 +
 - + I4.50.51.S2 + I5.S0.51.S2 +
 - + I6.50.S1.S2 + I7.S0.S1.S2)

Both outputs are in the high impedance OFF-state (Z) when the output enable input is HIGH, allowing multiplexer expansion by tying the outputs.

		CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT	
	propagation delay	CH BH 21 61 EH 2	17 0			
t _{PHL} /	In to Y	C _L = 15 pF V _{CC} = 5 V	15 17	19 19	ns ns	
^t PLH	In to Y S _n to Y S _n to Y	VCC = 5 V	20 21	20 21	ns ns	
CI	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	44	46	pF	

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x VCC^2 x f_i + Σ (CL x VCC^2 x f_o) where:

f; = input frequency in MHz

fo = output frequency in MHz

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

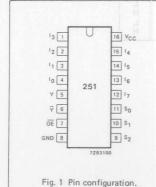
PACKAGE OUTLINES

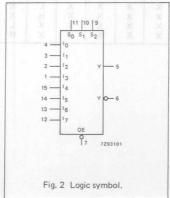
16-lead DIL; plastic (SOT38Z).

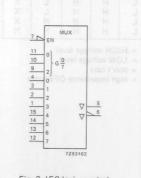
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	l ₀ to l ₇	multiplexer inputs
5	Y	multiplexer output
6 X 7	Y	complementary multiplexer output
7 × ×	ŌĒ	3-state output enable input (active LOW)
8	GND	ground (0 V)
11, 10, 9	S ₀ , S ₁ , S ₂	select inputs
16	S ₀ , S ₁ , S ₂ VCC	positive supply voltage







CL = output load capacitance in pF

VCC = supply voltage in V

Fig. 4 Functional diagram.

5

6

FUNCTION TABLE

					INP	UTS					· Fe	OUT	PUTS
ŌĒ	s ₂	S ₁	s ₀	10	11	12	13	14	15	16	17	∀ di	Y
Н	×	X	X	X	X	X	X	X	X	X	X	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	Н	L
L	L	L	H	H	X	×	×	×	X	X	X	H	108.
L	L	L	Н	X	Н	X	X	X	X	X	X	L 904	H
L	L	Н	L	X	X	L	X	X	X	X	X	Н	La La La
L	L	Н	L	^	X	Н	X	X	X	X	X	H	H
L	PLOT	H H	H	X	X	×	H	X	X	X X	X	L	Н
	Н	1	L	×	X	X	X	CIN	X	X	×××	Н	L
L	Н	L	L	×××	X	X	X	H	X	X X	X	L	Н
L	Н	L	Н		X	X	X	X	L		X	Н	L
L	Н	L	Н	X	X	X	X	X	Н	X	X	L	Н
L	Н	Н	L	X	X	X	X	X	X	L	X	Н	L
L	Н	Н	L	X	X	X	X	X	X	Н	X	L	Н
L	H H	H	H	X X	X X X	X	×	X	X	X	L	H	H

GND = 0 V; Tamp = 25 °C; c = 14 = 6 ns

1. Cpp is used to determine the dynam

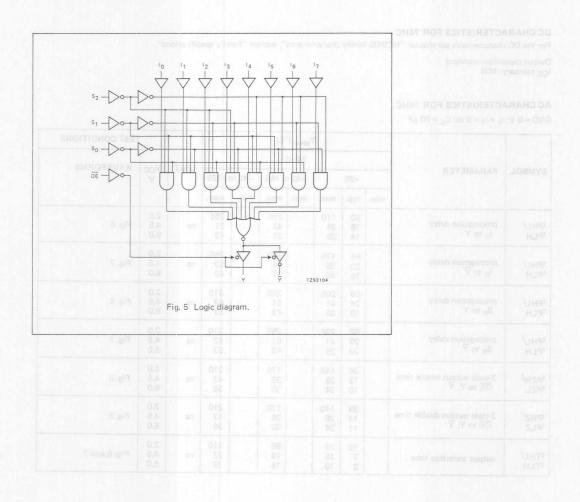
Pg = CPG x 10 - 5 (Ct x Vcc x 16) where

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)					TEST CONDITIONS
avano.	DADAMETER				74H0				LINUT		WAVEFORMS
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORINS
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/	propagation delay I _n to Y		50 18 14	170 34 29		215 43 37	Ų	255 51 43	ns	2.0 4.5 6.0	Fig. 6
tPHL/	propagation delay I _n to ₹		55 20 16	175 35 30	51	220 44 37	76.	265 53 45	ns	2.0 4.5 6.0	Fig. 7
tphl/	propagation delay S _n to Y		66 24 19	205 41 35		255 51 43	,insy	310 62 53	ns pi	2.0 4.5 6.0	Fig. 6
tPHL/	propagation delay S _n to \overline{Y}		69 25 20	205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 7
tPZH/ tPZL	3-state output enable time OE to Y, \overline{Y}		36 13 10	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
tPHZ/ tPLZ	3-state output disable time $\overline{\text{OE}}$ to Y, $\overline{\text{Y}}$		39 14 11	140 28 24		170 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
^t THL∕ ^t TLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I _n S ₀ S ₁ , S ₂ OE	1.00 1.50 1.50 1.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

					T _{amb} (°C)					TEST CONDITIONS
					74H	СТ				.,	may FORMS
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	+125	UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/	propagation delay		22	35		44		53	ns	4.5	Fig. 6
tPHL/ tPLH	propagation delay I_n to \overline{Y}		22	35		44	Wage	53	ns	4.5	Fig. 7
tPHL/ tPLH	propagation delay S _n to Y		24	44		55	ere no	66	ns	4.5	Fig. 6
tPHL/ tPLH	propagation delay S_n to \overline{Y}		25	44		55	bour 9	66	ns	4.5	Fig. 7
t _{PZH} /	3-state output enable time $\overline{\text{OE}}$ to Y, $\overline{\text{Y}}$		13	28		35		42	ns	4.5	Fig. 8
t _{PHZ} / t _{PLZ}	3-state output disable time $\overline{\text{OE}}$ to Y, $\overline{\text{Y}}$		14	28		35		42	ns	4.5	Fig. 8 Obyen OA of or
t _{THL} /	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

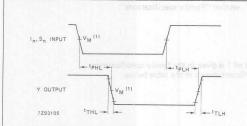


Fig. 6 Waveforms showing the multiplexer input (I_{Π}) and select input (S_{Π}) to output (Y) propagation delays and the output transition times.

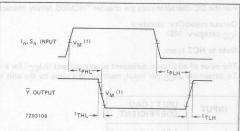
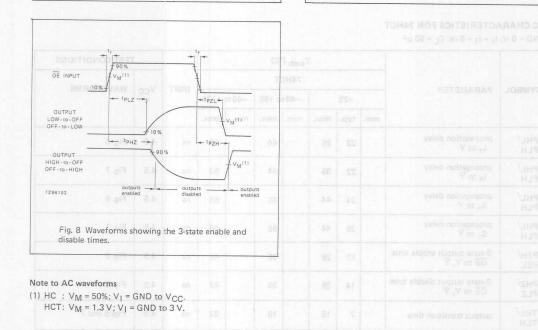


Fig. 7 Waveforms showing the multiplexer input (1_n) and select input (S_n) to output (\overline{Y}) propagation delays and the output transition times.



DUAL 4-INPUT MULTIPLEXER; 3-STATE

FEATURES

- · Non-inverting data path
- 3-state outputs for bus interface
- and multiplex expansion
- Common select inputs
- · Separate output enable inputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT253 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT253 have two identical 4-input multiplexers with 3-state outputs which select two bits from four sources selected by common data select inputs (S₀, S₁).

When the individual output enable (10E, 20E) inputs of the 4-input multiplexers are HIGH, the outputs are forced to the high impedance OFF-state. The "253" is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to S0 and S1.

The logic equations for the outputs are:

$$\begin{aligned} 1 &= 1 \overline{OE}(11_0.\overline{S}_1.\overline{S}_0 + 11_1.\overline{S}_1.S_0 + \\ &+ 11_2.S_1.\overline{S}_0 + 11_3.S_1.S_0) \\ 2 &= 2 \overline{OE}(21_0.\overline{S}_1.\overline{S}_0 + 21_1.\overline{S}_1.S_0 + \\ &+ 21_2.S_1.\overline{S}_0 + 21_3.S_1.S_0) \end{aligned}$$

APPLICATIONS

- Data selectors
- Data multiplexers

		CONDITIONS	TY	PICAL	LIBLIT
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
^t PHL [/] ^t PLH	propagation delay 1I _n , 2I _n to nY; S _n to nY	C _L = 15 pF V _{CC} = 5 V	17	17 19	ns
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	55	55	pF

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W): AT MOTTOWUR

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

- fi = input frequency in MHz fo = output frequency in MHz
- C_L = output load capacitance in pF V_{CC} = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

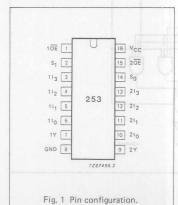
PACKAGE OUTLINES

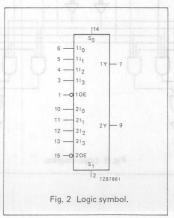
16-lead DIL; plastic (SOT38Z).

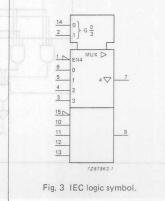
16-lead mini-pack; plastic (SO16; SOT109A).

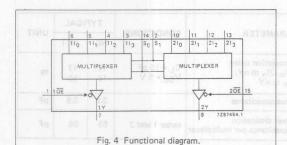
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	10E, 20E	output enable inputs (active LOW)
14, 2	S ₀ , S ₁	common data select inputs
7, 9	1Y, 2Y	3-state multiplexer outputs
8	GND	ground (0 V)
6, 5, 4, 3	11 ₀ to 11 ₃	data inputs from source 1
10, 11, 12, 13	21 ₀ to 21 ₃	data inputs from source 2
16	Vcc	positive supply voltage









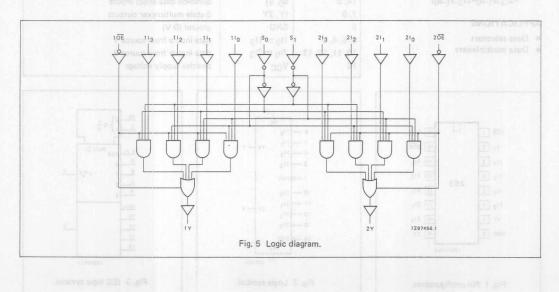
FUNCTION TABLE of gold and a second power dissipation (Fig. 18 and an interest of the second power dissipation). I

SEL	200,704,00	natioad V ni	ATA	INPUT	S	OUTPUT ENABLE	OUT	PUT	the sounds tredness 1 = input frequent 20 × 202 = 09
s ₀	S ₁	nI ₀	nl ₁	nl ₂	nl3	nŌĒ	nY		Z (C _L x V _{CC} ² x t _o) 2. For HC the condit
X	X	X	X	X	X	-HIOV of O			For HCT the conditi
L H H	L L L	L H X	X X L H	X X X	× × ×	L L L (A80	L H L		PACKAGE OUTLINI 16-lead DTL; plastic 180 16-lead mini-pack; plastic
L L H	H H H	X X X	X X X	L H X	X X L	NAME AN	L H L		H = HIGH voltage leve L = LOW voltage leve X = don't care Z = high impedance (

H = HIGH voltage level L = LOW voltage level X = don't care

Z = high impedance OFF-state

Common select inputs



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications" DR SELECTION SECTION (1997) AND DOCUMENT OF THE PROPERTY OF THE PROPERT

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb}	(°C)					TEST CONDIT	IONS
SYMBOL	PARAMETER				74H	С			UNIT	Vcc	WAVEFORM	TURMI
			+25		-40	to +85	-40 t	o +125	01111	V		
		min.	typ.	max.	min.	max.	min.	max.				
^t PHL/ ^t PLH	propagation delay 1I _n to nY; 2I _n to nY		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6	18
t _{PHL} /	propagation delay S _n to nY		58 21 17	175 35 30		220 44 37		265 53 45	ns Ro	2.0 4.5 6.0	Fig. 6	
t _{PZH} / ² / ² / ²	3-state output enable time nOE to nY		30 11 9	100 20 17	(°C) TOH	125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 7	
^t PHZ/	3-state output disable time nOE to nY	25 3x.	41 15 12	150 30 26	\$4.010 sm .rns	190 38 33	an la	225 45 38	ns	2.0 4.5 6.0	Fig. 7	YMBOL
^t THL [/] ^t TLH	output transition time		14 5 4	60 12 10	81-	75 15 13	38	90 18 15	ns	2.0 4.5 6.0	Fig. 6	HT _e

DC CHARACTERISTICS FOR 74HCT and all mail and contain the state of the

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
110	0.40
21 _n	0.40
nOE	1.10
Sn	1.10
S ₀ S ₁	1.10

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		DE			T _{amb} (°C)	100	30	. amiz	aldate	TEST CONDITIONS
		1	8		74H	СТ			der		Audison
SYMBOL	PARAMETER O.S.	1 05	+25		-401	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
^t PHL/	propagation delay 1I _n to nY; 2I _n to nY		20	38	\$1 81 81	48	GB 51 01	57	ns	4.5	Fig. 6
t _{PHL} /	propagation delay S _n to nY		22	40		50		60	ns	4.5	Fig. 6
tPZH/ tPZL	3-state output enable time nOE to nY		14	30		38		45	ns	4.5	Fig. 7
^t PHZ/ ^t PLZ	3-state output disable time nOE to nY		13	30		38		45	ns	4.5	Fig. 7
tTHL/ tTLH	output transition time		5	12		15		18	ns	4.5	Fig. 6

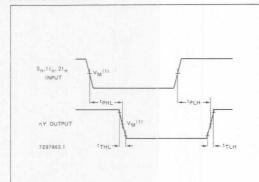


Fig. 6 Waveforms showing the input (11 $_{\rm II}$, 21 $_{\rm II}$) to output (1Y, 2Y) propagation delays and the output transition times.

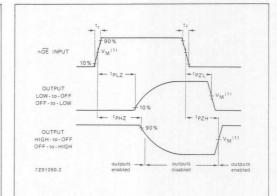
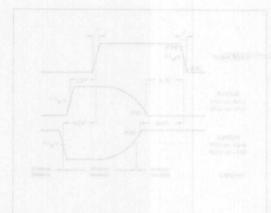


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.





Note to AC seletorins
(1) HC : V_M = 80%, V_I = 900 to V_{CC}

QUAD 2-INPUT MULTIPLEXER: 3-STATE

FEATURES

- Non-inverting data path
- 3-state outputs interface directly with system bus
- Output capability: bus driver
- · Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT257 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT257 have four identical 2-input multiplexers with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S).

The data inputs from source 0 (11₀ to 41₀) are selected when input 5 is LOW and the data inputs from source 1 (11₁ to 41₁) are selected when S is HIGH. Data appears at the outputs (1Y to 4Y) in true (non-inverting) form from the selected inputs.

The "257" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The outputs are forced to a high impedance OFF-state when OE is HIGH.

The logic equations for the outputs are:

$$1Y = \overline{OE}.(11_1.S + 11_0.\overline{S})$$

$$2Y = \overline{OE}.(2I_1.S + 2I_0.\overline{S})$$

$$3Y = \overline{OE}.(31_1.S + 31_0.\overline{S})$$

$$4Y = \overline{OE}.(41_1.S + 41_0.\overline{S})$$

The "257" is identical to the "258" but has non-inverting (true) outputs.

OVARDOL	DARAMETER	COMPITIONS	TYF	PICAL	LINUT
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
^t PHL/ ^t PLH	propagation delay nlg, nl ₁ to nY S to nY	C _L = 15 pF V _{CC} = 5 V	11 14	13 17	ns ns
Cı	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	45	45	pF

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

$$\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$$

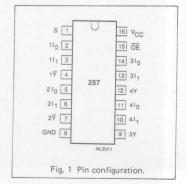
PACKAGE OUTLINES

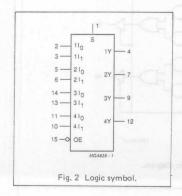
16-lead DIL; plastic (SOT38Z).

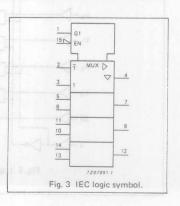
16-lead mini-pack; plastic (SO16; SOT109A).

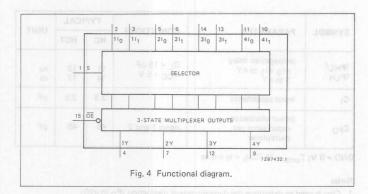
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 14, 11	11 ₀ to 41 ₀	data inputs from source 0
3, 6, 13, 10	11 ₁ to 41 ₁	data inputs from source 1
4, 7, 12, 9	1Y to 4Y	3-state multiplexer outputs
8	GND	ground (0 V)
15	ŌĒ	3-state output enable input (active LOW)
16	Vcc	positive supply voltage









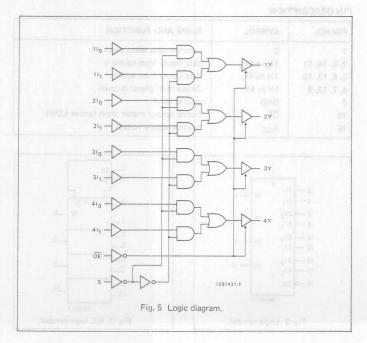
FUNCTION TABLE

	IN	OUTPUT		
ŌĒ	S	nlo	nl ₁	nY
Н	X	X	X	Z
L	Н	×	L	L
L	Н	X	Н	Н
L	L	L	X	L
L	L	Н	X	Н

H = HIGH voltage level

L = LOW voltage level

Z = high impedance OFF-state





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF with add of hoofs at 1 to be of sinularisation

SYMBOL						T _{amb} (°C)		TEST CONDITIONS				
					74H0	0	UNIT	THE	WAVEFORMS				
	PARAMETE		+25			-40 to +85		-40 to +125		VCC	WAVEFORM		
			min.	typ.	max.	min.	max.	min.	max.			1.35	
tPHL/	propagation nl ₀ to nY; nl ₁ to nY			36 13 10	110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 6	4 Q 4 W 7 7
tPHL/	propagation S to nY	delay		47 17 14	150 30 26	1011	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6 13 = 13 (V 0 = QV	
tPZH/	3-state outp	e	33 12 10	150 30 26	TON	190 38 33	26	225 45 38	ns	2.0 4.5 6.0	Fig. 7	доами	
^t PHZ [/] ^t PLZ	3-state output disable time OE to nY		ne xen	41 15 12	150 30 26	n n	190 38 33	im .q	225 45 38	ns	2.0 4.5 6.0	Fig. 7	
tTHL/ tTLH	output trans		an B	14 5 4	60 12 10	38	75 15 13	je j	90 18 15	ns	2.0 4.5 6.0	Fig. 6	HTA
	0.01	6.4-	4.0			2,0		35	20			Yn oz 8	HTM

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

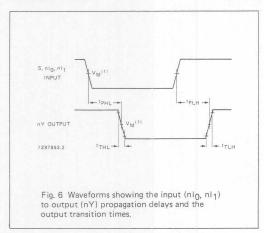
The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

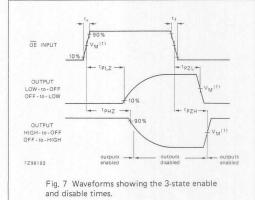
INPUT	UNIT LOAD COEFFICIENT
nlo	0.40
nl1	0.40
ŌĒ	1.35
S	0.70

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

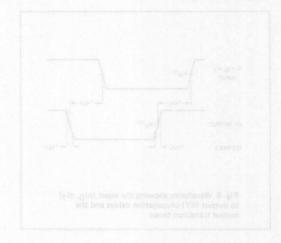
	H die		-				18		JSC N	1		140,000	THO LONG THE PARTY OF THE PARTY	MULL
SYMBOL		2.0	an	T _{amb} (°C)							UNIT	TEST CONDITIONS		
	DARAMET											Idane II	WAVEFORMS	/HZ97
	PARAMETER 0.8			+25		-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS		
				min.	typ.	max.	min.	max.	min.	max.	emit e	Cosib to	3-state outp	
tPHL/	propagation nl ₀ to nY; nl ₁ to nY		an	00	16	30	ς 1	38	4 67	45	ns	4.5	Fig. 6	VIHT
tPHL/ tPLH	propagation S to nY	delay			20	35	.3	44		53	ns	4.5	Fig. 6	Har
t _{PZH} / t _{PZL}	3-state output enable time OE to nY			15	30		38		45	ns	4.5	Fig. 7		
t _{PHZ} / t _{PLZ}	3-state output disable time OE to nY			16	30		38		45	ns	4.5	Fig. 7		
t _{THL} / t _{TLH}	output transition time				5	12		15		18	ns	4.5	Fig. 6	

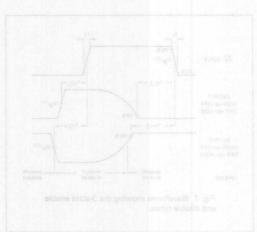




Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.





Note to AC waveforms
(1) HC: V_M = 50%:V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_S = GND to 3 V.

QUAD 2-INPUT MULTIPLEXER; 3-STATE; INVERTING

FEATURES

- Inverting data path
- 3-state outputs interface directly with system bus
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT258 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT258 have four identical 2-input multiplexers with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S).

The data inputs from source 0 (110 to 410) are selected when input S is LOW and the data inputs from source 1 (111 to 411) are selected when S is HIGH. Data appears at the outputs (1 \overline{Y} to 4 \overline{Y}) in inverted form from the select inputs. The "258" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S. The outputs are forced to a high impedance OFF-state when $\overline{\text{OE}}$ is HIGH.

The logic equations for the outputs are:

$$1\overline{Y} = \overline{OE}.(11_1.S + 11_0.\overline{S})$$

$$2\overline{Y} = \overline{OE}.(21_1.S + 21_0.\overline{S})$$

$$3\overline{Y} = \overline{OE}.(31_1.S + 31_0.\overline{S})$$

$$4\overline{Y} = \overline{OE}.(41_1.S + 41_0.\overline{S})$$

The "258" is identical to the "257" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYF	UNIT		
	PARAMETER	CONDITIONS	нс	нст	ONT	
^t PHL [/] ^t PLH	propagation delay nI ₀ , nI ₁ to nY S to nY	C _L = 15 pF V _{CC} = 5 V	9	13 16	ns ns	
Cl	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	55	38	pF	

GND = 0 V; $T_{amb} = 25 \,^{\circ}C$; $t_r = t_f = 6 \, \text{ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

$$f_{0}$$
 = output frequency in MHz $$V_{CC}$$ = supply voltage Σ (C $_{L}$ x $V_{CC}{}^{2}$ x f_{0}) = sum of outputs

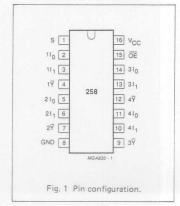
PACKAGE OUTLINES

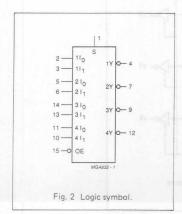
16-lead DIL; plastic (SOT38Z).

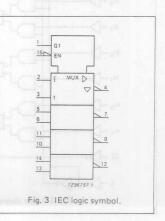
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION						
1	S	common data select input						
2, 5, 14, 11	11 ₀ to 41 ₀	data inputs from source 0						
3, 6, 13, 10 11 ₁ to 41 ₁		data inputs from source 1						
4, 7, 12, 9	1₹ to 4₹	3-state multiplexer outputs						
8	GND	ground (0 V)						
15 OE		3-state output enable input (active LOW)						
16	Vcc	positive supply voltage						







110 111

15 3-STATE MULTIPLEXER OUTPUTS 3Ÿ 4 12 9 7796758

5 6 14 13

SELECTOR

310 311

210 211

10 111

410 411

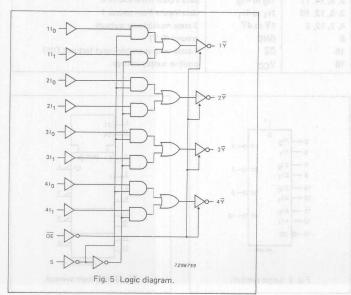
Fig. 4 Functional diagram.

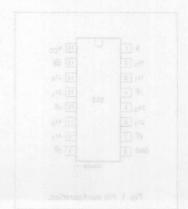
FUNCTION TABLE

	IN	OUTPUT		
ŌĒ	S	nI ₀	nl ₁	nΨ
Н	X	×	X	Z
L	Н	X	L	н
L	Н	X	Н	L
L	L	L	X	Н
L	L	Н	X	L

H = HIGH voltage level L = LOW voltage level X = don't care

Z = high impedance OFF-state





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC

					Tamb (°C)		TEST CONDITIONS				
CVMPOL	0404445750	74HC								TV	MANUFECTIAL	
SYMBOL	PARAMETER		+25		-40	-40 to +85 -40 to +125			UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay nl ₀ to $n\overline{Y}$; nl ₁ to $n\overline{Y}$		30 11 9	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig. 6	
tPHL/MON	propagation delay $S \text{ to } n\overline{Y}$		47 17 14	140 28 24	0°) ₈₁	175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 6	
tPZH/	3-state output enable time ○E to n♥	BS.F	39 14 11	140 28 24	61 04	175 35 30	25	210 42 36	ns	2.0 4.5 6.0	Fig. 7	
tPHZ/	3-state output disable time OE to nŸ	AST	55 20 16	150 30 26	(F) (F)	190 38 33	m .ey	225 45 38	ns	2.0 4.5 6.0	Fig. 7	
t _{THL} /	output transition time	18	14 5 4	60 12 10		75 15 13	e 34	90 18 15	ns	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", and solutions and SO side of

Output capability: bus driver ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nlo	0.50
nl ₁	0.50
ŌĒ	1.50
S	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V: $t_r = t_f = 6 \text{ ns}$; $C_1 = 50 \text{ pF}$

		T _{amb} (°C)								TEST CONDITIONS			
	0.8										WAVEFORMS		
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	Yn or 30		
		min.	typ.	max.	min.	max.	min.	max.		donit a	Security current		
tPHL/	propagation delay nl ₀ to $n\overline{Y}$; nl ₁ to $n\overline{Y}$	88	16	27	£	34	6 28 6 28 4 6	41	ns	4.5	Fig. 6	Z143 /2143	
tPHL/	propagation delay S to nY	8	19	34		43		51	ns	4.5	Fig. 6	HJT?	
tPZH/ tPZL	3-state output enable time OE to n Y		18	30		38		45	ns	4.5	Fig. 7		
t _{PHZ} / t _{PLZ}	3-state output disable time OE to n Y		17	30		38		45	ns	4.5	Fig. 7		
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6		

AC WAVEFORMS

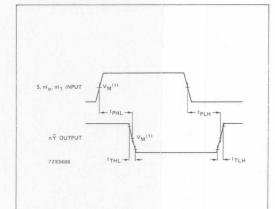


Fig. 6 Waveforms showing input (nI0, nI1, S) to output (n \overline{Y}) propagation delays and the output transition times.

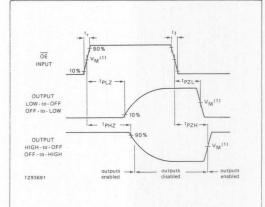


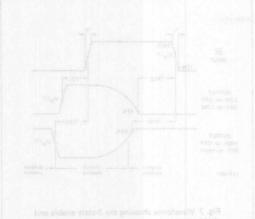
Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

AC WAVEFORING





More to AC vesustorms

(1) HC: V_M = 50%; V₁ = GND to V_{CC} HCT: V_M = 1.3 V, V₁ = GND to 3 V,

8-BIT ADDRESSABLE LATCH

FEATURES

- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Output capability: standard
- · Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT259 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT259 are high-speed 8-bit addressable latches designed for general purpose storage applications in digital systems. The "259" are multifunctional devices capable of storing single-line data in eight addressable latches, and also 3-to-8 decoder and demultiplexer, with active HIGH outputs (Q₀ to Q₇), functions are available.

The "259" also incorporates an active LOW common reset (MR) for resetting all latches, as well as, an active LOW enable input (LE).

(continued on next page)

		CONDITIONS	TYP	UNIT		
SYMBOL	PARAMETER	CONDITIONS	нс	нст	ONT	
^t PHL [/] ^t PLH ^t PHL	$\begin{array}{c} \text{propagation delay} \\ \text{D to } \Omega_n \\ \text{A}_n, \ \overline{\text{LE}} \text{ to } \Omega_n \\ \hline \overline{\text{MR}} \text{ to } \Omega_n \end{array}$	C _L = 15 pF V _{CC} = 5 V	18 17 15	20 20 20	ns ns	
CI	input capacitance	10 B ²	3.5	3.5	pF	
CPD	power dissipation capacitance per latch	notes 1 and 2	19	19	pF	

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD
$$\times$$
 VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

f; = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is $V_I = GND$ to V_{CC} For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5$ V

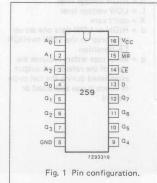
PACKAGE OUTLINES

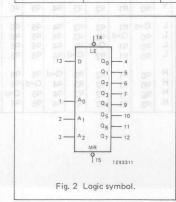
16-lead DIL; plastic (SOT38Z).

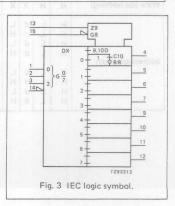
16-lead mini-pack; plastic (SO16; SOT109A).

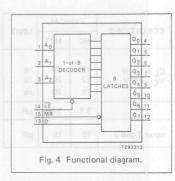
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A ₀ to A ₂	address inputs
4, 5, 6, 7, 9 10, 11, 12	Q ₀ to Q ₇	latch outputs
8	GND	ground (0 V)
13	D	data input
14-0	LE	latch enable input (active LOW)
15	MR	conditional reset input (active LOW)
16	Vcc	positive supply voltage









MODE SELECT TABLE

LE	MR	MODE	selfit ni yamupant tuqni 's
,	V ni	address blo levels	s Hill be yousuped sugue =
L	Н	addressable latch	(C) x Vec x (a) = sum of ourse
H	Н	memory	TWD will a heiribnes sits. OH to
L	L	active HIGH 8-channel dem	ultiplexer
Н	L	reset	THE - LAST HORSEMED BUT I PALETY

FUNCTION TABLE

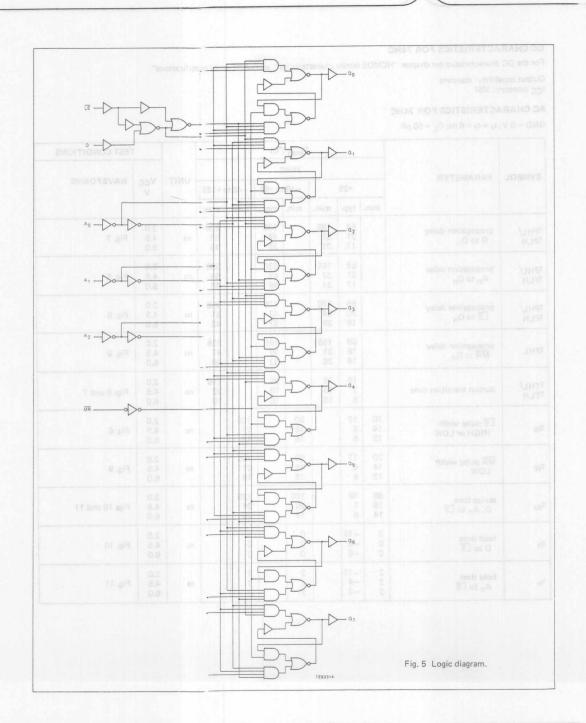
00504711040050			INP	UTS					(DUTP	UTS			
OPERATING MODES	MR	LE	D	A ₀	A ₁	A ₂	α ₀	01	02	03	04	05	06	07
master reset	F	Н	Х	X	X	X	L	Foe	L	L	L .0	L	L	L
demultiplex (active HIGH)			d d d d	L H L H	LLHH		Q=d L L L	L Q=d L L	L L Q=d L	L L Q=d	L L	L3 3 L3 3 L 01 L 01		LLLL
decoder (when D = H) (WO.J e		L	d d d	H L H	L H H	H H H	L L L	L L L		L L L	Q=d L L L	L Q=d L L	L L Q=d L	L L Q=d
store (do nothing)	Н	Н	X	X	X	X	90	91	92	q 3	94	95	96	97
addressable latch	HHHH		0 0 0 0	L H L H	L H H		Q=d q0 q0 q0	91 Q=d 91 91	92 92 Q=d 92	93 93 93 Q=d	94 94 94	95 95 95 95	96 96 96 96	97 97 97 97
and the state of t	HHHH		0000	L H L H	L H H	H H H	90 90 90 90	91 91 91 91	92 92 92 92	93 93 93	Q=d q4 q4 q4	95 Q=d 95 95	96 96 Q=d 96	97 97 97 Q=d

GENERAL DESCRIPTION

The "259" has four modes of operation as shown in the mode select table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs.

In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the state of the D input with all other outputs in the LOW state. In the reset mode all outputs are LOW and unaffected by the address (A0 to A2) and data (D) input. When operating the "259" as an addressable latch, changing more than one bit of address could impose a transient-wrong address. Therefore, this should only be done while in the memory mode. The mode select table summarizes the operations of the "259".

- H = HIGH voltage level
- L = LOW voltage level
- X = don't care
- d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH LE transition
- q = lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

			.0-	4	T _{amb} (°C)		-		TEST CONDITIONS		
			74HC									
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/	propagation delay D to Q _n		58 21 17	185 37 31	G,	230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 7	
tPHL/	propagation delay A _n to Q _n		58 21 17	185 37 31	d	230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 8	
t _{PHL} /	propagation delay LE to Q _n		55 20 16	170 34 29	g	215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6	
[†] PHL	p <u>rop</u> agation delay MR to Ω _n		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 9	
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13	d	95 19 16		119 22 19	ns	2.0 4.5 6.0	Figs 6 and 7	
tW	LE pulse width HIGH or LOW	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 6	
tw	MR pulse width LOW	70 14 12	17 6 5	4	90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 9	
t _{su}	set-up time D, A _n to LE	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Figs 10 and 11	
^t h	hold time D to LE	0 0 0	-19 -6 -5	4	0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 10	
^t h	hold time A _n to LE	2 2 2	-11 -4 -3		2 2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 11	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
An LE D MR	1.50 1.50 1.20 0.75

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

					T _{amb} (°C)		TV		TEST CONDITIONS		
CVMDOL	10,0				74H0	СТ	UNIT	Vcc	WAVEFORMS			
SYMBOL	PARAMETER	+25			-40 to +85			-40 to +125		V	WAVEFORING	
	may.	min.	typ.	max.	min.	max.	min.	max.		" wy	TURTUE D	
t _{PHL} / —	propagation delay D to Q _n	CINCT .	23	39		49	n Ad etc	59	ns	4.5	Fig. 7	
tPHL/	propagation delay	R) to th	25	41		51		62	ns	4.5	Fig. 8	
tPHL/	propagation delay LE to Q _n		22	38		48		57	ns	4.5	Fig. 6	
tPHL	propagation delay		23	39		49		59	ns	4.5	Fig. 9	
tTHL/	output transition time		7	15		19	-101-	22	ns	4.5	Figs 6 and 7	
tw	LE pulse width	19	11		24		29		ns	4.5	Fig. 6	
tW	MR pulse width	18	10	nns ns	23		27	1	ns	4.5	Fig. 9 - 10	
t _{su}	set-up time D to LE	17	10	di) di)	21	-rame	26	DU-798 6	ns	4.5	Fig. 10	
t _{su}	set-up time A _n to LE	17	10	180	21		26		ns	4.5	Fig. 11	
^t h	hold time D to LE	0	-8		0		0		ns	4.5	Fig. 10	
t _h	hold time An to LE	0	-4		0		0		ns	4.5	Fig. 11 - MV TOH	

AC WAVEFORMS

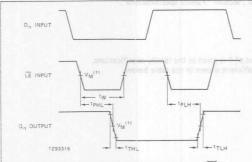


Fig. 6 Waveforms showing the enable input ($\overline{\text{LE}}$) to output (Q_{n}) propagation delays, the enable input pulse width and the output transition times.

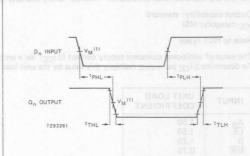


Fig. 7 Waveforms showing the data input (D) to output ($\mathbf{Q}_{\mathbf{D}}$) propagation delays and the output transition times. THAT ROT SOLTENS

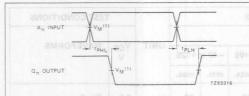


Fig. 8 Waveforms showing the address inputs (An) to outputs (Qn) propagation delays and the output transition times.

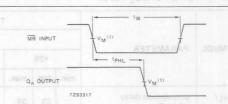
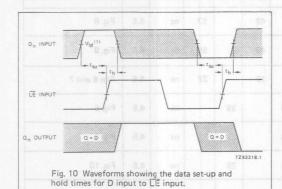


Fig. 9 Waveforms showing the conditional reset input (\overline{MR}) to output (Q_n) propagation delays.



Note to AC waveforms

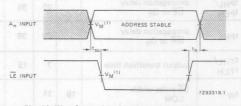


Fig. 11 Waveforms showing the address set-up and hold times for A_n inputs to \overline{LE} input.

Note to Figs 10 and 11

The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : $V_{M} = 50\%$; $V_{I} = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to 3 V}$.

OCTAL D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

FEATURES

- Ideal buffer for MOS microprocessor or memory
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- See "377" for clock enable version
- See "373" for transparent latch version
- See "374" for 3-state version
- Output capability; standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT273 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT273 have eight edgetriggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset (MR) inputs load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Ω_n) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the MR input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

			TYF			
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT	
^t PHL [/] ^t PLH	propagation delay <u>CP</u> to Q _n <u>MR</u> to Q _n	C _L = 15 pF V _{CC} = 5 V	15 15	15 20	ns ns	
fmax	maximum clock frequency	75 75	66	36	MHz	
Ci	input capacitance	2 10	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	23	pF	

$$GND = 0 \text{ V}; T_{amb} = 25 \,^{\circ}\text{C}; t_r = t_f = 6 \text{ ns}$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x VCC^2 x f_i + Σ (CL x VCC^2 x f_o) where:

fi = input frequency in MHz CI =

 f_0 = output frequency in MHz VCC = s

CL = output load capacitance in pF
VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} - 1.5 V

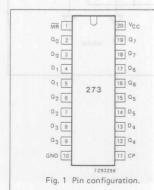
PACKAGE OUTLINES

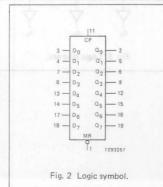
20-lead DIL; plastic (SOT146).

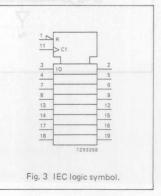
20-lead mini-pack; plastic (SO20; SOT163 A).

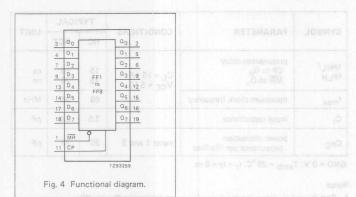
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	MR	master reset input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q ₀ to Q ₇	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D ₀ to D ₇	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	Vcc	positive supply voltage









FUNCTION TABLE

voltage in V		OUTPUTS		
OPERATING MODES	MR	СР	Dn	Qn
reset (clear)	L	X	X	L
load "1"	Н	1	h	H
load "0"	Н	1	I	Tos acoa :

H = HIGH voltage level

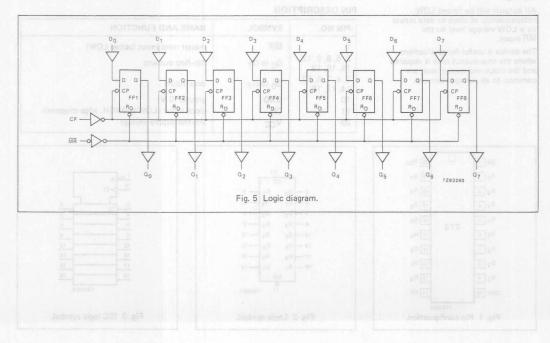
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

↑ = LOW-to-HIGH transition

X = don't care



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; tr = tr = 6 ns; Ct = 50 pF | mail with neview if to bad find a rol (2,314) member virgous tracestup isodribbs to sulev entities.

					T _{amb} (°C)					TEST CONDIT	IONS
SYMBOL	PARAMETER			V	74H		UNIT	Vcc	WAVEFORMS			
STIMBUL	PARAMETER	+25		-40 t		to +85 -40		-40 to +125		V	MR 1,00	
		min.	typ.	max.	min.	max.	min.	max.			81.0	
^t PHL [/]	propagation delay CP to Ω_{N}		41 15 13	150 30 26		185 37 31		225 45 38	ns TOHAT	2.0 4.5 6.0	Fig. 6	
^t PHL2MOT	propagation delay \overline{MR} to Q_n		44 16 14	150 30 26	(0°) di	185 37 31		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
t _{THL} / 2N	output transition time	125	19 7 6	75 15 13	10 to 4:	95 19 15	-25	110 22 19	ns	2.0 4.5 6.0	Fig. 6	
tw	clock pulse width HIGH or LOW	80 16 14	14 5 4	m .x	100 20 17	iri .x	120 24 20	anien	ns	2.0 4.5 6.0	Fig. 6	/_h
tW	master reset pulse width LOW	60 12 10	17 6 5		75 15 13		90 18 15	2	ns	2.0 4.5 6.0	Fig. 7	٤
t _{rem}	removal time MR to CP	50 10 9	-6 -2 -2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7	
t _{su}	set-up time D _n to CP	60 12 10	11 4 3	·S	75 15 13	2	90 18 15	B 81	ns _{cub}	2.0 4.5 6.0	Fig. 8	
^t h	hold time On to CP	3 3 3	-6 -2 -2	H	3 3 3		3 3	10 -	ns	2.0 4.5 6.0	Fig. 8	DR
f _{max}	maximum clock pulse frequency	6.0 30 35	20.6 103 122	BT	4.8 24 28	1	4.0 20 24	12 5	MHz	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
MR	1.00
CP	1.75
Dn	0.15

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

	rs 4.5 Fig. 7	10.00			T _{amb} (°C)	8 26				TEST CONDITIONS
OVMOOL	DADAMETED 0.9	101			74HC	СТ	UNIT	Vaa	WAVEFORMS		
SYMBOL	PARAMETER	64.63	+25		-401	to +85	-40 to	o +125	UNIT	VCC	WAVEFORMS
	2.0	min.	typ.	max.	min.	max.	min.	max.			
tPHL/	propagation delay CP to Q _n		16	30		38		45	ns	4.5	Fig. 6
^t PHL	propagation delay MR to Q _n		23	34		43		51	ns	4.5	Fig. 708km
t _{THL} / t _{TLH}	output transition time		7	15		19	6 2	22	ns	4.5	Fig. 6
tW	clock pulse width HIGH or LOW	16	9	00	20		24	60	ns	4.5	Fig. 6
tW	master reset pulse width LOW	16	8	81	20		24	12	ns	4.5	Fig. 7
^t rem	removal time MR to CP	10	-2	63 55 63	13	03 100 00	15 5-	80 60 60	ns	4.5	Fig. 7
t _{su}	set-up time D _n to CP	12	5	4.1	15 8	4	18 8.0	8.0 8	ns	4.5	Fig. 8
th	hold time D _n to CP	3	-4	12	3		3	35	ns	4.5	Fig. 8
f _{max}	maximum clock pulse frequency	30	56		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

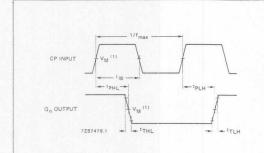


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width output transition times and the maximum clock pulse frequency.

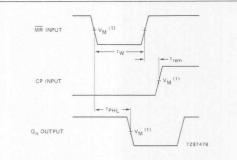


Fig. 7 Waveforms showing the master reset (\overline{MR}) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

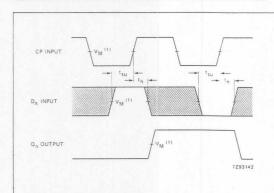


Fig. 8 Waveforms showing the data set-up and hold times for the data input (D_n) .

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

AC WAVEFORMS

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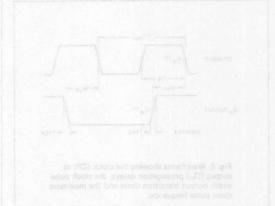






Fig. 8 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig. 8

The sheded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms (1) HC: $V_{RR} = SUS; V_{I} = GND$ to $V_{RR} = V_{I} + V_{I} = GND$ to

9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

FEATURES

- Word-length easily expanded by cascading
- Similar pin configuration to the "180" for easy system up-grading
- Generates either odd or even parity for nine data bits
- Output capability: standard
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT280 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT280 are 9-bit parity generators or checkers commonly used to detect errors in high-speed data transmission or data retrieval systems. Both even and odd parity outputs are available for generating or checking even or odd parity up to 9 bits.

The even parity output (Σ_E) is HIGH when an even number of data inputs (I $_0$ to I $_8$) are HIGH. The odd parity output (Σ_0) is HIGH when an odd number of data inputs are HIGH.

Expansion to larger word sizes is accomplished by tying the even outputs (Σ_E) of up to nine parallel devices to the data inputs of the final stage. For a single-chip 16-bit even/odd parity generator/checker, see PC74HC/HCT7080.

APPLICATIONS

- 25-line parity generator/checker
- 81-line parity generator/checker

0)////001	DARAMETER	CONDITIONS	TYF	LINIT	
SYMBOL PARAMETER	PARAMETER	CONDITIONS	нс	нст	UNIT
tPHL/	propagation delay In to Σ E In to Σ O	C _L = 15 pF V _{CC} = 5 V	17 20	18 22	ns ns
C _I	input capacitance		3.5	3.5	pF
C _{PD} www.	power dissipation capacitance per package	notes 1 and 2	65	65	pF

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

f; = input frequency in MHz CL

IHz CL = output load capacitance in pF
MHz VCC = supply voltage in V

 f_0 = output frequency in MHz $\Sigma (C_L \times V_{CC}^2 \times f_0)$ = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

TOT THE CONDITION IS VI - GIVE to VCC -

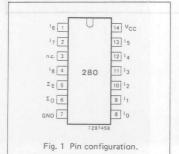
PACKAGE OUTLINES

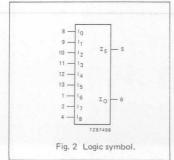
14-lead DIL; plastic (SOT27).

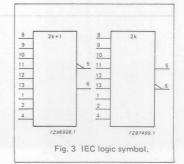
14-lead mini-pack; plastic (SO14; SOT108A).

PIN DESCRIPTION

PIN NO.	SYMBOL		NAME AND FUNCTION	
8, 9, 10, 11, 12, 13, 1, 2, 4 5, 6	l ₀ to l ₈ Σ _E , Σ _O		data inputs	
7	GND		ground (0 V)	
14	Vcc	-	positive supply voltage	







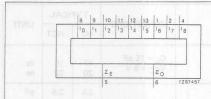
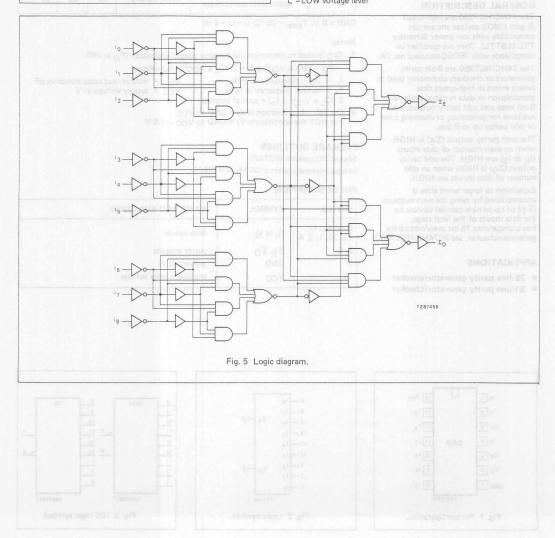


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS	OUTPUTS					
number of HIGH data inputs (I ₀ to I ₈)	ΣΕ	Σο				
even	Н	nicLs7				

H = HIGH voltage level L =LOW voltage level



DC CHARACTERISTICS FOR 74HC

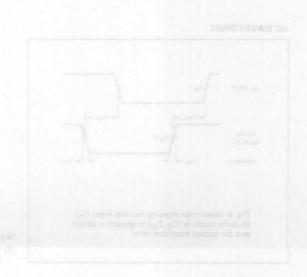
For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

					T _{amb} (°C)					TEST CONDITIONS		
0)/44001	74HC		INPUT COEFFICE										
SYMBOL	PARAMETER		+25		-401	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.					
tPHL/ tPLH	propagation delay $I_{\rm n}$ to $\Sigma_{\rm E}$		55 20 16	200 40 34		250 50 43		300 60 51	ns _{To}	2.0 4.5 6.0	Fig. 6		
t _{PHL} /MO	propagation delay I_n to Σ_O		63 23 18	200 40 34	(at)	250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6		
tTHL/ tTLH	output transition time	25	19 7 6	75 15 13	o to hi	95 19 16	as o ou	110 22 19	ns	2.0 4.5 6.0	Fig. 6		



DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
l _n	1.0

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	PARAMETER		00			T _{amb} (°C)				TEST CONDITIONS		
SYMBOL			74HCT 46 81						UNIT	V	OG OT ALL		
			011+25			-40 to +85 -40		-40 t	-40 to +125		V _{CC}	WAVEFORMS	
			min.	typ.	max.	min.	max.	min.	max.			HT, ontone stability	
tPHL/ tPLH	propagation de I_n to Σ_E	lay		21	42		53		63	ns	4.5	Fig. 6	
tPHL/ tPLH	propagation de I_n to Σ_O	lay		26	45		56		68	ns	4.5	Fig. 6	
tTHL/ tTLH	output transition	on time		7	15		19		22	ns	4.5	Fig. 6	

AC WAVEFORMS

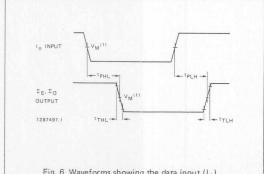
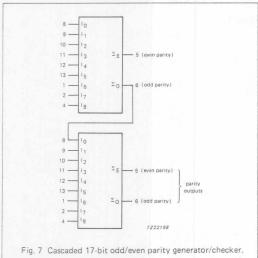


Fig. 6 Waveforms showing the data input (In) to parity outputs (Σ_E, Σ_O) propagation delays and the output transition time.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 V$; $V_I = GND$ to 3 V.

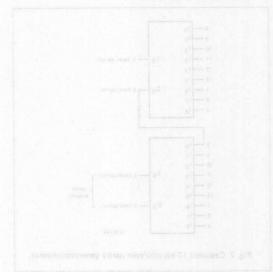
APPLICATION INFORMATION



Note to Fig. 7

For a single-chip 16-bit even/odd parity generator/checker, see PC74HC/HCT7080.

APPLICATION INFORMATION



Note to Fig. 7

For a single-only 16-bit even/odd parity generator/checker,

4-BIT BINARY FULL ADDER WITH FAST CARRY

FEATURES

- · High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal look-ahead carry
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT283 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT283 add two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the sum outputs (Σ_1 to Σ_4) and the out-going carry (C_{OUT}) according to the equation:

$$C_{1N} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) =$$

Where (+) = plus.

$$= \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Due to the symmetry of the binary add function, the "283" can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic); see function table. In case of all active LOW operands the results \$\Sigma_1\$ to \$\Sigma_4\$ and \$\Commongy T\$ should be interpreted also as active LOW. With active HIGH inputs, \$\Cinc_1 N\$ must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus \$\Cinc_1 N\$, \$A_1\$, \$B_1\$ can be assigned arbitrarily to pins \$\Sigma_6.7\$, etc.

See the "583" for the BCD version.

		20101710110	TYF	LINIT	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
^t PHL [/] ^t PLH	propagation delay CIN to Σ_1 CIN to Σ_2 CIN to Σ_3 CIN to Σ_3 CIN to Σ_4 An or Bn to Σ_n CIN to COUT	C _L = 15 pF V _{CC} = 5 V	16 18 20 23 21 20 20	15 21 23 27 25 23 24	ns ns ns ns ns ns
Ci	input capacitance		3,5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	88	92	pF

GND = 0 V;
$$T_{amb} = 25 \,^{\circ}\text{C}$$
; $t_r = t_f = 6 \,\text{ns}$

Motes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

$$PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

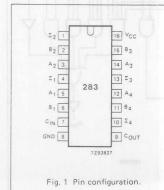
PACKAGE OUTLINES

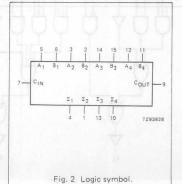
16-lead DIL; plastic (SOT38Z).

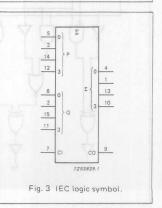
16-lead mini-pack; plastic (SO16; SOT109A).

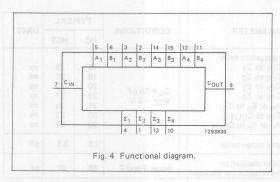
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 1, 13, 10	Σ_1 to Σ_4	sum outputs
5, 3, 14, 12	A ₁ to A ₄	A operand inputs
6, 2, 15, 11	B ₁ to B ₄	B operand inputs
7	CIN	carry input
8	GND	ground (0 V)
9	COUT	carry output
16	Vcc	positive supply voltage









FUNCTION TABLE

PINS	CIN	A ₁	A ₂	А3	A ₄	В1	B ₂	В3	В4	Σ1	Σ2	Σ3	Σ4	COUT	EXAMPLE
logic levels	L	L	Н	L	Н	Н	L	L	Н	Н	Н	L	L	Н	82)+
active HIGH	0	0	11110	0	13	1	0	0	1	1	1	0	0	1	(a) 10081 +
active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(b)

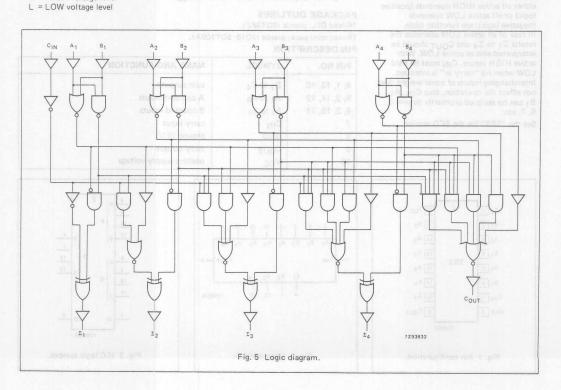
H = HIGH voltage level

1010 10011 (a) for active HIGH,

Example 1001

example = (9 + 10 = 19) (b) for active LOW,

(b) for active LOW, example = (carry + 6 + 5 = 12)



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

					Tamb	(°C)				Т	EST CONDIT	TIONS
					74H	С						
SYMBOL	PARAMETER		+25		-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/	propagation delay C_{1N} to Σ_1		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6	84, Aa. Ag, Bg
tPHL/ tPLH	propagation delay C_{1N} to Σ_2		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 6	
tPHL/ tPLH	propagation delay C _{IN} to Σ ₃	u	63 23 18	195 39 33	(0) Ta	245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6	JOSMY
tPHL/ tPLH	propagation delay C _{1N} to Σ ₄	.30	74 27 22	230 46 39	sami	290 58 49	xém .	345 69 59	ns	2.0 4.5 6.0	Fig. 6	
tPHL/	propagation delay $A_{n} \text{ or } B_{n} \text{ to } \Sigma_{n}$	20	69 25 20	210 42 36	39	265 53 45	16	315 63 54	ns	2.0 4.5 6.0	Fig. 6	VINS FLIS
tPHL/	propagation delay	an	63 23 18	195 39 33	58	245 49 42	-84	295 59 50	ns	2.0 4.5 6.0	Fig. 6	ATH SHD
tPHL/ tPLH	propagation delay A _n or B _n to COUT	2/5	63 23 18	195 39 33	88	245 49 42	88	295 59 50	ns	2.0 4.5 6.0	Fig. 6	H116
tTHL/ tTLH	output transition time	en .	19 7 6	75 15 13	19	95 19 16	49	110 22 19	ns	2.0 4.5 6.0	Fig. 6	834 71H4

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications",

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
CIN	1.50
B ₂ , A ₂ , A ₁	1.00
B ₁	0.40
B ₄ , A ₄ , A ₃ , B ₃	0.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V} \cdot t_{-} = t_{4} = 6 \text{ ps} \cdot C_{1} = 50 \text{ pF}$

	2.0				T _{amb}	(°C)	207	0.0		Т	EST CONDITIONS	3
SYMBOL PARAMETER	4.5 Fig. 6	74HCT 25 25							UNIT	Velst	WAVEFORMS	
	- Attameten	+25			-40	-40 to +85 -40 to +1			UNIT	V _{CC}		
	4.5 Fig. 6	min.	typ.	max.	min.	max.	min.	max.		Visial		
tPHL/ tPLH	propagation delay C_{IN} to Σ_{1}		18	31	265	39	213	47	ns	4.5	Fig. 6	1989
tPHL/	propagation delay C_{1N} to Σ_2		25	43	ake.	54	38	65	ns	4.5	Fig. 6	HJR
tPHL/	propagation delay C_{1N} to Σ_3	80	27	46	49	58	2	69	ns	4.5	Fig. 6	H.19
tPHL/ tPLH	propagation delay C _{1N} to Σ ₄	alo .	31	53	245 49 49	66	190	80	ns	4.5	Fig. 6	UHS
tphl/ tplh	propagation delay A_n or B_n to Σ_n		29	49	ā@ @#	61	BY T	74	ns	4.5	Fig. 6	VIHT
tPHL/	propagation delay		27	46	81	58		69	ns	4.5	Fig. 6	HJI
tPHL/	propagation delay An or Bn to COUT		28	48		60		72	ns	4.5	Fig. 6	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 6	



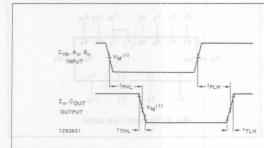


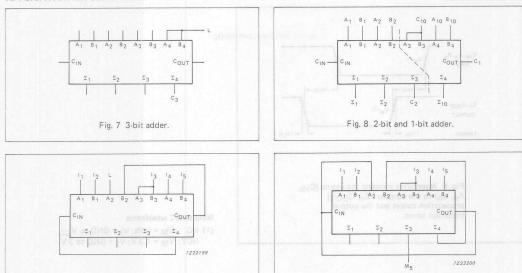
Fig. 6 Waveforms showing the inputs (C_{IN} , A_n , B_n) to the outputs (Σ_n , C_{OUT}) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_1 = GND$ to V_{CC} . HCT: $V_M = 1.3$ V; $V_1 = GND$ to 3 V.

Fig. 10 5-input majority gate.

APPLICATION INFORMATION



Note to Figs 7 to 10

Fig. 9 5-input encoder.

Figure 7 shows a 3-bit adder using the "283". Tying the operand inputs of the fourth adder (A_3 , B_3) LOW makes Σ_3 dependent on, and equal to, the carry from the third adder. Based on the same principle, Figure 8 shows a method of dividing the "283" into a 2-bit and 1-bit adder. The third stage adder (A_2 , B_2 , Σ_2) is used simply as means of transfering the carry into the fourth stage (via A_2 and B_2) and transfering the carry from the second stage on Σ_2 . Note that as long as A_2 and B_2 are the same, HIGH or LOW, they do not influence Σ_2 . Similary, when A_2 and B_2 are the same, the carry into the third stage does not influence the carry out of the third stage. Figure 9 shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs Σ_0 , Σ_1 and Σ_2 produce a binary number equal to the number inputs (I_1 to I_5) that are HIGH. Figure 10 shows a method of implementing a 5-input majority gate. When three or more inputs (I_1 to I_5) are HIGH, the output M_5 is HIGH.

DIGITAL PHASE-LOCKED-LOOP FILTER

FEATURES

- Digital design avoids analog compensation errors
- Easily cascadable for higher order loops
- Useful frequency range:
 DC to 55 MHz typical (K-clock)
 DC to 35 MHz typical (I/D-clock)
- Dynamically variable bandwidth
- Very narrow bandwidth attainable
- Power-on reset
- Output capability: standard/bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

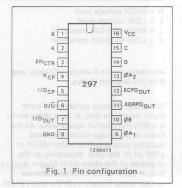
The 74HC/HCT297 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT297 are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. These devices contain all the necessary circuits, with the exception of the divide-by-n counter, to build first order phase-locked-loops.

Both EXCLUSIVE-OR (XORPD) and edgecontrolled (ECPD) phase detectors are provided for maximum flexibility. The input signals for the EXCLUSIVE-OR phase detector must have a 50% duty factor to obtain the maximum lockrange.

Proper partioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation (see Fig. 7) or to cascade to higher order phase-locked-loops.

(continued on next page)



			TYF	UNIT		
SYMBOL	PARAMETER MOTTOMUT GWA IMA	CONDITIONS	НС	нст	MAIA	
tPHL/ tPLH	propagation delay I/DCP to I/DOUT \$\phi A_1, \phi B to XORPDOUT \$\phi B, \phi A_2 to ECPDOUT	C _L = 15 pF	15 13 19	. 18 13 19	ns a	
maximum clock frequency KCP I/DCP		V _{CC} = 5 V	63 41	68 40	MHz	
CI	input capacitance	10.	3.5	3.5	pF	
CPD	power dissipation capacitance per package	notes 1 and 2	18	19	pF ₈	

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

fi = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF

VCC = supply voltage in V

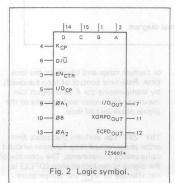
 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

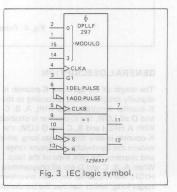
2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} - 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z),

16-lead mini-pack; plastic (SO16L; SOT162A).

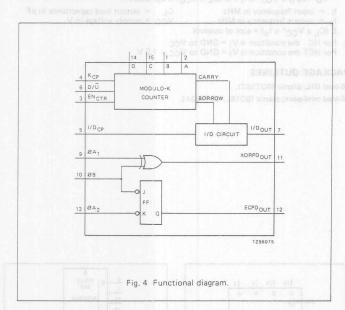




DIGITAL PHASE-LOCKED-LOOP FILTER

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION				
2, 1, 15, 14	A, B, C, D	modulo control inputs				
3 81	ENCTR	K-counter enable input				
4	K _{CP}	K-counter clock input (LOW-to-HIGH, edge-triggered)				
5 3HM 30	I/D _{CP}	increment/decrement clock input (HIGH-to-LOW, edge-triggered)				
6 40 88	D/Ū	down/up control				
7	I/Dout	increment/decrement bus output				
8 74 81	GND	ground (0 V) and somewhere				
9, 10, 13	φΑ1, φΒ, φΑ2	phase inputs				
11	XORPDOUT	EXCLUSIVE-OR phase detector output				
12	ECPDOUT	edge-controlled phase detector output				
6 VCC		positive supply voltage				



GENERAL DESCRIPTION

The length of the up/down K-counter is digitally programmable according to the K-counter function table. With, A, B, C and D all LOW, the K-counter is disabled. With A HIGH and B, C and D LOW, the K-counter is only three stages long, which widens the bandwidth or capture range and shortens the lock time of the loop. When A, B, C and D are all programmed HIGH, the K-counter becomes seventeen stages long, which narrows the bandwidth

or capture range and lengthens the lock time. Real-time control of loop bandwith by manipulating the A to D inputs can maximize the overall performance of the digital phase-locked loop.

The "297" can perform the classic first-order phase-locked-loop function without using analog components. The accuracy of the digital phase-locked-loop (DPLL) is not affected by V_{CC} and temperature variations but depends solely on

K-COUNTER (DIGITAL CONTROL) FUNCTION TABLE

D	С	В	А	MODULO (K)
(algelo) O-glaci du dat		L H H	LHLH	inhibited 2³ 2⁴ 2⁵
L L L	TITI	LLHH	LHLH	2 ⁶ 2 ⁷ 2 ⁸ 2 ⁹
Н Н Н		L H H	L H L	2 ¹⁰ 2 ¹¹ 2 ¹² 2 ¹³
н н н	TITI	LLHH	L H L	2 ¹⁴ 2 ¹⁵ 2 ¹⁶ 2 ¹⁷

EXCLUSIVE-OR PHASE DETECTOR FUNCTION TABLE

ORPDOUT
Both EXCL
be Houngo
provided for
ingut signal

EDGE-CONTROLLED PHASE DETECTOR TABLE

φ A ₂	φВ	ECPDOUT
H or L	↓	H
↓	H or L	L
H or L	↑	no change
↑	H or L	no change

H = HIGH voltage level

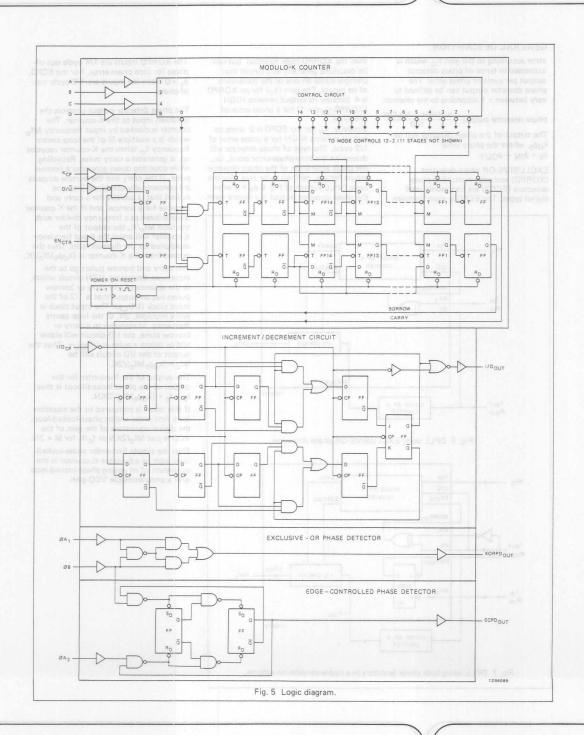
L = LOW voltage level

↓ = HIGH-to-LOW transition

↑ = LOW-to-HIGH transition

accuracies of the K-clock, I/D-clock and loop propagation delays.

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty factor square wave. At the limits of linear operation, the phase detector output will be either HIGH or LOW all of the time depending on the direction of the phase error $(\phi_{\parallel N} - \phi_{OUT})$. Within these limits the phase detector output varies linearly with the input phase



GENERAL DESCRIPTION

error according to the gain k_d , which is expressed in terms of phase detector output per cycle or phase error. The phase detector output can be defined to vary between \pm 1 according to the relation:

phase detector output = $\frac{\% \text{ HIGH} - \% \text{ LOW}}{100}$

The output of the phase detector will be $k_d\phi_e$, where the phase error ϕ_e = $\phi_{\rm IN}$ - $\phi_{\rm OUT}$.

EXCLUSIVE-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex

than the XORPD logic function but can be described generally as a circuit that changes states on one of the transitions of its inputs. The gain (k_d) for an XORPD is 4 because its output remains HIGH (XORPDOUT = 1) for a phase error of 1/4 cycle.

Similarly, k_d for the ECPD is 2 since its output remains HIGH for a phase error of 1/2 cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for a ϕ_e defined to be zero. For the basic DPLL system of Fig. 6 ϕ_e = 0 when the phase detector output is a square wave.

The XORPD inputs are 1/4 cycle out-of-phase for zero phase error. For the ECPD, $\phi_{\rm e}=0$ when the inputs are 1/2 cycle out-of-phase.

The phase detector output controls the up/down input to the K-counter. The counter is clocked by input frequency Mfc, which is a multiple M of the loop centre frequency fc. When the K-counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and the borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K-counter is considered as a frequency divider with the ratio Mf_C/K, the output of the K-counter will equal the input frequency multiplied by the division ratio. Thus the output from the K-counter is $(k_d \phi_e Mf_c)/K$. The carry and borrow pulses go to the

The carry and borrow pulses go to the increment/decrement (I/D) circuit which, in the absence of any carry or borrow pulses has an output that is 1/2 of the input clock (I/Dcp). The input clock is just a multiple, 2N, of the loop centre frequency. In response to a carry or borrow pulse, the I/D circuit will either add or delete a pulse at I/D_{OUT}. Thus the output of the I/D circuit will be $Nf_C + (k_d \phi_e Mf_C)/2K$.

The output of the N-counter (or the output of the phase-locked-loop) is thus: $f_O = f_C + (k_d \phi_e M f_c)/2KN$.

If this result is compared to the equation for a first-order analog phase-locked-loop, the digital equivalent of the gain of the VCO is just $Mf_c/2KN$ or f_c/K for M=2N.

Thus the simple first-order phase-locked-loop with an adjustable K-counter is the equivalent of an analog phase-locked-loop with a programmable VCO gain.

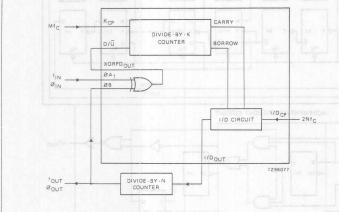


Fig. 6 DPLL using EXCLUSIVE-OR phase detection.

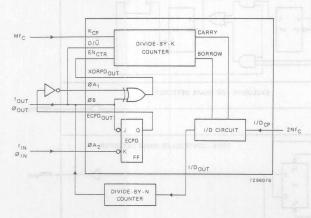


Fig. 7 DPLL using both phase detectors in a ripple-cancelation scheme.

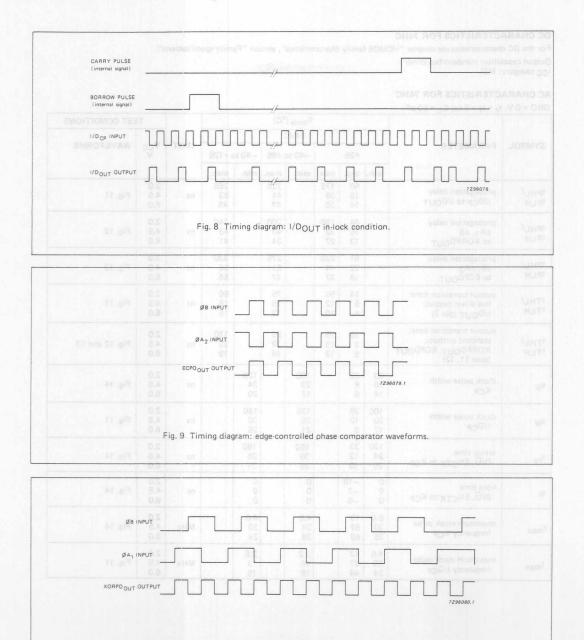


Fig. 10 Timing diagram: EXCLUSIVE-OR phase detector waveforms.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard/bus driver

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V} \cdot t_r = t_f = 6 \text{ ns} \cdot C_1 = 50 \text{ nF}$

SYMBOL	PARAMETER	T _{amb} (°C)								TEST CONDITIONS	
					74H	0	1111	101		n.F	TURNIN (60V)
		+25			-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.	П	П	1997UO 700 CO
tPHL/ tPLH	propagation delay		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 11
tPHL/	propagation delay φA ₁ , φB to XORPD _{OUT}	nomb	44 16 13	160 32 27	U00/I	200 40 34	ib gnie	240 48 41	ns	2.0 4.5 6.0	Fig. 12
tPHL/	propagation delay øB, øA ₂ to ECPD _{OUT}		61 22 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 13
tTHL/ tTLH	output transition time: bus driver output; I/D _{OUT} (pin 7)		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 11
tTHL/ tTLH	output transition time: standard outputs; XORPDOUT, ECPDOUT (pins 11, 12)		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 12 and 13
tW	clock pulse width	80 16 14	22 8 6		100- 20 17		120 24 20	USTUD A	ns	2.0 4.5 6.0	Fig. 14
tW	clock pulse width	100 20 17	28 10 8	esc do	125 25 21		150 30 26	anis eni	ns	2.0 4.5 6.0	Fig. 11
t _{su}	set-up time D/U, ENCTR to KCP	120 24 20	33 12 10		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 14
th	hold time D/U, ENCTR to KCP	0 0 0	-19 -7 -6		0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 14
f _{max}	maximum clock pulse frequency KCP	6.0 30 35	19 57 68		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 14
f _{max}	maximum clock pulse frequency I/DCP	4.0 20 24	12 37 44		3.2 16 19		2.6 13 15		MHz	2.0 4.5 6.0	Fig. 11

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard/bus driver

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
ENCTR, D/Ū	0.3
A, B, C, D, K _{CP} , φA ₂	0.6
I/D _{CP} , φA ₁ , φB	1.5

AC CHARACTERISTICS FOR 74HCT

					Tamb	(°C)				T	EST CONDITIONS
		210		1	74H	ICT			UNIT	1/00	WAVEFORMS
SYMBOL	PARAMETER		+25		-40 t	o +85	-40 to	+125	UNIT	VCC	WAVEFORING
		min.	typ.	max.	min.	max.	min.	max.		-5	
tPHL/	propagation delay		21	35		44		53	ns	4.5	Fig. 11
tPHL/	propagation delay ϕA_1 , ϕB to XORPDOUT		16	32		40	T	48	ns	4.5	Fig. 12
tPHL/	propagation delay φB, φA ₂ to ECPD _{OUT}		22	44	lar soll	55	4.	66	ns	4.5	Fig. 13
tTHL/ tTLH	output transition time bus driver output I/D _{OUT} (pin 7)		5	12		15	sessio (T)	18	X) ragra		Fig. 11
tTHL/ tTLH	output transition time standard outputs XORPDOUT, ECPDOUT (pins 11, 12)		7	15		19	EJ NAS	22	ns	4.5	Figs 12 and 13
tw	clock pulse width KCP	16	8		20		24		ns	4.5	Fig. 14
tw	clock pulse width	25	13		31		38		ns	4.5	Fig. 11
t _{su}	set-up time D/Ū, ENCTR to KCP	24	13		30		36		ns	4.5	Fig. 14
th	hold time D/Ū, EN _{CTR} to K _{CP}	0	-8		0		0		ns	4.5	Fig. 14
fmax	maximum clock pulse frequency KCP	30	62	À	24	1	20		MHz	4.5	Fig. 14
fmax	maximum clock pulse frequency I/DCP	20	36		16		13	*	MHz	4.5	Fig. 11

AC WAVEFORMS

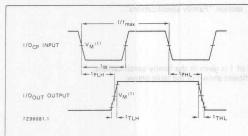


Fig. 11 Waveforms showing the clock (I/Dcp) to output (I/DOUT) propagation delays, the clock pulse width, output transition times and maximum clock pulse frequency.

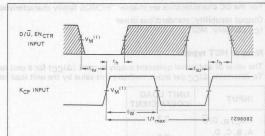


Fig. 14 Waveforms showing the clock (KCP) pulse width and the maximum clock pulse as agolu frequency, and the input (D/U, ENCTR) to clock (KCP) set-up and hold times.

Note to Fig. 14

The shaded areas indicate when the input is permitted to change for predictable output performance.

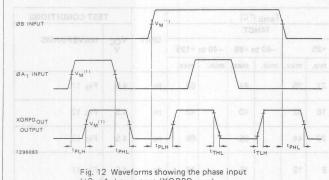
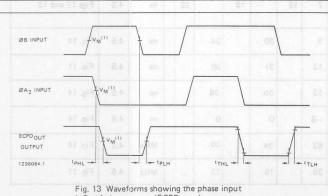


Fig. 12 Waveforms showing the phase input $(\phi B, \phi A_1)$ to output (XORPDOUT) propagation delays and output transition times.



(φB, φA₂) to output (ECPDOUT) propagation delays and output transition times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 V$; $V_I = GND$ to 3 V.

8-BIT UNIVERSAL SHIFT REGISTER: 3-STATE

GENERAL DESCRIPTI SARUTAS

- Multiplexed inputs/outputs provide improved bit density
- Four operating modes: shift left shift right hold (store) load data
- Operates with output enable or at high-impedance OFF-state (Z)
- 3-state outputs drive bus lines directly
- Can be cascaded for n-bits word length
- Output capability: bus driver (parallel I/Os) standard (serial outputs)
- Icc category: MSI

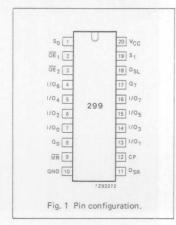
GENERAL DESCRIPTION

The 74HC/HCT299 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT299 contain eight edgetriggered D-type flip-flops and the interstage logic necessary to perform synchronous shift-right, shift-left, parallel load and hold operations. The type of operation is determined by the mode select inputs (So and S1), as shown in the mode select table.

All flip-flop outputs have 3-state buffers to separate these outputs (I/O₀ to I/O₇) such, that they can serve as data inputs in the parallel load mode. The serial outputs (Q₀ and Q₇) are used for expansion in serial shifting of longer words.

(continued on next page)



		CONDITIONS	TYF	PICAL	IO N
SYMBOL	PARAMETER MOTTOMUST GMA 3M	CONDITIONS	НС	нст	UNIT
tPHL/WO_I	propagation delay CP to Q ₀ , Q ₇ CP to I/O _n	C _L = 15 pF	20 20	19 19	ns ns
^t PHL	\overline{MR} to Q_0 , Q_7 or I/Q_0	(PU)	20	23	ns NS (8
f _{max}	maximum clock frequency	1726	50	46	MHz
CI	input capacitance	sens	3.5	3.5	pF
C1/O	input/output capacitance	selo	10	10	pF.
C _{PD}	power dissipation capacitance per package	notes 1 and 2	120	125	pF ^{OS}

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

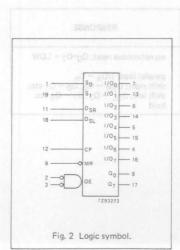
1. CPD is used to determine the dynamic power dissipation (PD in μ W):

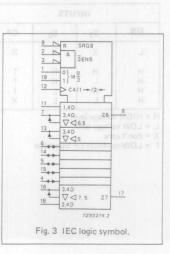
$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is VI = GND to VCC
- For HCT the condition is $V_1 = GND$ to $V_{CC} 1.5 V$

PACKAGE OUTLINES

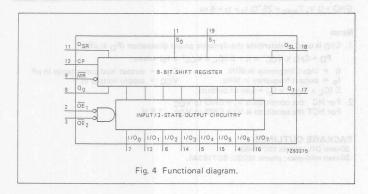
- 20-lead DIL; plastic (SOT146).
- 20-lead mini-pack; plastic (SO20; SOT163A).





PIN DESCRIPTION

PIN NO.	HCT	SYMBOL	NAME AND FUNCTION
1, 19		S ₀ , S ₁	mode select inputs
2, 3		OE ₁ , OE ₂	3-state output enable inputs (active LOW)
7, 13, 6, 5, 15, 4,		1/0 ₀ to 1/0 ₇	parallel data inputs or 3-state parallel outputs (bus driver)
8, 17		Q ₀ , Q ₇	serial outputs (standard output)
9		MR	asynchronous master reset input (active LOW)
10		GND	ground (0 V)
1179		DSR	serial data shift-right input
12		CP	clock input (LOW-to-HIGH, edge-triggered)
18		DSL	serial data shift-left input
20		Vcc	positive supply voltage



MODE SELECT TABLE

	INP	UTS		RESPONSE		
MR	S ₁	s ₀	СР	RESPONSE		
L	X	X	X	asynchronous reset; Q_0 - Q_7 = LOW		
H H H	H L H	H H L	† † *	parallel load; I/O _n \rightarrow Q _n shift right; D _{SR} \rightarrow Q ₀ , Q ₀ \rightarrow Q ₁ etc. shift left; D _{SL} \rightarrow Q ₇ , Q ₇ \rightarrow Q ₆ etc. hold		

H = HIGH voltage level

L = LOW voltage level

X = don't care

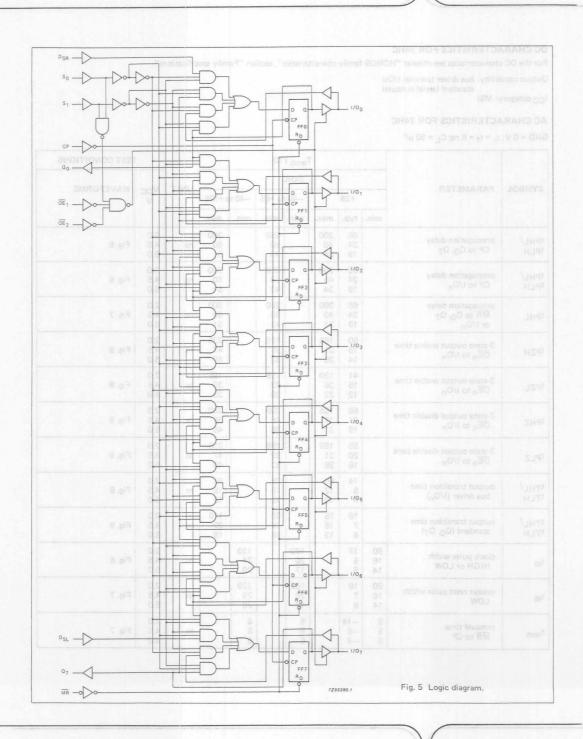
↑ = LOW-to-HIGH CP transition

GENERAL DESCRIPTION

A LOW signal on the asynchronous master reset input (\overline{MR}) overrides the S_n and clock (CP) inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock pulse. Inputs can change when the clock is either state, provided that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on the 3-state output enable inputs (\overline{OE}_1 or \overline{OE}_2) disables the 3-state buffers and the I/ O_n outputs are set to the high-impedance OFF-state. In this condition, the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 , when in preparation for a parallel load operation.





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver (parallel I/Os) standard (serial outputs)

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)		HO			TEST CONDITIONS
CVMDOI	DADAMETER			P	74H			LC			WAVEFORMS
SYMBOL	PARAMETER		+25	PI	-40	to +85	-40 t	o +125	UNIT	VCC	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			5
t _{PHL} /	propagation delay CP to Q ₀ , Q ₇		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t _{PHL} /	propagation delay CP to I/O _n		66 24 19	200 40 34	0 0+ 10 0 CHI	250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
^t PHL	propagation delay MR to Ω ₀ , Ω ₇ or I/O _n		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 7
^t PZH	3-state output enable time OE _n to I/O _n		50 18 14	155 31 26	0 0	195 39 33		235 47 40	ns	2:.0 4.5 6.0	Fig. 9
^t PZL	3-state output enable time OE _n to I/O _n		41 15 12	130 26 22	100	165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig. 9
^t PHZ	3-state output disable time OE _n to I/O _n		66 24 19	185 37 31	0 0	230 46 39	Œ	280 56 48	ns	2.0 4.5 6.0	Fig. 9
^t PLZ	3-state output disable time $\overline{\text{OE}}_{\text{n}}$ to I/O _n		55 20 16	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 9
^t THL/ ^t TLH	output transition time bus driver (I/O _n)		14 5 4	60 12 10	0 0	75 15 13	CE.	90 18 15	ns	2.0 4.5 6.0	Fig. 6
t _{THL} /	output transition time standard (Q ₀ , Q ₇)		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
tw	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t _W	master reset pulse width LOW	80 16 14	19 7 6		100 20 17		120 24 20	-0	ns	2.0 4.5 6.0	Fig. 7
^t rem	removal time MR to CP	5 5 5	-14 -5 -4	D-1	5 5 5	H	5 5 5	FE	ns	2.0 4.5 6.0	Fig. 7

AC CHARACTERISTICS FOR 74HC (Cont'd)

						T _{amb} (°C)			74		TEST CONDI	TIONS
	TEST CONDIT		1			74H0	Tar						
SYMBOL	PARAMETER			+25 —40 to		-40 to +85 -40 to +125		UNIT	VCC V	WAVEFOR	MS		
	3010121011		min.	typ.	max.	min.	max.	min.	max.				
t _{su}	set-up time DSR, DSL to	СР	100 20 17	33 12 10	71 .20	125 25 21	m 200	150 30 26	g "mim	ns	2.0 4.5 6.0	Fig. 6	\jieq!
t _{su}	set-up time S ₀ , S ₁ to CP	G.A 21	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8	PTH4: HT4:
t _{su}	set-up time I/O _n to CP	ns 4,5	125 25 21	39 14 11		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 6	THE
th	hold time I/O _n , D _{SR} , D _S to CP	d.a - an	0 0	-14 -5 -4		0 0 0		0 0		ns	2.0 4.5 6.0	Fig. 6	724 /HZ4
t _h	hold time S ₀ , S ₁ to CP	8.5 8.5 8.5	0 0	-28 -10 -8		0 0		0 0	2	ns	2.0 4.5 6.0	Fig. 8	275
f _{max}	maximum clock frequency	pulse	5.0 25 29	15 45 54		4.0 20 24		3.4 17 20		MHz	2.0 4.5 6.0	Fig. 6	VAT

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver (parallel I/Os) standard (serial outputs)

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT	4.5
I/O _n DSR, DSL CP, S ₀	0.25 0.25 0.60	4,6
MR, S ₁	0.25 0.30	45

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)	Hau-				TEST CONDITIONS
SYMBOL	PARAMETER	125			74HC	Т			UNIT	N	WAVEFORMS
STIVIBUL	PARAMETER	,881	+25	ien Jau	-40	to +85	-40 t	o +125	UNII	V _{CC}	WAVEFORMS
	2.0	min.	typ.	max.	min.	max.	min.	max.			anis much
t _{PHL} /	propagation delay CP to Ω ₀ , Q ₇		22	37		46		56	ns	4.5	Fig. 6
t _{PHL} /	propagation delay CP to I/O _n		22	37		46		56	ns	4.5	Fig. 6
^t PHL	propagation delay MR to Ω ₀ , Ω ₇ or I/O _n		27	46	a	58		69	ns	4.5	Fig. 7
tPZH/ tPZL	$\frac{3\text{-state output enable time}}{\overline{\text{OE}}_n \text{ to I/O}_n}$		19	30		38	14	45	ns	4.5	Fig. 9
[†] PHZ	3-state output disable time OE _n to I/O _n		24	37		46	28	56	ns	4.5	Fig. 9
^t PLZ	3-state output disable time OE _n to I/O _n		20	32		40	01	48	ns	4.5	Fig. 9
t _{THL} / t _{TLH}	output transition time bus driver (I/O _n)		5	12		15		18	ns	4.5	Fig. 6
t _{THL} / t _{TLH}	output transition time standard (Q ₀ , Q ₇)		7	15		19		22	ns	4.5	Fig. 6
tw	clock pulse width HIGH or LOW	20	10	паюв	25	Tel 157361	30	108 fam	ns	4.5	Fig. 6
tw	master reset pulse width LOW	20	11		25		30		ns	4.5	Fig. 7 milidenea yours
^t rem	removal time MR to CP	10	2		9		11		ns	4.5	Fig. 7 ISM synoperso 2
t _{su}	set-up time I/O _n , D _{SR} , D _{SL} to CP	25	14	de ai f lant she	31	Jinu s bšol v	38	(A) toer vd solet	ns	4.5	Fig. 6
t _{su}	set-up time S ₀ , S ₁ to CP	32	18		40		48		ns	4.5	Fig. 8
^t h	hold time I/O _n , D _{SR} , D _{SL} to CP	0	-11		0		0		ns	4.5	Fig. 6 85.0 180 480
^t h	hold time S ₀ , S ₁ to CP	0	-17		0		0		ns	4.5	Fig. 8
f _{max}	maximum clock pulse frequency	25	42		20		17		MHz	4.5	Fig. 6

AC WAVEFORMS

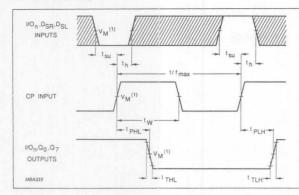


Fig. 6 Waveforms showing the clock (CP) to output (I/O $_{n}$, O_{0} , O_{7}) propagation delays, the clock pulse width, the I/O_{n} , D_{SR} and D_{SL} to CP set-up and hold times, the output transition times and the maximum clock frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

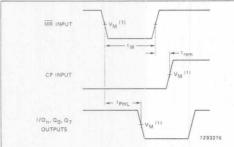


Fig. 7 Waveforms showing the master reset (\overline{MR}) pulse width (LOW), the master reset to output (I/O_n, Q₀, Q₇) propagation delays and the master reset to clock (CP) removal time.

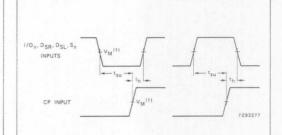


Fig. 8 Waveforms showing the set-up and hold times from the mode control inputs $(S_0,\,S_1)$ to the clock (CP).

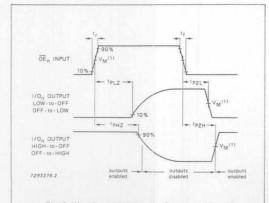


Fig. 9 Waveforms showing the 3-state enable and disable times for $\overline{\text{OE}}_n$ inputs.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

AC WAVEFORMS

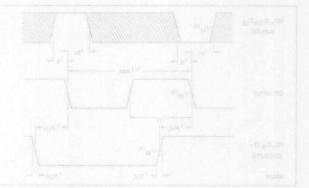
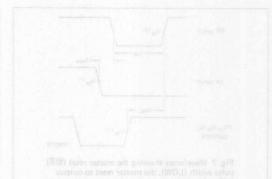


Fig. 6 Wevstorms showing the clock (CP) to output (I/ $\Omega_{\rm p}$, $\Omega_{\rm p}$, 0.7) propersion delays, the clock puts width, the I/ $\Omega_{\rm p}$, $\Omega_{\rm p}$ and $\Omega_{\rm SL}$ to CP set-up and hold times, the output transition times and the maximum clock frequency.

Note to Fig. 6

Its shaded areas indicate when the input is amnifted to change for predictable output artformance.



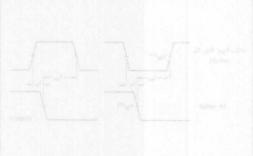


Fig. 8 Waveforms showing the set-up and hold dimes from the mode control inputs $(S_0,\,S_1)$ to the clock (CP).

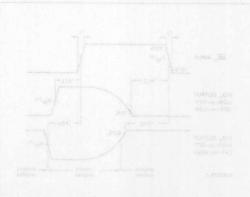


Fig. 9. Waveforms showing the 3-state enable and disable times for \overline{OE}_n inputs.

to AC waveforms () Fig. : $V_M = 50\% \ V_1 = 60\% \ \text{to } V_C$ HCT: $V_M = 1.5\% \ V_1 = 60\% \ \text{to } 0$

8-INPUT MULTIPLEXER/REGISTER WITH TRANSPARENT LATCHES; 3-STATE

FEATURES

- Transparent data latches
- Transparent address latch
- Easily expanding
- Complementary outputs
- · Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT354 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT354 data selectors/ multiplexers contain full on-chip binary decoding, to select one-of-eight data sources. The data select address is stored in transparent latches that are enabled by a LOW on the latch enable input (LE).

The transparent 8-bit data latches are enabled when the active LOW data enable input (Ē) is LOW. When the output enable input $\overline{OE}_1 = HIGH, \overline{OE}_2 = HIGH \text{ or }$ OE3 = LOW, the outputs go to the high impedance OFF-state. Operation of these output enable inputs does not affect the state of the latches.

CVMDOL	PARAMETER	CONDITIONS	TYPICAL		LINIT
SYMBOL	PARAMETER US ONA SM	CONDITIONS	НС	нст	ns ns
t _{PHL} /	propagation delay D _n , E to Y, Y S _n , LE to Y, Y	C _L = 15 pF V _{CC} = 5 V	20 24	22 27	
CI (WO.	input capacitance	Kin I I I I	3.5	3.5	pF
C _{PD}	power dissipation capacitance per latch	notes 1 and 2	68	71	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes HELL SHOULD TO A SIGNARY STATES 1. CPD is used to determine the dynamic power dissipation (PD in μ W):

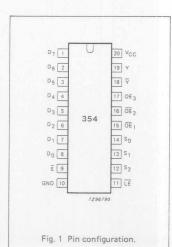
PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

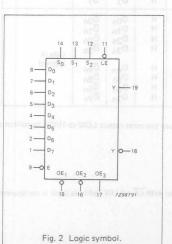
- f; = input frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V
- f_0 = output frequency in MHz
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is VI = GND to VCC For HCT the condition is $V_I = GND$ to VCC - 1.5 V

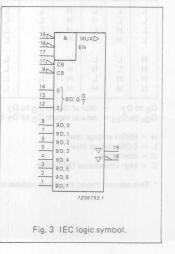
PACKAGE OUTLINES

20-lead DIL; plastic (SOT146).

20-lead mini-pack; plastic (SO20; SOT163A).







PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1 9 10	D ₀ to D ₇ E GND LE	data inputs data enable input (active LOW) ground (0 V) address latch enable input (active LOW)
14, 13, 12 15, 16	S_0, S_1, S_2 $\overline{OE}_1, \overline{OE}_2$	select inputs normalize prevent output enable inputs (active LOW)
17 18 19	OE ₃ ∀	output enable input (active HIGH) 3-state multiplexer output (active LOW) 3-state multiplexer output (active HIGH)
20	V _{CC} 10 noiseaze	positive supply voltage

FUNCTION TABLE TO VIOLET TO SOLVE

		OUT	of GND	Vec	UTS	INP			
DESCRIPTION	nounund	= [A 80	ABLE	PUT EN	OUT		s *	DRES	AD
ACKAGE OUT	₹ _{31/11}	Υ	OE ₃	OE ₂	ŌĒ ₁	Ē	s ₀	S ₁	S ₂
outputs in high impedance OFF-state	Z Z Z	Z Z Z	X X L	X H X	H X X	X X X	X X X	X X X	X X X
data latch is	D 0 D 1 D 2 D 3	D ₀ D ₁ D ₂ D ₃	H H H	L L L	L L L	L L L	L H L	L H H	L L L
transparent	□4 □5 □6 □7	D ₄ D ₅ D ₆ D ₇	H H H	L L L	L L L	L L L	L H L H	L H H	HHHH
data is	D̄ _{0n} D̄ _{1n} D̄ _{2n} D̄ _{3n}	D _{0n} D _{1n} D _{2n} D _{3n}	Н Н Н	L L L		H H H	L H L	L H H	L L L
latched	D _{4n} D _{5n} D _{6n} D _{7n}	D4n D5n D6n D7n	H H H	L L L		H H H	L H L	L H H	H H H

 D_0 to D_7 = data at inputs D_0 to D_7

 D_{0n} to D_{7n} = data at inputs D_0 to D_7 before the most recent LOW-to-HIGH transition of E

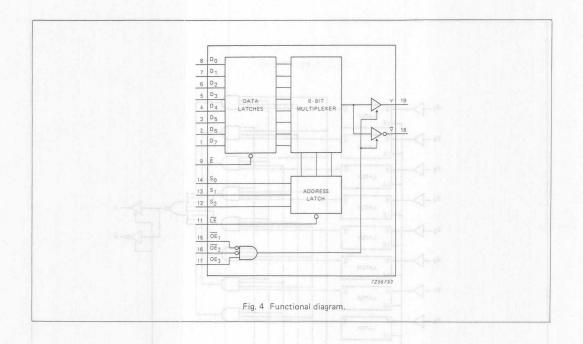
H = HIGH voltage level

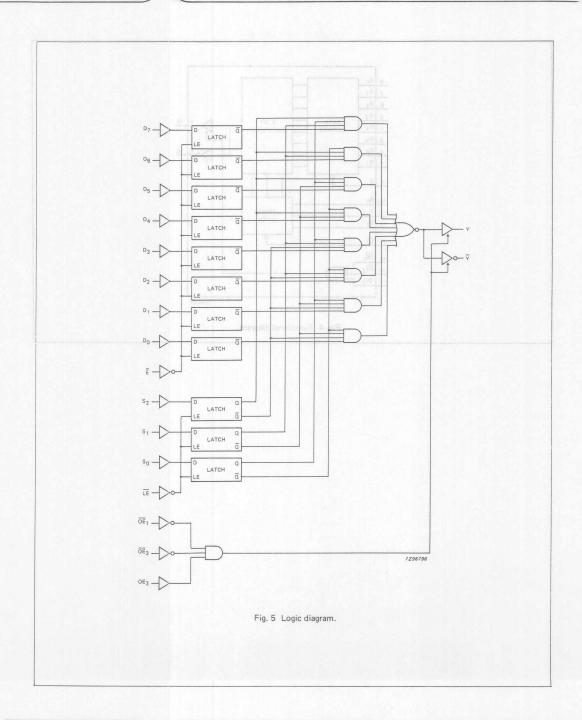
L = LOW voltage level

X = don't care

Z = high impedance OFF-state

* This column shows the input address set-up with \overline{LE} = LOW (address latch is transparent).





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC XEM Mim XEM Mim XEM QVI Mim

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

					T _{amb} (°C)	2-	8		TEST CONDITIONS		
	2.0		1	3	74H	С	8-	8	UNIT		WAVEFORMS	
SYMBOL	PARAMETER 4		+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay D _n to Y, \overline{Y}	ly spei	61 22 18	210 42 36	"esim	265 53 45	nisy ch	315 63 54	ns On an	2.0 4.5 6.0	Fig. 7	
t _{PHL} /	propagation delay E to Y, \overline{Y}		63 23 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 6 IBM VIDOUED	
t _{PHL} /	propagation delay losus yillos S _n to Y, \overline{Y}		77 28 22	260 52 44	i asol iiteoa	325 65 55	ui (ogi u adi y	390 78 66	ns vicio	2.0 4.5 6.0	Fig. 8	
t _{PHL} /	propagation delay LE to Y, Y		77 28 22	290 58 49		365 73 62		435 87 74	ns	2.0 4.5 6.0	Fig. 9 300	
t _{PZH} /	3-state output enable time $\overline{\text{OE}}_{n}$ to Y, $\overline{\text{Y}}$		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 12 a.g.	
tPZH/ tPZL	3-state output enable time OE $_3$ to Y, \overline{Y}		44 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 12	
t _{PHZ} /	3-state output disable time $\overline{\text{OE}}_{n}$ to Y, $\overline{\text{Y}}$		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 12	
^t PHZ [/] ^t PLZ	3-state output disable time OE3 to Y, \overline{Y}		55 20 16	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 12	
tTHL/ tTLH	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 7, 8 and 9	
tw	data enable pulse width \overline{E} LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6	
tw	latch enable pulse width LE LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9	
t _{su}	set-up time D _n to E	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10	
t _{su}	set-up time S _n to LE	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10	

		of topics yill		noitage	T _{amb} (°C)		et acout		ato yea	TEST CONDITIONS
0.4440.01	DADAMETER				74H	С			UNIT	Vcc	WAVEFORMS
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	ONT	V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		107 a	
	hold time	5	-6		5		5		719 (2.0	an 8 = y = 21V 0 = 0M
th axo	D _n to E	5	-2 -2		5	aT	5		ns	4.5 6.0	Fig. 11
t _h	hold time S _n to LE	5 5 5	-8 -3 -2	- 281	5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 10 9 308.648

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver SI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT UNIT LOA						
D _n , S _n 0.2 OE ₃ 0.25 LE 0.5 0.5 E, OE _n 1.0	2.0 4.5 6.0					
Fig. 12	2.0 4.5 6.0					
Fig. 12						

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)				٦	TEST CONDITIONS
CVMPOL	DADAMETER				74HC	т			UNIT		WAVEFORMS
SYMBOL	PARAMETER	pro-	+25		-40	to +85	-40 t	0 +125	UNIT	V _{CC}	WAVEFORING
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/	propagation delay D_n to Y, \overline{Y}		25	47		59	\	71	ns	4.5	Fig. 7
^t PHL/ ^t PLH	propagation delay E to Y, Y		26	54		68		81	ns	4.5	Fig. 6
tphL/	propagation delay S_n to Y, \overline{Y}	1	30	59		74	1	89	ns	4.5	Fig. 8
t _{PHL} /	propagation delay		31	63		79		95	ns	4.5	Fig. 9
^t PZH [/] -	3-state output enable time OEn to Y, Y		18	34		43	I	51	ns	4.5	Fig. 12
^t PZH/ ^t PZL	3-state output enable time OE ₃ to Y, \overline{Y}		18	34		43	dL	51	ns _{Har}	4.5	Fig. 12
t _{PHZ} /	3-state output disable time \overline{OE}_n to Y, \overline{Y}		18	33		41	Car.	50	ns	4.5	Fig. 12
tPHZ/ no	3-state output disable time OE_3 to Y, \overline{Y}	oitset	21	39		49	ti nolta	59	ns	4.5	Fig. 12
t _{THL} /	output transition time		5	12		15		18	ns	4.5	Figs 7, 8 and 9
tw	data enable pulse width E LOW	16	6		20		24		ns	4.5	Fig. 6
tw	latch enable pulse width LE LOW	16	6		20		24		ns	4.5	Fig. 9
t _{su}	set-up time D _n to E	10	4		13		15		ns	4.5	Fig. 11
^t su	set-up time S _n to LE	10	5	16 (82)	13		15		ns	4.5	Fig. 10
^t h	hold time D _n to E	9	0		11		14	H-16.10 ² -4	ns	4.5	Fig. 11
^t h	hold time S _n to LE	9	-3	96 Y	11		14		ns	4.5	Fig. 10

AC WAVEFORMS

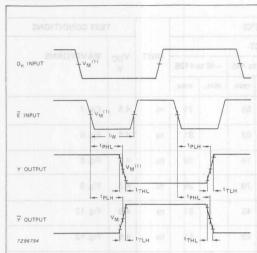


Fig. 6 Waveforms showing the data enable input (\overline{E}) pulse width, the data enable to output (Y,\overline{Y}) propagation delays and the output transition times.

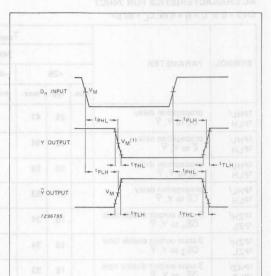


Fig. 7 Waveforms showing the data input (D_n) to output (Y, \overline{Y}) propagation delays and the output transition times $(\overline{E}$ = LOW).

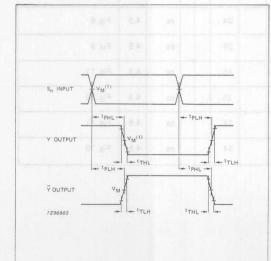


Fig. 8 Waveforms showing the select input (S_n) to output (Y,\overline{Y}) propagation delays and the output transition times $(\overline{LE}=LOW).$

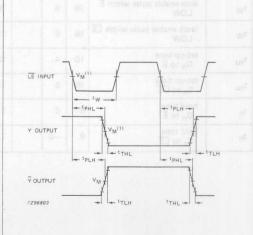


Fig. 9 Waveforms showing the address latch enable input (\overline{LE}) pulse width, the address latch enable input to output (Y, \overline{Y}) propagation delays and the output transition times.

AC WAVEFORMS (Cont'd)

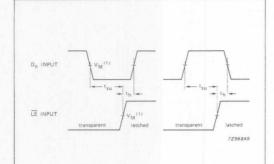


Fig. 10 Waveforms showing the set-up and hold times for the select input (S_n) to the address latch enable input $(\overline{LE}).$

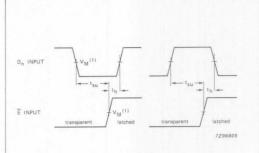


Fig. 11 Waveforms showing the set-up and hold times for the data input (D_n) to the data enable input (\overline{E}).

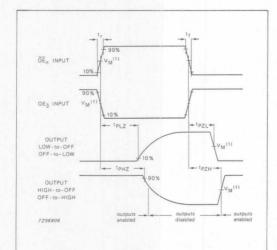
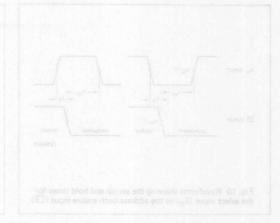


Fig. 12 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

AC WAVEFORMS (Control)



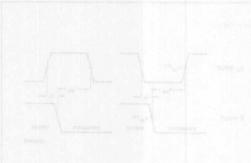
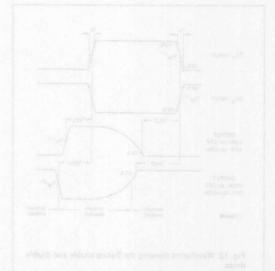


Fig. 11. Washforms showing the setup and hold times for the data input $\{D_n\}$ to the data enable input $\{B\}$.



(t) HCT: V_M = 60%: V_I = 6ND to V_{CC} HCT: V_M = 1.3 V; V_I = 6ND to 3 V.

8-INPUT MULTIPLEXER/REGISTER; 3-STATE

FEATURES

- Non-transparent data latches
- Transparent address latch
- Easily expanding
- Complementary outputs
- Output capability: bus driver
- I_{CC} category: MS1

GENERAL DESCRIPTION

The 74HC/HCT356 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT356 data selectors/ multiplexers contain full on-chip binary decoding, to select one-of-eight data sources. The data select address is stored in transparent latches that are enabled by a LOW on the latch enable input LE.

Data on the 8 input lines (D₀ to D₇) is clocked into a edge-triggered data register by a LOW-to-HIGH transition of the clock (CP).

When the output enable input \overline{OE}_1 = HIGH, \overline{OE}_2 = HIGH or OE3 = LOW, the outputs go to the high impedance OFF-state.

Operation of these output enable inputs does not affect the state of the latches and register.

01/14001	DADAMETED	CONDITIONS	TYP	UNIT	
SYMBOL	PARAMETER MOLTOMUR DIVA RM	TER CONDITIONS		нст	
^t PHL [/]	propagation delay S _n , LE to Y, \overline{Y} CP to Y, \overline{Y}	C _L = 15 pF	24 20	25 22	ns ns
CI	input capacitance (V 0) bm	ang S	3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	123	125	pF

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

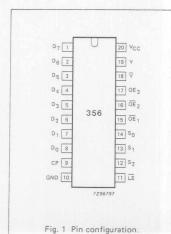
Notes

- 1. CPD is used to determine the dynamic power dissipation (P_D in μW):
 - $PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$ where: f; = input frequency in MHz CL = output load capacitance in pF
 - f_0 = output frequency in MHz
 - VCC = supply voltage in V
 - $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is VI = GND to VCC
- For HCT the condition is $V_1 = GND$ to VCC 1.5 V

PACKAGE OUTLINES

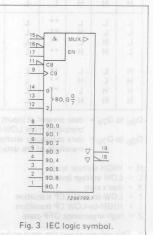
20-lead DIL; plastic (SOT146).

20-lead mini-pack; plastic (SO20; SOT163A).









PIN	DE	CO	DI	DTI	ON

SYMBOL	NAME AND FUNCTION
D ₀ to D ₇	data inputs Yeles not apequiq
CP	clock input data (LOW-to-HIGH, edge-triggered)
GND	ground (0 V) sanstiesces tueni
LE	address latch enable input (active LOW)
So, S1, S2	select inputs a sea sensitioness.
OE ₁ , OE ₂	output enable inputs (active LOW)
OE ₃	output enable input (active HIGH)
7	3-state multiplexer output (active LOW)
Y	3-state multiplexer output (active HIGH)
Vcc	positive supply voltage
	D ₀ to D ₇ CP GND LE S ₀ , S ₁ , S ₂ OE ₁ , OE ₂

FUNCTION TABLE

			INF	PUTS	1 - 50 A	OND TO	OUT	PUTS	For HQT the d
AD	DDRES	SS *		OUT	PUT EN	ABLE			DESCRIPTION
s ₂	s ₁	s ₀	СР	ŌĒ ₁	ŌE ₂	OE ₃	Υ	SANIA	PACKAGE OUT
X X X	X X X	X X X	X X X	H X X	X H X	X X L	Z Z Z	Z Z Z Z	outputs in high impedance OFF-state
L L L	L H H	L H L	† † †	L L L	L L L	H H H	D _{0n} D _{1n} D _{2n} D _{3n}	D0n D1n D2n D3n	data is clocked
H H H	L H H	L H L	† † †	L L L	L L L	H H H	D _{4n} D _{5n} D _{6n} D _{7n}	D4n D5n D6n D7n	into latch
L L L	L H H	L H L H	** ** **		L L L	H H H	D _{0p} D _{1p} D _{2p} D _{3p}	DOp D1p D2p D3p	outputs do not
H H H	L H H	L H L	**	L L L	L L L	H H H	D _{4p} D _{5p} D _{6p} D _{7p}	D _{4p} D _{5p} D _{6p} D _{7p}	change states

 D_{0n} to D_{7n} = data present at inputs D_0 to D_7 when the data latch clock made the transition from LOW-to-HIGH

D_{Op} to D_{7p} = data previously latched into the data latch by the LOW-to-HIGH transition of the data latch clock

H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH CP transition

↓ = HIGH-to-LOW CP transition

Z = high impedance OFF-state

* This column shows the input address set-up with $\overline{LE} = LOW$ (address latch is transparent).

** CP is HIGH, LOW or \.

8-INPUT MULTIPLEXER/REGISTER; 3-STATE

· Non-transparent data latches

Transparent address latch

Complementary outputs

Ourput capability: bus drive

ICO category: NISI

GENERAL DESCRIPTION

Si-gate CMOS devices and are pin ...

TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 76HC/HCT356 data selectors/ nultiplexers contain full on-chip binary

sources. The data select address is stored in transparent latches that are enabled by

a LOW on the latter enable input LE.

Data on the 8 input lines (D₀ to D₇)

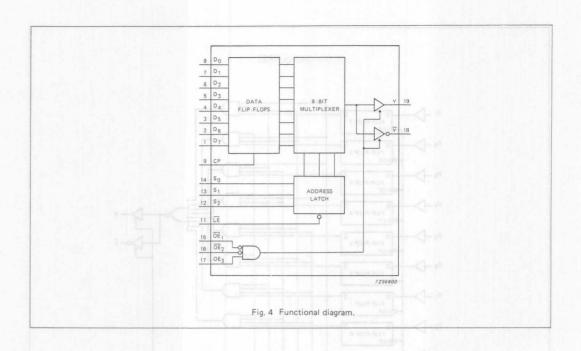
register by a LOW-re-HIGH transition of the clock (CP).

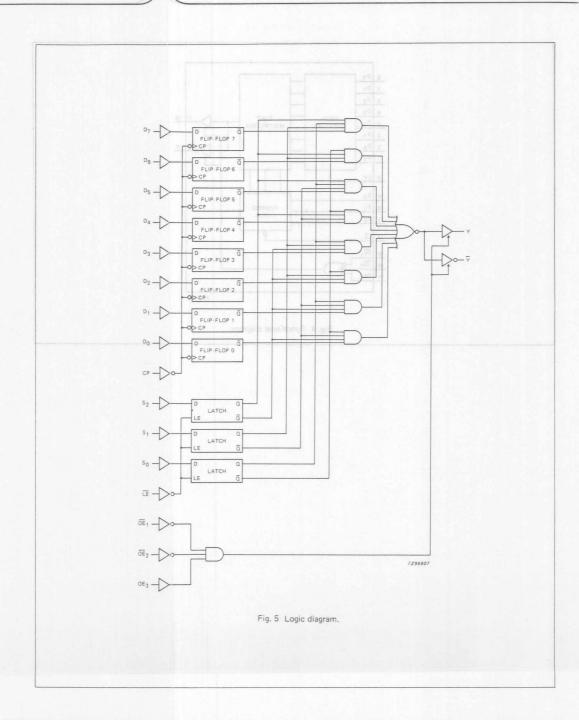
 OE_2 = HIGH, OE_2 = HIGH or OE_3 = LOW, the outputs go to the high

Operation of these output anable inputs
does not affect the state of the latenes

nod register.

Dy I W Vcc





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC at and of moving at 1 to beef they a not 1001A1 memory plugge measure functions to sultay and

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF 100 and moved the bull section and yet substituting the first section $t_r = 100$ pc.

					T _{amb} (°C)				TEST CONDITIONS		
01/140.01					74H	С					WAN/EEGENG	
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			15 0,5 55 ₀ , 0P 1.0	
^t PHL/	propagation delay CP to Y, \overline{Y}		66 24 19	240 48 41		300 60 51		360 72 61	ns Ag	2.0 4.5 6.0	Fig. 6	
tPHL/	propagation delay S_n to Y, \overline{Y}		77 28 22	260 52 44	P) dei	325 65 55		390 78 66	ns	2.0 4.5 6.0	Fig. 7	
^t PHL [/]	propagation delay LE to Y, Y	+125 max.	77 28 22	270 54 46	as Oil-	340 68 58	25+	405 81 69	ns	2.0 4.5 6.0	Fig. 8	
t _{PZH} /	3-state output enable time $\overline{\text{OE}}_n$ to Y, $\overline{\text{Y}}$	77	41 15 12	125 25 21		155 31 26	85	190 38 32	ns	2.0 4.5 6.0	Fig. 11	
t _{PZH} /	3-state output enable time OE_3 to Y, \overrightarrow{Y}	98	47 17 14	150 30 26		190 38 33	28	225 45 38	ns	2.0 4.5 6.0	Fig. 11	
^t PHZ [/]	3-state output disable time $\overline{\text{OE}}_n$ to Y, $\overline{\text{Y}}$	18	50 18 14	155 31 26		195 39 33	50	235 47 40	ns	2.0 4.5 6.0	Fig. 11	
^t PHZ [/]	3-state output disable time OE ₃ to Y, ₹	ta	58 21 17	155 31 26		195 39 33	81	235 47 40	ns	2.0 4.5 6.0	Fig. 11	
^t THL/ ^t TLH	output transition time	50	14 5 4	60 12 10		75 15 13	20	90 18 15	ns	2.0 4.5 6.0	Figs 6, 7 and 8	
t _W 8 :	clock pulse width CP	80 16 14	17 6 5	ā	100 20 17	2	120 24 20		ns	2.0 4.5 6.0	Fig. 6	
tW	latch enable pulse width LE LOW	80 16 14	17 6 5		100 20 17		120 24 20	at	ns	2.0 4.5 6.0	Fig. 8	
su	set-up time D _n to CP	50 10 9	11 4 3		65 13 11		75 15 13	Dr.	ns	2.0 4.5 6.0	Fig. 10	
su	set-up time S _n to LE	50 10 9	14 5 4		65 13 11		75 15 13	at	ns	2.0 4.5 6.0	Fig. 9	
h	hold time D _n to CP	5 5 5	-6 -2 -2		5 5 5		5 5 5	ē	ns	2.0 4.5 6.0	Fig. 10	
^t h	hold time S _n to LE	5 5 5	-8 -3 -2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 9	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. The supply current ($\triangle I_{CC}$) for a unit load coefficient shown in the table below.

INPUT	UNIT LOA							
D C 0								
D _n , S _n 2M OE3 <u>LE</u> OE _n , CP	0.2 0.25	25V						
OE _n , CP	0.5 1.0							

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

314D O V,	tr = tf = 6 lis, CL = 50 pr	18		11			1 61				11 01 10	H-FT
		ORE		125	T _{amb} (°C) oas				ve lab	EST CONDITIO	NS
SYMBOL	PARAMETER	80		85	74HC	T 41	22		UNIT	Vcc	WAVEFORMS	
STINDOL	2.0	405	+25	0#8 R/	-40	to +85	-40 t	+125	01111	V	propagation	
		min.	typ.	max.	min.	max.	min.	max.			,Y ot Bu	HJ9
t _{PHL} /	propagation delay CP to Y, Y	38 38 32	26	51 13		64 83	15 12	77	ns si	4.5	Fig. 6	
t _{PHL} /	propagation delay S _n to Y, \(\overline{Y}\)	225	28	59 08		74 08	ta 71	89	ns smu sk	4.5	Fig. 7	/HZ9
t _{PHL} /	propagation delay LE to Y, Y	38	29	63		79 88	14 50	95	ns	4.5	Fig. 8	724
t _{PZH} /	3-state output enable time \overline{OE}_n to Y, \overline{Y}	4.7 40	17	34		43	18	51	ns	4.5	Fig. 110	ZTB
t _{PZH} /	3-state output enable time OE ₃ to Y, \overline{Y}	235	18	34		43	38	51	ns 3 etc	4.5	Fig. 11= 8	ZH6 /ZH6
tPHZ/ tPLZ	$\frac{3\text{-state output disable time}}{OE_n \text{ to Y}, \overline{Y}}$	08	17	33		41 0	14	50	ns	4.5	Fig. 11	Liser
tPHZ/	3-state output disable time OE_3 to Y, \overline{Y}	15	20	33	no	41 0	5	50	ns	4.5	Fig. 11	HJT
tTHL/ tTLH	output transition time		5	12	20	15	9	18	ns	4.5	Figs 6, 7 and 8	W
tw	clock pulse width CP HIGH or LOW	16	8 05		20		24	80	ns	4.5	Fig. 6	W
tw	latch enable pulse width LE LOW	16	6		20		24	14	ns	4.5	Fig. 8	
t _{su}	set-up time D _n to CP	10	4 8		13		15	6	ns	4.5	Fig. 10	115
t _{su}	set-up time S _n to LE	10	5 8		13		15	10	ns	4.5	Fig. 9	112
^t h	hold time D _n to CP	5	0		5		5 8	8	ns	4.5	Fig. 10	
th	hold time S _n to LE	5	-2		5		5	8	ns	4.5	Fig. 9	
	ns 4,6 Fig. 9				1		E-	8			PINIDIOIDIT I	- 1

AC WAVEFORMS

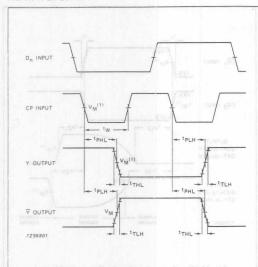
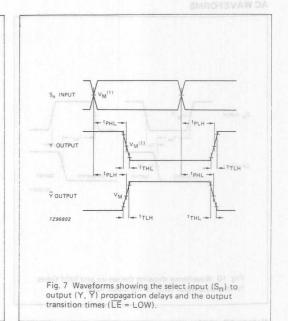


Fig. 6 Waveforms showing the clock (CP) to the output (Y,\overline{Y}) propagation delays, the clock pulse width and the output transition times.



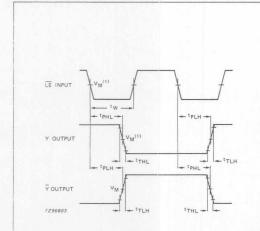


Fig. 8. Waveforms showing the address latch enable input (\overline{LE}) pulse width, the latch enable input to output (Y,\overline{Y}) propagation delays and the output transition times.

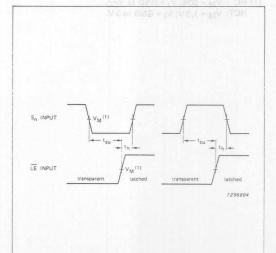
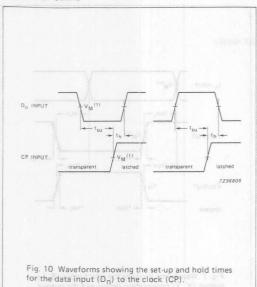
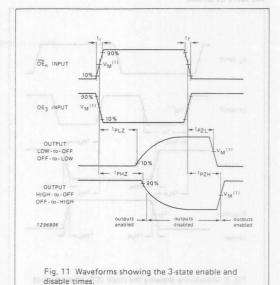


Fig. 9 Waveforms showing the set-up and hold times for the select input (S $_n)$ to the address latch enable input ($\overline{LE}).$

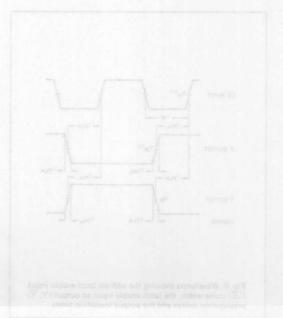
AC WAVEFORMS





Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3$ V; $V_I = GND$ to 3 V.



HEX BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Non-inverting outputs
- Output capability: bus driver
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT365 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT365 are hex non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs $(\overline{OE}_1, \overline{OE}_2)$.

A HIGH on $\overline{\text{OE}}_n$ causes the outputs to assume a high impedance OFF-state.

The "365" is identical to the "366" but has non-inverting outputs.

TOAT NOT			TYF	LINIT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
tPHL/	propagation delay nA to nY	C _L = 15 pF V _{CC} = 5 V	9	11	ns
CI	input capacitance		3,5	3,5	pF
CPD	power dissipation capacitance per buffer	notes 1 and 2	40	40	pF

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

- 1. CPD is used to determine the dynamic power dissipation (PD in μ W):
 - PD = CPD \times VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:
 - f; = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

- fo = output frequency in MHz $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{OE}_1, \overline{OE}_2$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	data outputs
8	GND	ground (0 V)
16	Vcc	positive supply voltage

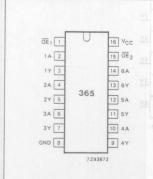
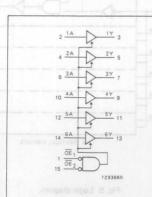
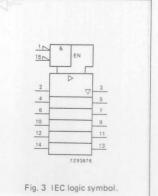


Fig. 1 Pin configuration.





FUNCTION TABLE

	INPUT	S	OUTPUT
OE ₁	OE ₂	nA	nY
L	L	L	L 140
L	L	Н	H
X	Н	X	Z
H	X	X	Z

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

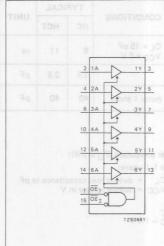
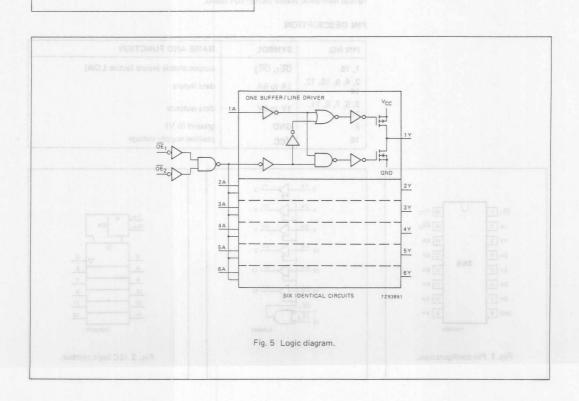


Fig. 4 Functional diagram.



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	Fig. 6						Tamb	(°C)		4.1		TEST CONDITIONS		
	0.40						74H0	;			Yn of An	HTds		
SYMBOL	PARAMET	ER 3.4		E8+25			-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS	
				min.	typ.	max.	min.	max.	min.	max.	emit al		3-state outp	
tPHL/ tPLH	propagation nA to nY		su		30 11 9	95 19 16	15	120 24 20	12	145 29 25	ns	2.0 4.5 6.0	Fig. 6	THE THE
tPZH/ tPZL	3-state outp		e time		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
tPHZ/	3-state outp		e time		61 22 18	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
tTHL/ tTLH	output tran	sition tim	ne		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability : bus driver

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
OE ₁	1.00
OE ₂	0.90
nA	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

					T _{amb}	(°C)		TEST CONDITIONS				
0)/14001		74HCT										
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.	Aq 6		an 8 = 11 = 11 : V 0 = OM.	
tPHL/	propagation delay nA to nY		14	25	(an)	31		38	ns	4.5	Fig. 6	
tPZH/	3-state output enable time OEn to nY	ëst	18	35	84 01 0	44	8	53	ns	4.5	Fig. 7	
t _{PHZ} /	3-state output disable time OEn to nY	.83	23	35	120	44	Se see	53	ns	4.5	Fig. 7	
tTHL/ tTLH	output transition time		5	12	20	15	at . at	18	ns	4.5	Fig. 6	

AC WAVEFORMS

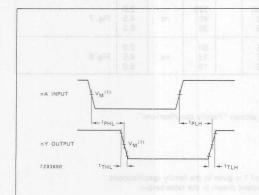


Fig. 6 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

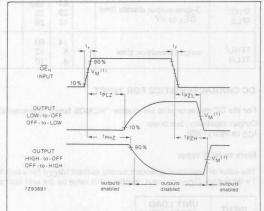


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_1 = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_1 = GND$ to 3 V.

HEX BUFFER/LINE DRIVER; 3-STATE: INVERTING

FEATURES

- Inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT366 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT366 are hex inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs $(\overline{OE}_1, \overline{OE}_2)$.

A HIGH on \overline{OE}_n causes the outputs to assume a high impedance OFF-state. The "366" is identical to the "365" but has inverting outputs.

FUNC			TYF		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
tPHL/	propagation delay nA to nY	C _L = 15 pF V _{CC} = 5 V	10	11	ns
CI	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per buffer	notes 1 and 2	30	30	ρF

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

- f; = input frequency in MHz fo = output frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

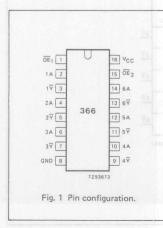
PACKAGE OUTLINES

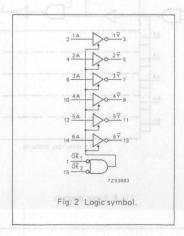
16-lead DIL; plastic (SOT38Z).

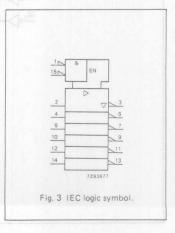
16-lead mini-pack; plastic (SO16; SOT109A).

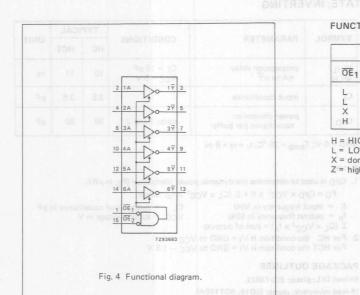
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{\text{OE}}_1$, $\overline{\text{OE}}_2$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1₹ to 6₹	data outputs
8	GND	ground (0 V)
16	Vcc	positive supply voltage









FUNCTION TABLE

	INPUT	owinh at	OUTPUT
	INPUT	OUTPUT	
ŌĒ ₁	OE ₂	nA	nΨ
Ļ	L	L	CT380 are hi
X	H	×	wood Z

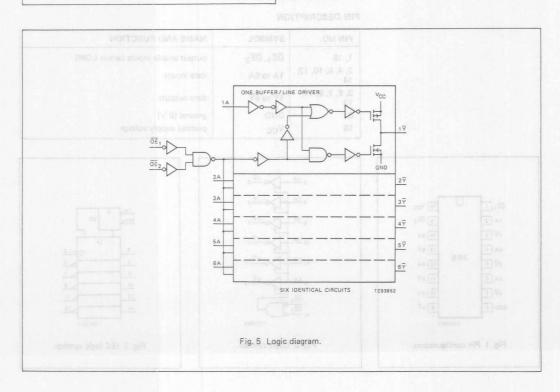
GENERAL

H = HIGH voltage level

L = LOW voltage level 10 X8A 316 88E TOHNOHAY arT

X = don't care

Z = high impedance OFF-state



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T_{amb}	(°C)		TEST CONDITIONS				
					74H0		le de		Yn ar An	FF1.83		
SYMBOL	PARAMETER	+25		-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.	amil s		caus siam-E	
tPHL/	propagation delay nA to nY		33 12 10	100 20 17	18	125 25 21	21	150 30 26	ns	2.0 4.5 6.0	Fig. 6	STAT
tPZH/	3-state output enable time OE _n to nY		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	CVIAV
tPHZ/	3-state output disable time \overrightarrow{OE}_n to \overrightarrow{nY}		55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
tTHL/ tTLH	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

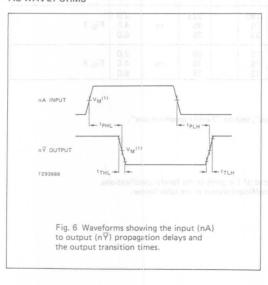
INPUT	UNIT LOAD COEFFICIENT
OE ₁ OE ₂ nA	1.00 0.90 1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; tr = tf = 6 ns; CL = 50 pF offusque ylime 3" nottoge, "entremarante a ylime" 20th -

		T _{amb} (°C)								TEST CONDITIONS		
OVIMBOL	242445752	74HCT										
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	N CC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.	3.0		STREET THE PRO	
tPHL/MOI tPLH	propagation delay nA to nY		13	24	(01)	30		36	ns	4.5	Fig. 6	
tpZH/ 334 tpZL	3-state output enable time OE _n to nY	33	16	35	88+ o	44	d	53	ns	4.5	Fig. 7	
t _{PHZ} /	3-state output disable time OEn to nY	0	20	35	125	44	xam . 001	53 8	ns	4.5	Fig. 7	
t _{THL} /	output transition time		5	12	23	15	17	18	ns	4.5	Fig. 6	

AC WAVEFORMS



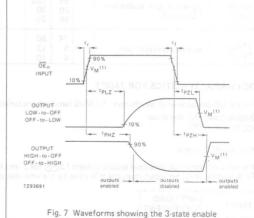


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 V$; $V_I = GND$ to 3 V.

HEX BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Non-inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT367 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL(LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT367 are hex non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs ($1\overline{OE}$, $2\overline{OE}$). A HIGH on $n\overline{OE}$ causes the outputs to

assume a high impedance OFF-state. The "367" is identical to the "368" but has non-inverting outputs.

CVMDOL	DADAMETER	CONDITIONS	TYF	PICAL	118117
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
tPHL/ tPLH	propagation delay nA to nY	C _L = 15 pF V _{CC} = 5 V	8	11	ns
CI	input capacitance	1 1 1	3.5	3.5	pF
CPD	power dissipation capacitance per buffer	notes 1 and 2	30	32	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD
$$\times$$
 VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

- f; = input frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}

 For HCT the condition is V_I = GND to V_{CC} 1.5 V

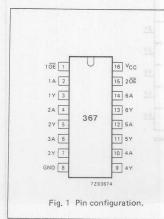
PACKAGE OUTLINES

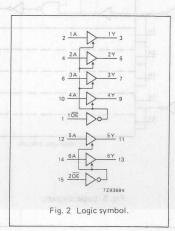
16-lead DIL; plastic (SOT38Z).

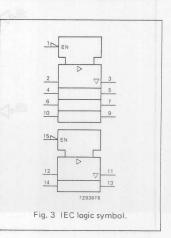
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

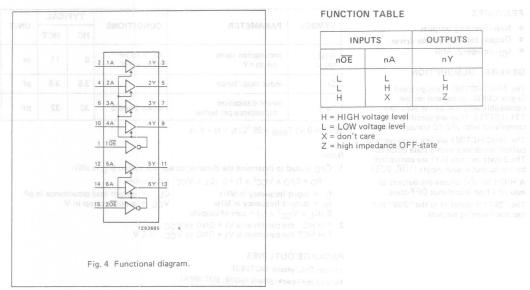
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	10E, 20E	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	data outputs
8	GND	ground (0 V)
16	Vcc	positive supply voltage



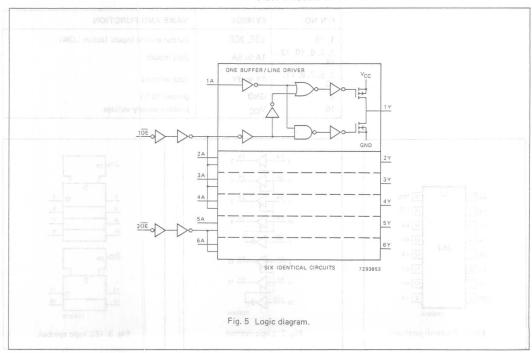




HEA SUPPLIED BRIVER, 3 STATE



IN DESCRIPTION



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_1 = 50 pF$

				T _{amb} (°C)								TEST CONDITIONS		
	Fig. 6			8	8		74H0	2	25				Yn or An	HJP
SYMBOL	PARAMET			3	+25		-40 t	o +85	-40 to	o +125	UNIT	Vcc	WAVEFORMS	
				min.	typ.	max.	min.	max.	min.	max.			and the same of	
tPHL/	propagation nA to nY			8	28 10 8	95 19 16	44	120 24 20	35	145 29 25	ns	2.0 4.5 6.0	Fig. 6	ZJA
tpZH/ tpZL	3-state outp	out enabl	e time		44 16 13	150 30 26	26	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	HUT
^t PHZ/ ^t PLZ	3-state outp		le time		55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
tTHL/ tTLH	output tran	nsition tir	ne		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Output capability: bus driver

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

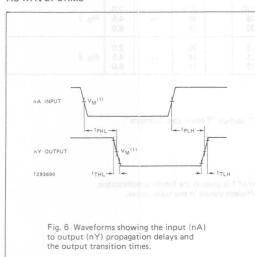
INPUT	UNIT LOAD COEFFICIENT
1 <u>OE</u> 2OE nA	1.00 0.90 1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

					T _{amb}	(°C)				1101	EST CONDITIONS
					74H	т					WANGE O DAMO
SYMBOL	PARAMETER		+25		-40	to + 85	-40	to +125		VCC	
		min.	typ.	max.	min.	max.	min.	max.	349.0		en Branch Company
tPHL/ tPLH	propagation delay nA to nY		14	25	31	31		38	ns	4.5	Fig. 6
tPZH/	3-state output enable time nOE to nY	Su	16	35	8- pt	44	85	53	ns	4.5	Fig. 7
tpHZ/	3-state output disable time	100	¢η .	New .	BIVI .	dm _ ?	m 2	vi j. min			
^t PLZ	nOE to nY	61	21	35	120	44	Bu	53	ns	4.5	Fig. 7
^t THL/ ^t TLH	output transition time		5	12	05.	15	81	18	ns	4.5	Fig. 6

AC WAVEFORMS



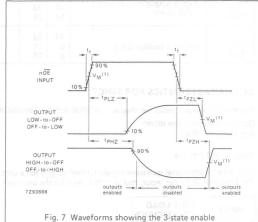


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- Inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT368 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

The 74HC/HCT368 are hex inverting buffer/line drivers with 3-state outputs. The 3-state outputs (\overline{NY}) are controlled by the output enable inputs $(1\overline{OE}, 2\overline{OE})$.

A HIGH on nOE causes the outputs to assume a high impedance OFF-state.

The "368" is identical to the "367" but has inverting outputs.

AUR			TYF	PICAL	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
tPHL/	propagation delay nA to nY	C _L = 15 pF V _{CC} = 5 V	9	11	ns
Cl	input capacitance	TROOP IN	3.5	3.5	pF
CPD	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

f; = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 V$

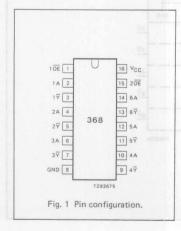
PACKAGE OUTLINES

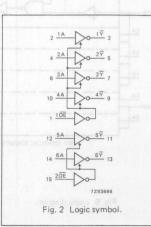
16-lead DIL; plastic (SOT38Z).

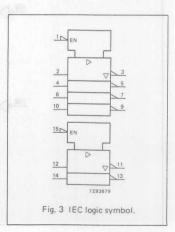
16-lead mini-pack; plastic (SO16; SOT109A).

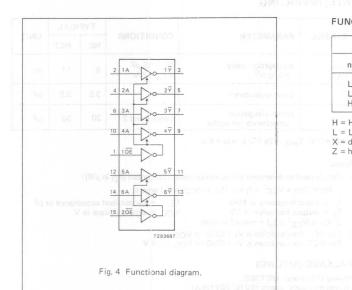
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	10E, 20E	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1₹ to 6₹	data outputs
8	GND	ground (0 V)
16	Vcc	positive supply voltage









FUNCTION TABLE

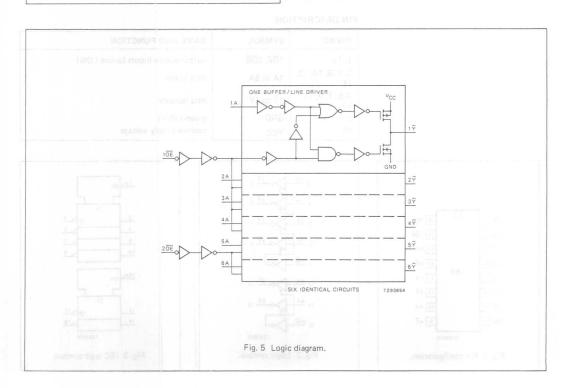
1	INPL	JTS TOTAL	OUTPUTS
	nŌĒ	nA	nΨ
	L L H	L H X	OTTO H 230 J

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb}	(°C)				Т	EST CONDITIONS
SYMBOL	PARAMETER		38		74H		AS	13		Valo	You An Hu
STIVIBUL	TARAMETER an		+25		-40	to +85	-40 t	o +125	UNIT	VCC	WAVEFORMS
	1.8.1	min.	typ.	max.	min.	max.	min.	max.			Yn ot 30n
tPHL/ tPLH	propagation delay nA to nY		30 11 9	95 19 16	2.0	120 24 20	35	145 29 25	ns	2.0 4.5 6.0	Fig. 6
tPZH/ tPZL	3-state output enable time		41 15 12	150 30 26	81	190 38 33	12	225 45 38	ns	2.0 4.5 6.0	Fig. 7
^t PHZ/ ^t PLZ	3-state output disable time nOE to nY		55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
tTHL/ tTLH	output transition time	- 1	14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

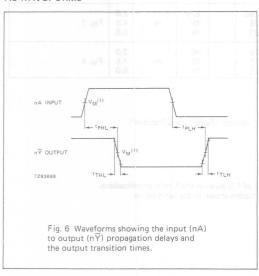
INPUT	UNIT LOAD COEFFICIENT
1 <u>0E</u> 2 <u>0</u> E	1.00
nA	1.00

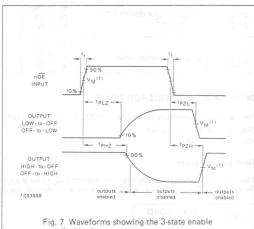
AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

					T_{amb}	(°C)				Т	EST CONDITIONS
01/14001	24244575				74H	СТ					EN TRESTE SE
SYMBOL	PARAMETER		+25		-40 t	o +85	-40 to	o +125	UNIT	VCC	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			Ten il - C - D M
tPHL/ tPLH	propagation delay nA to nY		13	24	(0)	30		36	ns	4.5	Fig. 6
tPZH/ tPZL	3-state output enable time nOE to nY	0	17	35	28+ n	44		53	ns	4.5	Fig. 7
tPHZ/ tPLZ	3-state output disable time nOE to nY		20	35	120	44		53	ns	4.5	Fig. 7
^t THL/ ^t TLH	output transition tirne		5	12	081	15	021	18	ns	4.5	Fig. 6

AC WAVEFORMS





and disable times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to 3 V}$.

OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE

FEATURES

- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the "563", "573" and "533"
- Output capability: bus driver
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT373 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT373 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable (OE) input are common to all latches.

The "373" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the $D_{\rm B}$ inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When \overline{OE} is LOW, the contents of the 8 latches are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches.

The "373" is functionally identical to the "533", "563" and "573", but the "563" and "533" have inverted outputs and the "563" and "573" have a different pin arrangement.

OE 1	U	20 VCC
00 2		19 07
D ₀ 3		18 07
D ₁ 4		17 D ₆
015	373	16 Q ₆
02 6	373	15 Q ₅
027		14 05
038		13 D ₄
03 9		12 Q ₄
GND 10		11 LE
_	7 7 2 9 3 2	150

SYMBOL	DADAMETER	CONDITIONS	TYF	UNIT		
STIVIBUL	PARAMETER	CONDITIONS	НС	нст	UNIT	
tPHL propagation delay D _n to Q _n LE to Q _n		C _L = 15 pF V _{CC} = 5 V	12 15	14 13	ns ns	
CI	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per latch	notes 1 and 2	45	41	pF	

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

f; = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

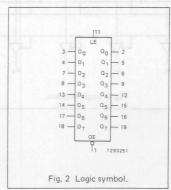
PACKAGE OUTLINES

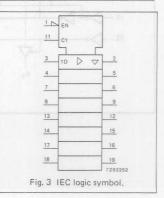
20-lead DIL; plastic (SOT146).

20-lead mini-pack; plastic (SO20; SOT163A).

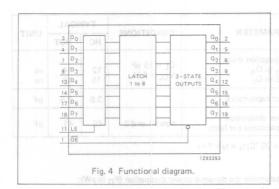
PIN DESCRIPTION

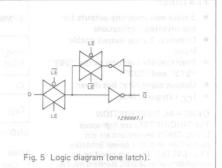
PIN NO.	SYMBOL	NAME AND FUNCTION
1	ŌĒ	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q ₀ to Q ₇	3-state latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D ₀ to D ₇	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	Vcc	positive supply voltage





OCTAL OITYPE TRANSPARENT LATCH SISTATE





FUNCTION TABLE

V ni sgano	- 1	NPUT	S	INTERNAL	OUTPUTS
OPERATING MODES	ŌE	LE	Dn	LATCHES	Q ₀ to Q ₇
enable and read register (transparent mode)	L	H H	L H	L H	H H H
latch and read register	L	L L	l h	.s/Harto	30 T146) suc 14 20; 8
latch register and disable outputs	Н	X	×	X	Z Z

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the

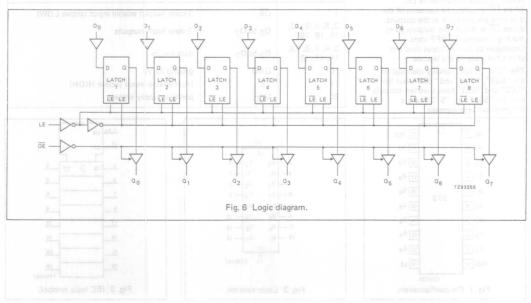
HIGH-to-LOW LE transition ned him in the land

L = LOW voltage level

I = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition

X = don't care

Z = high impedance OFF-state



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)			TEST CONDITIONS			
01/440.01	242445752				74H	0				TIAS	D193300	TUPME
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORM	
		min.	typ.	max.	min.	max.	min.	max.			1,00	30
^t PHL/ ^t PLH	propagation delay D _n to Ω _n		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
tpHL/	propagation delay LE to Ω _n		50 18 14	175 35 30	D Tak	220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8	
^t PZH [/]	3-state output enable time OE to Q _n	126	44 16 13	150 30 26	THUM or Oa	190 38 33	25-	225 45 38	ns	2.0 4.5 6.0	Fig. 9	JOBMYS
^t PHZ/ ^t PLZ	3-state output disable time OE to Q _n	Jan	47 17 14	150 30 26	in in	190 38 33	ray	225 45 38	ns	2.0 4.5 6.0	Fig. 9	Visio
tTHL/ tTLH	output transition time	81	14 5 4	60 12 10	10	75 15 13	8 8	90 18 15	ns	2.0 4.5 6.0	Fig. 7	AHE/
tW	LE pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	
t _{su}	set-up time D _n to LE	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10	Z14 ZH3 ZH3
^t h	hold time D _n to LE	5 5 5	-8 -3 -2	2	5 5 5		5 5 5	31	ns	2.0 4.5 6.0	Fig. 10	HJT

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LO	
Dn	0.30	33.
OE	1.50	

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		1 8			T _{amb} (°C)				TEST CONDITIONS		
01/14001	PARAMETER	82S 08174CHT 061 44 88 74CHT 05 34							UNIT		WAVEFORMS	
SYMBOL	PARAMETER	⁸⁸ +25			-40 to +85		-40 to +125		UNII	VCC	WAVEFORING	
		min.	typ.	max.	min.	max.	min.	max.	ентіт н	deelb n	arun a da 2 'SH	
^t PHL/	propagation delay D _n to Q _n	88	17	30	2.0	38) 2d	45	ns	4.5	Fig. 7	
^t PHL/ ^t PLH	propagation delay LE to Ω _n	8	16	32	1	40		48	ns	4.5	Fig. 8	
t _{PZH} / t _{PZL}	3-state output enable time OE to Qn		19	32	00	40	Š	48	ns	4.5	Fig. 9	
^t PHZ/ ^t PLZ	3-state output disable time $\overline{\text{OE}}$ to Q_n		18	30		38		45	ns	4.5	Fig. 9	
tTHL/ tTLH	output transition time		5	12	1	15	8	18	ns	4.5	Fig. 7	
t _W	LE pulse width HIGH	16	4	8	20	70 70 70	24	- i a	ns	4.5	Fig. 8	
t _{su}	set-up time D _n to LE	12	6		15		18		ns	4.5	Fig. 10	
th	hold time D _n to LE	4	-1		4		4		ns	4.5	Fig. 10	

AC WAVEFORMS

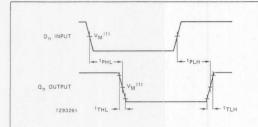


Fig. 7 Waveforms showing the input (D_n) to output (Q_n) propagation delays and the output transition times.

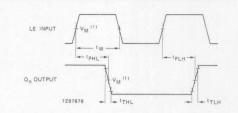


Fig. 8 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Ω_n) propagation delays and the output transition times.

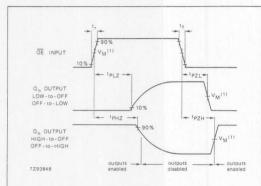


Fig. 9 Waveforms showing the 3-state enable and disable times.

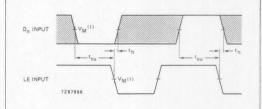


Fig. 10 Waveforms showing the data set-up and hold times for D_n input to LE input.

Note to Fig. 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

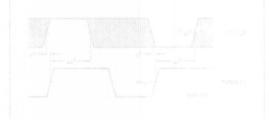
Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3$ V; $V_I = GND$ to 3 V.









OCTAL D-TYPE FLIP-FLOP; POSITIVE EDGE-TRIGGER; 3-STATE

FEATURES

- 3-state non-inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- · Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT374 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT374 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications.

A clock (CP) and an output enable (OE) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When \overline{OE} is LOW, the contents of the 8 flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

The "374" is functionally identical to the "534", but has non-inverting outputs.

	2.0.445750	CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT	
tPHL/ tPLH	propagation delay CP to Ω _n	C _L = 15 pF V _C C = 5 V	15	13	ns	
f _{max}	maximum clock frequency	ACC = 2 A	77	48	MHz	
CI	input capacitance	0.00	3.5	3.5	pF	
power dissipation capacitance per flip-flop		notes 1 and 2	17	17	pF	

GND = 0 V; $T_{amb} = 25 \, ^{\circ}C$; $t_r = t_f = 6 \, \text{ns}$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

 $PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$ where:

f_i = input frequency in MHz f_o = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

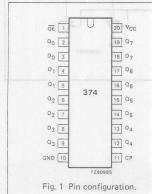
PACKAGE OUTLINES

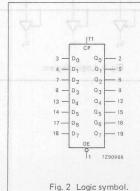
20-lead DIL; plastic (SOT146).

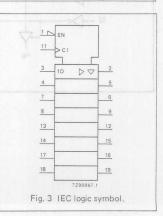
20-lead mini-pack; plastic (SO20; SOT163A).

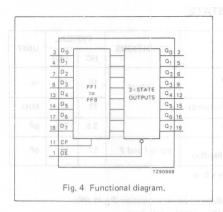
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	ŌĒ	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q ₀ to Q ₇	3-state flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D ₀ to D ₇	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	Vcc	positive supply voltage









FUNCTION TABLE

OPERATING MODES	- 1	NPUT	S	INTERNAL	OUTPUTS	
OPERATING MODES	ŌĒ	СР	Dn	FLIP-FLOPS	Q ₀ to Q ₇	
load and read register	L	†	l h	L H 46).	NUT LINES	
load register and disable outputs	Н	↑	l h	L H	Z Z	

H = HIGH voltage level

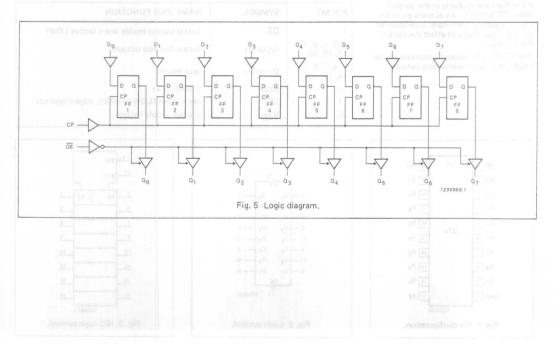
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

Z = high impedance OFF-state

↑ = LOW-to-HIGH CP transition



DC CHARACTERISTICS FOR 74HC 1990 VIEWS 11 notifies the state of the Policy of the Poli

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

AC CHARACTERISTICS FOR 74HC are not in avoid in the control of the state of the control of the c

 $GND = 0 \text{ V; } t_r = t_f = 6 \text{ ns; } C_L = 50 \text{ pF}$

		MA			T _{amb} (°C)		TEST CONDITIONS				
SYMBOL	PARAMETER				74HC				UNIT	V	WAVEFOR	90
STIVIBUL	PARAMETER	+25			-40 t	-40 to +85		-40 to +125		VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.	ZAHCT	FOR		
tPHL/	propagation delay CP to Q _n		50 18 14	165 33 28	100	205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 6	(N 0 = 0 V)
tPZH/	3-state output enable time OE to Q _n	207	41 15 12	150 30 26	TOHR	190 38 33	30	225 45 38	ns	2.0 4.5 6.0	Fig. 7	SYMBOL
^t PHZ/ ^t PLZ	3-state output disable time $\overline{\text{OE}}$ to Ω_{D}	JAST	50 18 14	150 30 26	in ini	190 38 33	yp. m	225 45 38	ns	2.0 4.5 6.0	Fig. 7	
t _{THL} /	output transition time	88	14 5 4	60 12 10	88	75 15 13	8 3	90 18 15	ns smit s	2.0 4.5 6.0	Fig. 6	/HZdz
tW	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns mit s	2.0 4.5 6.0	Fig. 6	77dz /2Hdz 72Hdz
t _{su}	set-up time D _n to CP	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8	JHT ²
^t h	hold time D _n to CP	5 5 5	-6 -2 -2	2	5 5 5		5 5 5	12	ns	2.0 4.5 6.0	Fig. 8	W ₃
f _{max}	maximum clock pulse frequency	6.0 30 35	23 70 83	8	4.8 24 28	8	4.0 20 24	. 8	MHz	2.0 4.5 6.0	Fig. 6 blod	H ₂

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications" A 2017 FIRE

Output capability: bus driver

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
ŌĒ	1.25
CP	0.90
D _n	0.35

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_f = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

		0.0					T _{amb} (°C)					TEST CONDITION	NS
0.44501	Pac. 7	2.0		68	S.		74H	СТ	01. 7		Section 5	lds (19.7)	WAVEFORMS	VIISH!
SYMBOL	PARAMETER			- 600	+25		-40 to +85		-40 to +125		UNIT	VCC	WAVEFORIUS	
				min.	typ.	max.	min.	max.	min.	max.	emir e	dezib 11		
t _{PHL} /	propagation CP to Q _n	delay		0.5	16	32	85	40	4 60	48	ns	4.5	Fig. 6	ne o
tPZH/ tPZL	3-state outpu ΘΕ to Q _n	ıt enabl	e time	ò	16	30		38	b i	45	ns	4.5	Fig. 7	137
^t PHZ/ ^t PLZ	3-state outpu ΘΕ to Q _n	ıt disabl	le time		18	28		35		42	ns	4.5	Fig. 7	
^t THL [/] ^t TLH	output transi	ition tin	ne		5	12		15	4	18	ns	4.5	Fig. 6	
t _W	clock pulse w HIGH or LO			19	11	B	24	E .	29	- 2	ns	4.5	Fig. 6	
t _{su}	set-up time D _n to CP			12	7	8	15	3	18		ns	4.5	Fig. 8	
^t h	hold time D _n to CP	4,5	sHM	5	-3	0 <u>5.</u> 43	5	21	5	35 8	ns	4.5	Fig. 8	No. of
fmax	maximum clo	ock puls	se	26	44		21		17		MHz	4.5	Fig. 6	

AC WAVEFORMS

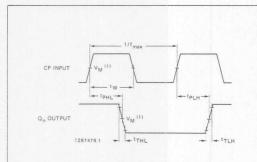


Fig. 6 Waveforms showing the clock (CP) to output (Ω_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

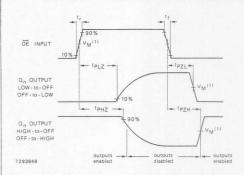


Fig. 7 Waveforms showing the 3-state enable and disable times.

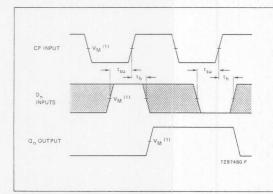


Fig. 8 Waveforms showing the data set-up and hold times for D_n input.

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_1 = GND$ to V_{CC} . HCT: $V_M = 1.3$ V; $V_1 = GND$ to 3 V.







OCTAL D-TYPE FLIP-FLOP WITH DATA ENABLE; POSITIVE-EDGE TRIGGER

FEATURES

- Ideal for addressable register applications
- Data enable for address and data synchronization applications
- Eight positive-edge triggered D-type flip-flops
- See "273" for master reset version
- See "373" for transparent latch version
- See "374" for 3-state version
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT377 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT377 have eight edgetriggered, D-type flip-flops with individual D inputs and Q outputs.

A common clock (CP) input loads all flip-flops simultaneously when the data enable (\overline{E}) is LOW.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

The \overline{E} input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

SYMBOL	DADAMETER	CONDITIONS	TYF	LIBUT		
	PARAMETER	CONDITIONS	нс	нст	UNIT	
tPHL/	propagation delay CP to Q _n	C _L = 15 pF V _{CC} = 5 V	13	14	ns	
f _{max}	maximum clock frequency	vCC - 2 v	77	53	MHz	
CI	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	20	pF	

 $GND = 0 \text{ V}; T_{amb} = 25 \text{ °C}; t_r = t_f = 6 \text{ ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

PD = CPD \times VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

fi = input frequency in MHz CL fo = output frequency in MHz VCC

CL = output load capacitance in pF VCC = supply voltage in V

 Σ (C_L x V_{CC}² x f₀) = sum of outputs 2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} - 1.5 V

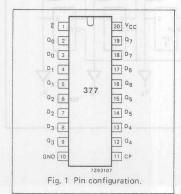
PACKAGE OUTLINES

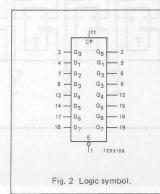
20-lead DIL; plastic (SOT146).

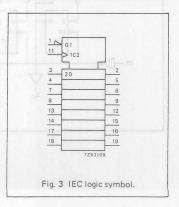
20-lead mini-pack; plastic (SO20; SOT163A).

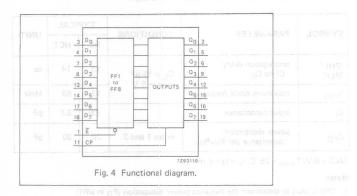
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1 40	E	data enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q ₀ to Q ₇	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D ₀ to D ₇	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	Vcc	positive supply voltage









FUNCTION TABLE 1 100 = 10

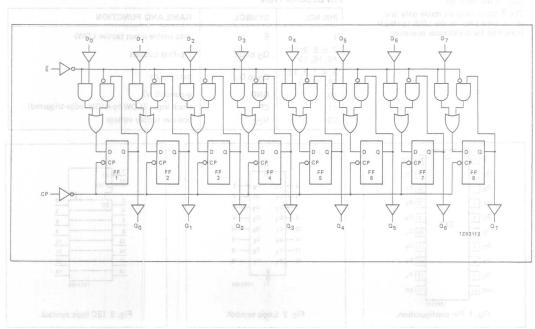
OPERATING	N Alddre	INPUT	OUTPUTS	
MODES	СР	√ a.Ē	Dn	OND On/ 2
load ''1''	1	1	h	Н
load "0"	1	1	1	L Lapi
hold (do nothing)	↑ X	h H	X	no change

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

TLC= LOW voltage level sale sale nemy visuas

I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition ↑ = LOW-to-HIGH CP transition

X = don't care



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_f = t_f = 6$ ns; $C_L = 50$ pF viring aft of navig of the bootstructure and (2016) there are viring tensorables to bulk and

					T _{amb} (°C)					TEST CONDITIONS
					74H	0				THE	INPUT COEFFICI
SYMBOL	PARAMETER		+25		-40 t	o +85	-40 to	o +125	UNIT	VCC V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/	propagation delay CP to Q _n		44 16 13	160 32 27		200 40 34		240 48 41	ns HAV	2.0 4.5 6.0	Fig. 6
tTHL/MOI	output transition time		19 7 6	75 15 13	(DF) d	95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
tW.	clock pulse width HIGH or LOW	80 16 14	14 5 4	5. LE	100 20 17	-	120 24 20		ns	2.0 4.5 6.0	Fig. 6
t _{su}	set-up time D _n to CP	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t _{su}	set-up time Ē to CP	60 12 10	6 2 2		75 15 13		90 18 15	τ	ns	2.0 4.5 6.0	Fig. 7
^t h	hold time D _n to CP	3 3 3	-8 -3 -2	81	3 3 3		3 3 3	e Us	ns	2.0 4.5 6.0	Fig. 7
^t h	hold time E to CP	4 4 4	-3 -1 -1	33	4 4 4	38	4 4 4	J 55	ns	2.0 4.5 6.0	Fig. 7
f _{max}	maximum clock pulse frequency	6 30 35	23 70 83	64	5 24 28	Z	4 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

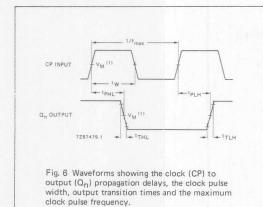
INPUT	UNIT LOAD COEFFICIENT
E	1.50
CP	0.50
Dn	0.20

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

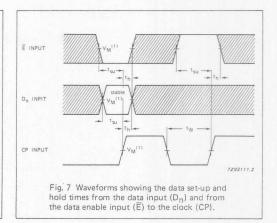
		9.5	20				T _{amb} (°C)			9	กส กอย่	TEST CONDITIONS
							74H	CT		8.			
SYMBOL	PARAMETE				+25	24	-40 t	o +85	-40 to	+125	UNIT	V _{CC}	WAVEFORMS
				min.	typ.	max.	min.	max.	min.	max.			
tPHL/ tPLH	propagation of CP to Ω _n	delay	2(17	32		40		48	ns	4.5	Fig. 6
tTHL/ tTLH	output transi	tion time	e		7	15		19		22	ns	4.5	Fig. 6
tW	clock pulse w HIGH or LC			20	8	ε	25		30		ns	4.5	Fig. 6
t _{su}	set-up time D _n to CP	6.0	0.0	12	4	0	15	8	18		ns	4.5	Fig. 7
t _{su}	set-up time E to CP	2.0 4.5 6.0	2/	22	12	D D	28	1 4	33		ns	4.5	Fig. 7
th	hold time D _n to CP	2,0	sHtt	2	-4	a. 05	2	T AS	2		ns	4.5	Fig. 7
th	hold time Ē to CP	0.5		3	-2	es .	3	911	3	S	ns	4.5	Fig. 7
f _{max}	maximum clo	ick pulse		27	48		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS



Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.



Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.





DUAL DECADE RIPPLE COUNTER

GENERAL DESCRIPTICASSUTA

- Two BCD decade or bi-quinary counters
- One package can be configured to divide-by-2, 4, 5, 10, 20, 25, 50 or 100
- Two master reset inputs to clear each decade counter individually
- Output capability: standard
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT390 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT390 are dual 4-bit decade ripple counters divided into four separately clocked sections. The counters have two divide-by-5 sections and two divide-by-5 sections. These sections are normally used in a RCD decade or

separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD decade or bi-quinary configuration, since they share a common master reset input (nMR). If the two master reset input (nMR) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clocks (nCP_Q and nCP₁) of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100.

(continued on next page)

	242445752	CONDITIONS	TYF	UNIT	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	OWIT
propagation delay nCP ₀ to nQ ₀ rCP ₁ to nQ ₁ rCP ₁ to nQ ₂ nCP ₁ to nQ ₂ nCP ₁ to nQ ₃ nMR to Q _n		C _L = 15 pF V _{CC} = 5 V	14 15 23 15 16	18 19 26 19	ns ns ns ns
^f max	maximum clock frequency nCP ₀ , nCP ₁	ama n. s	66	61	MHz
Cl	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per counter	notes 1 and 2	20	21	pF

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

Notes

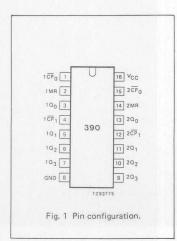
1. CPD is used to determine the dynamic power dissipation (PD in μ W):

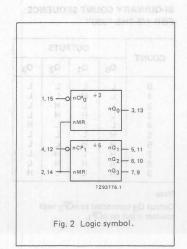
PD = CPD x VCC² x f_i +
$$\Sigma$$
 (CL x VCC² x f_o) where:

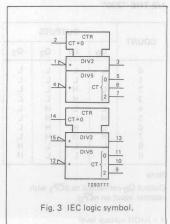
$$\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$$

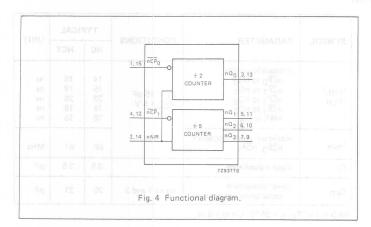
PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).









PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15 tonstier	1CP ₀ , 2CP ₀	clock input divide-by-2 section (HIGH-to-LOW, edge-triggered)
2, 14	1MR, 2MR	asynchronous master reset inputs (active HIGH)
3, 5, 6, 7	10 ₀ to 10 ₃ v =	flip-flop outputs
4, 12	1 <u>CP</u> ₁ , 2 <u>CP</u> ₁	clock input divide-by-5 section (HIGH-to-LOW, edge triggered)
8	GND	ground (0 V)
13, 11, 10, 9	2Q ₀ to 2Q ₃	flip-flop outputs
16	Vcc	flip-flop outputs positive supply voltage

BCD COUNT SEQUENCE FOR 1/2 THE "390"

COUNT	OUTPUTS									
COONT	00	01	02	03						
0	L	L	L	L						
1 -	H	L	L	L						
2	L	H	L	L						
3	Н	Н	L	L						
4	L	L	Н	L						
5	Н	Lol	H	L						
6	L	Н	Н	L						
7	Н	Н	Н	L						
8	L	L	L	Н						
9	H	L	L	Н						

Note

Output Q_0 connected to $n\overline{CP}_1$ with counter input on $n\overline{CP}_0$.

H = HIGH voltage level L = LOW voltage level

BI-QUINARY COUNT SEQUENCE FOR 1/2 THE "390"

COUNT	OUTPUTS									
COUNT	α ₀	Ω ₁	02	03						
0	L	L	L	L						
1	L	H	L	L						
2	L	L	Н	L						
3	L	Н	Н	L						
4	L	L	L	Н						
5	Н	L	L	L						
6	Н	Н	L	L						
7	H	L	Н	L						
8	H	H	Н	L						
9	H	Litter	-Ears	H						

Note

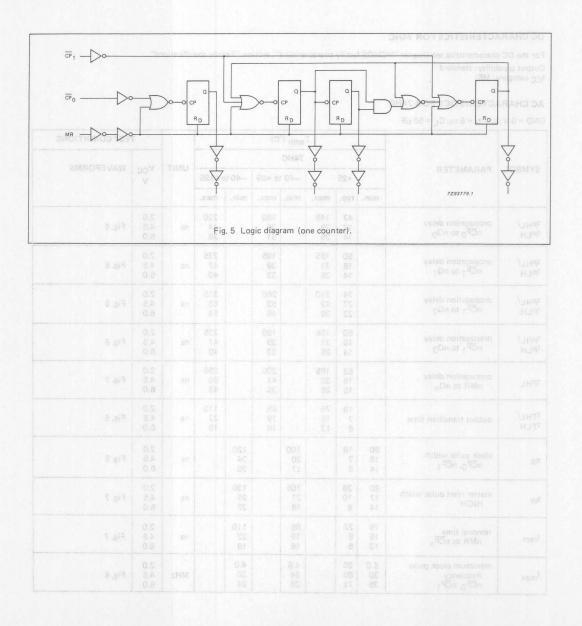
Output Q_3 connected to $n\overline{CP}_0$ with counter input on $n\overline{CP}_1$.

GENERAL DESCRIPTION

Each section is triggered by the HIGH-to-LOW transition of the clock inputs ($n\overline{CP}_0$ and $n\overline{CP}_1$). For BCD decade operation, the nQ_0 output is connected to the $n\overline{CP}_1$ input of the divide-by-5 section. For bi-quinary decade operation, the nQ_3 output is connected to the $n\overline{CP}_0$ input and nQ_0 becomes the decade output.

The master reset inputs (1MR and 2MR) are active HIGH asynchronous inputs to each decade counter which operates on the portion of the counter identified by the "1" and "2" prefixes in the pin configuration. A HIGH level on the nMR input overrides the clocks and sets the four outputs LOW.





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

	$t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$										
			ļ		T _{amb} (°C)					FEST CONDITIONS
SYMBOL	PARAMETER	74HC						ě	UNIT	Vcc	WAVEFORMS
STIVIBOL	PARAMETER	+25		ONT	V CC	WAVEFURIVIS					
	(45,400)	min.	typ.	max.	min.	max.	min.	max.			
^t PHL/ ^t PLH	propagation delay nCP ₀ to nQ ₀		47 17 14	145 29 25	ja) me	180 36 31	o.l.d.	220 44 38	ns	2.0 4.5 6.0	Fig. 6
tPHL/ tPLH	propagation delay		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 6
^t PHL [/]	propagation delay		74 27 22	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 6
^t PHL [/] ^t PLH	propagation delay		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 6
^t PHL	propagation delay nMR to nQ _n		52 19 15	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 7
^t THL [/] ^t TLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
tW	clock pulse width nCP ₀ , nCP ₁	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t₩	master reset pulse w dth HIGH	80 17 14	28 10 8		105 21 18		130 26 22		ns	2.0 4.5 6.0	Fig. 7
^t rem	removal time nMR to nCPn	75 15 13	22 8 6		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 7
f _{max}	maximum clock pulse frequency nCP ₀ , nCP ₁	6.0 30 35	20 60 71		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nCP ₀	0.45 0.60

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

	urpur (nO _n) propagation dela pok (nOR _n) removal time.	0 07 39		iom on	r _{amb} (°C)		TEST CONDITIONS			
SYMBOL		000.0	74HCT								
SAMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		GND	lote to AC waveforms. 1) HC .: V _M = 50%; V ₁
tPHL/	propagation delay		21	34		43		51	ns ns	4.5	Fig. 6
t _{PHL} /	propagation delay nCP ₁ to nQ ₁		22	38		48		57	ns	4.5	Fig. 6
t _{PHL} /	propagation delay nCP ₁ to nQ ₂		30	51		64		77	ns	4.5	Fig. 6
t _{PHL} /	propagation delay nCP ₁ to nQ ₃		22	38		48		57	ns	4.5	Fig. 6
^t PHL	propagation delay nMR to nQ _n		21	36		45		54	ns	4.5	Fig. 7
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 6
tW	clock pulse width nCP ₀ , nCP ₁	18	8		23		27		ns	4.5	Fig. 6
tw	master reset pulse width HIGH	17	10		21		26		ns	4.5	Fig. 7
t _{rem}	removal time nMR to nCPn	15	8		19		22		ns	4.5	Fig. 7
fmax	maximum clock pulse frequency nCP ₀ , nCP ₁	27	55		22		18		MHz	4.5	Fig. 6

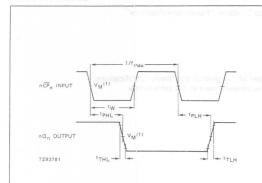


Fig. 6 Waveforms showing the clock $(n\overline{CP}_n)$ to output (nQ_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

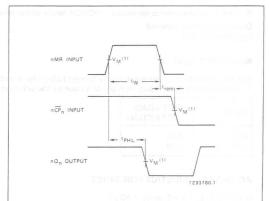


Fig. 7 Waveforms showing the master reset (nMR) pulse width, the master reset to output (nQ_n) propagation delays and the master reset to clock (n $\overline{\text{CP}}_n$) removal time.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

DUAL 4-BIT BINARY RIPPLE COUNTER

FEATURES OF SOURCES THUCO

- Two 4-bit binary counters with individual clocks
- Divide-by any binary module up to 28 in one package
- Two master resets to clear each
 4-bit counter individually
- Output capability: standard
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT393 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT393 are 4-bit binary ripple counters with separate clocks (1CP and 2 CP) and master reset (1MR and 2MR) inputs to each counter. The operation of each half of the "393" is the same as the "93" except no external clock connections are required.

The counters are triggered by a HIGH-to-LOW transition of the clock inputs. The counter outputs are internally connected to provide clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high-speed address decoding.

The master resets are active-HIGH asynchronous inputs to each 4-bit counter identified by the "1" and "2" in the pin description.

A HIGH level on the nMR input overrides the clock and sets the outputs LOW.

OV/MED O I	BARAMETER	CONDITIONS	TYF			
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT	
^t PHL [/] ^t PLH	propagation delay $n\overline{CP}$ to $n\Omega_0$ $n\Omega$ to $n\Omega_{n+1}$ nMR to $n\Omega_n$	C _L = 15 pF V _{CC} = 5 V	12 5 11	20 6 15	ns ns ns	
f _{max}	maximum clock frequency	h look	99	53	MHz	
CI	input capacitance	2 -01	3.5	3.5	рF	
C _{PD}	power dissipation capacitance per counter	notes 1 and 2	23	25	pF	

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

f; = input frequency in MHz f_O = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

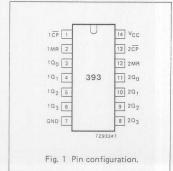
PACKAGE OUTLINES

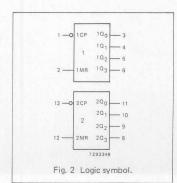
14-lead DIL; plastic (SOT27).

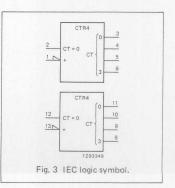
14-lead mini-pack; plastic (SO14; SOT108A).

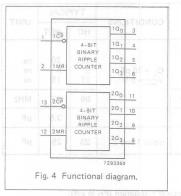
PIN DESCRIPTION

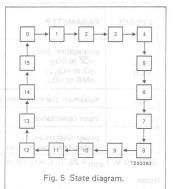
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1CP, 2CP	clock inputs (HIGH-to-LOW, edge-triggered)
2, 12	1MR, 2MR	asynchronous master reset inputs (active HIGH)
3, 4, 5, 6, 11, 10, 9, 8	1Q ₀ to 1Q ₃ , 2Q ₀ to 2Q ₃	flip-flop outputs
7	GND	ground (0 V)
14	Vcc	positive supply voltage

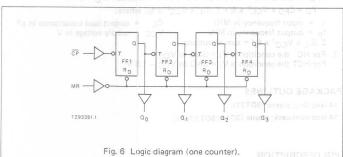










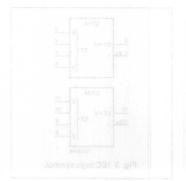


COUNT SEQUENCE FOR 1 COUNTER

COLINIT		OUT	PUTS	
COUNT	Ω ₀	01	02	03
	suHivii nsb :yr	n Egalo il Hoga	nde she	-L □L ∞
6 beaut	OL SIL	H	Н	e de la composition della comp
8 m being 9 on bish 10 v isold 11 accord	are Aper E C Han are 4 bit	L L H	ar Luca ar Luca ar Luca ar Luca	H
13	o Had r	L L H	H H	H H

H = HIGH voltage level

L = LOW voltage level







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

SYMBOL		T _{amb} (°C)								TEST CONDITIONS		
	PARAMETER	74HC								, TVE	WAVEFORMS	
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}		
		min.	typ.	max.	min.	max.	min.	max.			0,4	2CP TMR
t _{PHL} /	propagation delay nCP to nQ ₀		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7	HWS
tPHL/	propagation delay nQ _n to nQ _{n+1}		14 5 4	45 9 8	400	55 11 9		70 14 12	ns	2.0 4.5 6.0	Fig. 7	
^t PHL	propagation delay	201	39 14 11	140 28 24	TOH!	175 35 30	200	210 42 36	ns	2.0 4.5 6.0	Fig. 8	JOSMYS
tTHL/ tTLH	output transition time	.881	19 7 6	75 15 13	em La	95 19 16	ores .cp	110 22 19	ns	2.0 4.5 6.0	Fig. 7	
tw	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	PLH
tW	master reset pulse width; HIGH	80 16 14	19 7 6		100 20 17		120 24 20	8	ns	2.0 4.5 6.0	Fig. 8	HT8
^t rem	removal time nMR to nCP	5 5 5	3 1 1		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8	JH9
^f max	maximum clock pulse frequency	6 30 35	30 90 107	98	5 24 28	5	4 20 24	1 61	MHz	2.0 4.5 6.0	Fig. 7	HJT

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1CP	0.4 V
2CP	0.4
1MR	1.0
2MR	1.0

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	PARAMETER	T _{amb} (°C)								TEST CONDITIONS		
SYMBOL PAR		10 I	74HCT 85 41							Jelay	WAVEFORMS	
	PARAMETER 0.8	i c	+25		-40 to +85		-40 to +125		UNIT	VCC	WAVEFORING	
	2.0 4.5 - Pig. 7	min.	typ.	max.	min.	max.	min.	max.	6	nii noi:	THE OWNER TRANSPORT	
t _{PHL} /	propagation delay	211	15	25		31	S. F.	38 08	ns	4.5	Fig. 7	
^t PHL/	propagation delay nQ _n to nQ _{n+1}	en	6	10	0	13		15 DE	ns	4.5 salur	Fig. 7	
^t PHL	propagation delay	2.	18	32		40		48	ns	4.5	Fig. 8	
t _{THL} / t _{TLH}	output transition time		7	15		19 3		22	ns	4.5	Fig. 7	
t _W	clock pulse width HIGH or LOW	19	11	20	24	24	29	95 96 95 96	ns	4.5	Fig. 7	
tw	master reset pulse width; HIGH	16	6		20		24		ns	4.5	Fig. 8	
^t rem	removal time nMR to nCP	5	0		5		5		ns	4.5	Fig. 8	
fmax	maximum clock pulse frequency	27	48		22		18		MHz	4.5	Fig. 7	

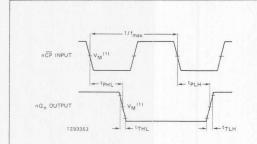


Fig. 7 Waveforms showing the clock $(n\overline{CP})$ to output $(1\Omega_n, 2\Omega_n)$ propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

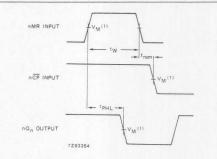


Fig. 8 Waveforms showing the master reset (nMR) pulse width, the master reset to output (Ω_n) propagation delays and the master reset to clock $(n\overline{CP})$ removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.





Note to AC waveforms

11) HC | VM = 50%, V = GND to VCC

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

FEATURES

- DC triggered from active HIGH or money active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- Output capability: standard (except for nREXT/CEXT)
- I_{CC} category: MSI

SYMBOL	DADAMETED	CONDITIONS		TYPICAL		
	PARAMETER	CONDITIONS	НС	нст	UNIT	
tPHL/	propagation delay $n\overline{A}$, nB to nQ , $n\overline{Q}$ $n\overline{R}_D$ to nQ , $n\overline{Q}$	C _L = 15 pF V _{CC} = 5 V R _{EXT} = 5 kΩ C _{EXT} = 0 pF	25 20	26 22	ns ns	
Cpriteb at d	input capacitance	9	3.5	3.5	pF	
tW plw esine	minimum output nuice	notes 1 and 2	75	75	ns	

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

- 1. CpD is used to determine the dynamic power dissipation (PD in μ W):
- TTL (LSTTL). They are specified in PD = CPD × $V_{CC}^2 \times f_1 + \Sigma(C_L \times V_{CC}^2 \times f_0) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_0 + 0.75 \times C_{EXT}^2 \times V_{CC}^2 \times V_{CC}^$ + D x 16 x V_{CC} where:
 - f; = input frequency in MHz
 - fo = output frequency in MHz D = duty factor in %
- = output load capacitance in pF
- V_{CC} = supply voltage in V C_{EXT} = timing capacitance in pF
- $\Sigma(C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_1 = GND to V_{CC} For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 V$

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1Ā, 2Ā	trigger inputs (negative-edge triggered)
2, 10	1B, 2B	trigger inputs (positive-edge triggered)
3, 11	1RD, 2RD	direct reset action (active LOW)
4, 12	10, 20	outputs (active LOW) feval spallov WOJ =
7	2REXT/CEXT	external resistor/capacitor connection
8	GND	ground (0 V) notineed WO J-ot-HOTH
13, 5	10, 20	outputs (active HIGH)
14, 6	1CEXT, 2CEXT	external capacitor connection
15	1REXT/CEXT	external resistor/capacitor connection
16	Vcc	positive supply voltage

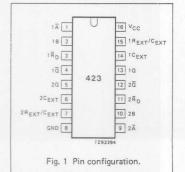
GENERAL DESCRIPTION

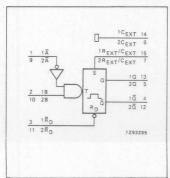
The 74HC/HCT423 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky compliance with JEDEC standard no. 7A.

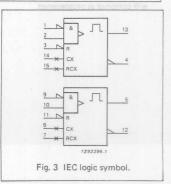
The 74HC/HCT423 are dual retriggerable monostable multivibrators with output pulse width control by two methods. The basic pulse time is programmed by selection of an external resistor (REXT) and capacitor (CEXT). The external resistor and capacitor are normally connected as shown in Fig. 6.

Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input (nA) or the active HIGH-going edge input (nB). By repeating this process, the output pulse periode (nQ = HIGH, $n\overline{Q} = LOW$) can be made as long as desired. When $n\overline{R}_D$ is LOW, it forces the nQ output LOW, the nQ output HIGH and also inhibits the triggering.

(continued on next page)







GENERAL DESCRIPTION (Cont'd)

Figures 7 and 8 illustrate pulse control 42 H subsequently and a by reset. The basic output pulse width is essentially determined by the values of the external timing components REXT

and CEXT. For pulse widths, when $C_{EXT} < 10\,000\,\mathrm{pF}$, see Fig. 9. When $C_{EXT} > 10\,000\,\mathrm{pF}$, the typical

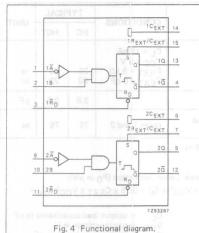
output pulse width is defined as: 109 (49) backbogge : v (100 pulse 100 pulse

 $t_W = 0.45 \times R_{EXT} \times C_{EXT}$ (typ.),

where, t_W = pulse width in ns; R_{EXT} = external resistor in $k\Omega$; CEXT = external capacitor in pF. MOIT918 3330 M 3330

Schmitt-trigger action in the $n\overline{A}$ and nB inputs, makes the circuit highly tolerant to slower input rise and fall times.

The "423" is identical to the "123" but an only one say the say of cannot be triggered via the reset input. A conbustions of



FUNCTION TABLE

FUNCTIO	N TABLE				
	INPUTS		OUT		
$n\overline{R}_D$	nĀ	nB	nQ	nΩ	
L X	X	X	L L*	H H * H *	
Н	L	NC140N	A GMA B	ma-ir	
Н	emegini eg	Н	a) e	7	

= HIGH voltage level

= LOW voltage level MOJ switch

= don't care

= LOW-to-HIGH transition

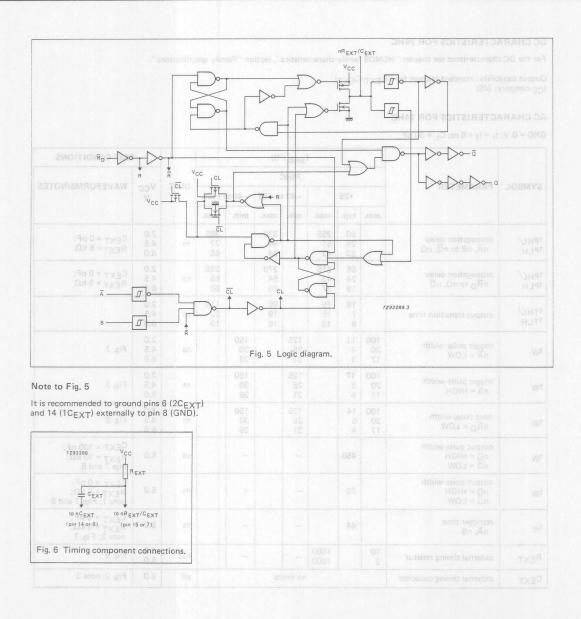
= HIGH-to-LOW transition ___ = one HIGH level output pulse and enumber

= one LOW level output pulse

* If the monostable was triggered before this condition was established, the pulse will continue as programmed.







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for nR_{EXT}/C_{EXT}) I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	9-05-05	h			T _{amb} (°C)				(T	TEST CONDITIONS	
	and aded		-	1	74H	С				.,	WAYEEODAS (NOTES	
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	VCC	WAVEFORMS/NOTES	
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay nĀ, nB to nQ, nQ	1	80 29 23	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	C _{EXT} = 0 pF; R _{EXT} = 5 kΩ	
t _{PHL} /	propagation delay nRD to nQ, nQ		66 24 19	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	C _{EXT} = 0 pF; R _{EXT} = 5 kΩ	
t _{THL} /	output transition time		19 7 6	75 15 13		95 19 16	1-	110 22 19	ns	2.0 4.5 6.0		
t _W	trigger pulse width nĀ = LOW	100 20 17	11 4 3	.menga	125 25 21	J & pi	150 30 26		ns	2.0 4.5 6.0	Fig. 7	
tw	trigger pulse width nB = HIGH	100 20 17	17 6 5		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7	
tW	reset pulse width nRD = LOW	100 20 17	14 5 4		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8	
tW	output pulse width nQ = HIGH nQ = LOW		450		-		_		μs	5.0	$C_{EXT} = 100 \text{ nF};$ $R_{EXT} = 10 \text{ k}\Omega;$ Figs 7 and 8	
tW	output pulse width $n\underline{Q} = HIGH$ $n\overline{Q} = LOW$		75		_		-		ns	5.0	$C_{EXT} = 0 pF;$ $R_{EXT} = 5 k\Omega;$ note 1; Figs 7 and 8	
t _{rt}	retrigger time nA, nB		44		-		-		ns	5.0	$C_{EXT} = 0 \text{ pF};$ $R_{EXT} = 5 \text{ k}\Omega;$ note 2; Fig. 7	
REXT	external timing resistor	10		1000 1000	-		-		kΩ	2.0 5.0	Fig. 9	
C _{EXT}	external timing capacitor				no lim	its		-	pF	5.0	Fig. 9; note 3	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for nR_{EXT}/C_{EXT}) I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nĀ, nB	0.35 0.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		1 3 0			r _{amb} (°C)			n etaitini	TEST CONDITIONS		
				V Glovelle	74HC	Т				.,		
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS/NOTES	
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay nĀ, nB to nQ, nQ		30	51		64		77	ns	4.5	C _{EXT} = 0 pF; R _{EXT} = 5 kΩ	
t _{PHL} /	propagation delay nRD to nQ, nQ		26	48		60		72	ns	4.5	C _{EXT} = 0 pF; R _{EXT} = 5 kΩ	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5		
tw	trigger pulse width nA = LOW	20	5		25		30		ns	4.5	Fig. 7	
tW	trigger pulse width nB = HIGH	20	5		25		30		ns	4.5	Fig. 7	
tW	reset pulse width nRD = LOW	20	7		25		30		ns	4.5	Fig. 8	
tw	output pulse width $nQ = HIGH$ $n\overline{Q} = LOW$		450		-		-		μs	5.0	C_{EXT} = 100 nF; R_{EXT} = 10 k Ω ; Figs 7 and 8	
tW	output pulse width $nQ = HIGH$ $n\overline{Q} = LOW$		75		-		-		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 k Ω ; note 1; Figs 7 and 8	
^t rt	retrigger time nĀ, nB		41		-		-		ns	5.0	$C_{EXT} = 0 \text{ pF};$ $R_{EXT} = 5 \text{ k}\Omega;$ note 2; Fig. 7	
REXT	external timing resistor	2		1000	_		_		kΩ	5.0	Fig. 9	
C _{EXT}	external timing capacitor			-	no limi	ts			pF	5.0	Fig 9; note 3	

Notes to AC characteristics

1. For other REXT and CEXT combinations see Fig. 9. Tables of Cables and

If $C_{EXT} > 10 pF$, the next formula is valid:

tW = K x REXT x CEXT (typ.)

where, tw = output pulse width in ns;

 $R_{\rm EXT}$ = external resistor in kΩ; $C_{\rm EXT}$ = external capacitor in pF; K = constant = 0.45 for $V_{\rm CC}$ = 5.0 V and 0.55 for $V_{\rm CC}$ = 2.0 V.

The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.

2. The time to retrigger the monostable multivibrator depends on the values of $R_{\mbox{EXT}}$ and $C_{\mbox{EXT}}$.

The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time.

If $C_{EXT} > 10$ pF, the next formula (at $V_{CC} = 5.0$ V) for the set-up time of a retrigger pulse is valid:

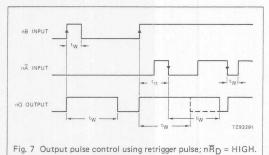
$$t_{rt} = 35 + (0.11 \times C_{EXT}) + (0.04 \times R_{EXT} \times C_{EXT})$$
 (typ.)

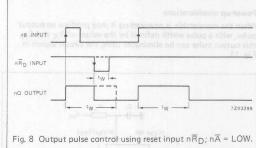
where, t_{rt} = retrigger time in ns; C_{EXT} = external capacitor in pF;

 $R_{EXT} = external resistor in k\Omega$.

The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.

3. When the device is powered-up, initiate the device via a reset pulse, when $C_{\mbox{EXT}} < 50 \mbox{ pF}$.





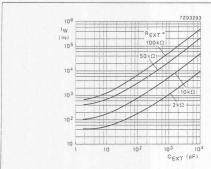


Fig. 9 Typical output pulse width as a function of the external capacitor values at V $_{CC}$ = 5.0 V and T_{amb} = 25 °C.

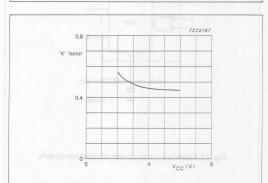
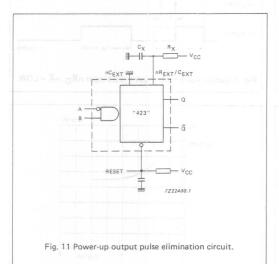


Fig. 10 Typical 'K' factor; external capacitance = 10 nF, external resistance = 10 k Ω to 100 k Ω and Tamb = 25 °C.

APPLICATION INFORMATION

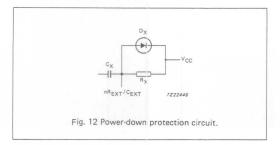
Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_X and C_{X} , this output pulse can be eliminated using the circuit shown in



Power-down considerations

A large capacitor (C_X) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of $V_{\rm CC}$ to zero occurs, the monostable may substain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode $(D\chi)$ preferably a germanium or Schottky-type diode able to withstand large current surges and connect as shown in Fig. 12.







OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE; INVERTING

FEATURES

- 3-state inverting outputs for bus oriented applications
- Common 3-state output enable input
- Output capability: bus driver
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT533 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT533 are octal D-type transparent latches f eaturing separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable (OE) input are common to all latches.

The "533" consists of eight D-type transparent latches with 3-state inverting outputs. When LE is HIGH, data at the Dn inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{\text{OE}}$ is LOW, the contents of the 8 latches are available at the outputs. When OE is HIGH, the outputs go to the high impedance OFF-state. Operation of the OE input does not affect the state of the latches.

The "533" is functionally identical to the "373", "563" and "573", but the "373" and "573" have non-inverted outputs and the "563" and "573" have a different pin arrangement.

CV/MDO1	DAGAMETED	CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	нс	нст	ONT	
t _{PHL} /	propagation delay D_n to $\overline{\Omega}_n$ LE to $\overline{\Omega}_n$	C _L = 15 pF V _{CC} = 5 V	14 18	16 19	ns ns	
CI	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per latch	notes 1 and 2	34	34	pF	

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μW): ΔΤ ΜΟΥΤΟΙΑΙΙΑ

PD = CPD
$$\times$$
 VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

f; = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V fo = output frequency in MHz

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is VI = GND to VCC For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 V$

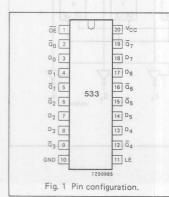
PACKAGE OUTLINES

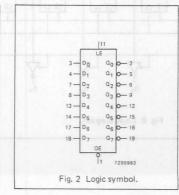
20-lead DIL; plastic (SOT146).

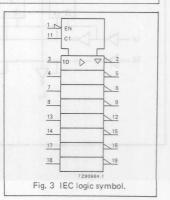
20-lead mini-pack; plastic (SO20; SOT163A).

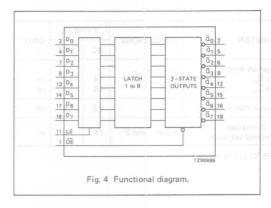
PIN DESCRIPTION

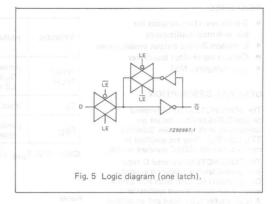
PIN NO.	SYMBOL	NAME AND FUNCTION
1	ŌĒ	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$\overline{\mathbb{Q}}_0$ to $\overline{\mathbb{Q}}_7$	3-state latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D ₀ to D ₇	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	Vcc	positive supply voltage











FUNCTION TABLE

OPERATING MODES	11	NPUT	S	INTERNAL	OUTPUTS
OPERATING MODES	ŌĒ	LE	Dn	LATCHES	$\overline{\mathbb{Q}}_0$ to $\overline{\mathbb{Q}}_7$
enable and read register (transparent mode)	L	Н	L H	SO L + OH	n = i (si no
latch and read register	L L	L	l h	L H sears	148H (SO4); SO
latch register and disable outputs	Н	X	X	X	Z Z

H = HIGH voltage level h = HIGH voltage level one set-up prior to

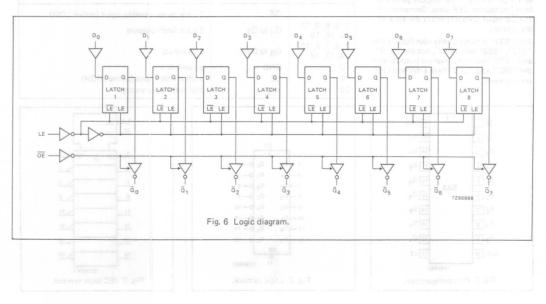
the HIGH-to-LOW LE transition

L = LOW voltage level

L = LOW voltage level ont set-up prior to the HIGH-to-LOW LE transition

X = don't care

Z = high impedance OFF-state



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

PARAMETER propagation delay Dn to Qn propagation delay LE to Qn		min.	+25 typ. 47 17 14 58	max. 150 30 26	74H0	max. 190 38	-40 to	max.	UNIT	Vcc V	WAVEFOR	30
propagation delay D_n to \overline{Q}_n propagation delay E to \overline{Q}_n		min.	47 17 14 58	max. 150 30 26		max. 190 38		max.	TANGT	V 2.0	0.30	30
\mathbb{D}_n to \mathbb{Q}_n aropagation delay LE to $\overline{\mathbb{Q}}_n$		min.	47 17 14 58	150 30 26	min.	190 38	min.	225				
\mathbb{D}_n to \mathbb{Q}_n aropagation delay LE to $\overline{\mathbb{Q}}_n$			17 14 58	30 26		38					CTERISTIC	
LE to $\overline{\mathbb{Q}}_n$						33		38	ns ag 0	4.5 6.0	Fig. 7	
	max22m1		21 17	175 35 30	0°1 dm	220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8	
ŌΕ to Ō _n	time	+128	44 16 13	150 30 26	40 to	190 38 33	#S+	225 45 38	ns	2.0 4.5 6.0	Fig. 9	
3-state output disable \overline{OE} to $\overline{\Omega}_{n}$	e time	18	50 18 14	150 30 26	-030	190 38 33	- AlV:	225 45 38	ns	2.0 4.5 6.0	Fig. 9	/JHd1
output transition time	e	45	14 5 4	60 12 10		75 15 13	22	90 18 15	ns	2.0 4.5 6.0	Fig. 7	H14) /TH4)
_E pulse width HIGH	en	80 16 14	14 5 4		100 20 17	8	120 24 20		ns emis eig	2.0 4.5 6.0	Fig. 8	/ZHd; 7Zd; /HZd;
et-up time D _n to LE	an	50 10 9	3 1 1	a	65 13 11	2	75 15 13		ns	2.0 4.5 6.0	Fig. 10	7145 7145
nold time D _n to LE	bn.	35 7 6	3 1 1		45 9 8		55 11 9	31	ns	2.0 4.5 6.0	Fig. 10	102
e	OE to Qn utput transition tim E pulse width HIGH trup time On to LE	E pulse width HIGH It-up time Dn to LE Dn to LE	DE to Qn Utput transition time E pulse width	utput transition time $\begin{bmatrix} 18\\14\\ 14\\ 14\\ 14\\ 14\\ 14\\ 14\\ 14\\ 16\\ 16\\ 14\\ 14\\ 14\\ 14\\ 16\\ 10\\ 10\\ 10\\ 10\\ 10\\ 10\\ 10\\ 10\\ 10\\ 10$	18 30 14 26 26 26 26 26 26 27 27	18 30 14 26 26 26 26 26 26 26 26 27 26 27 27	18 30 38 33 38 38 39 38 39 38 39 39	18 30 38 33 38 34 26 33 38 34 36 36 37 38 38 38 38 38 38 38	18 30 38 38 38 38 38 38 3	18 30 38 38 38 38 38 38 3	18 30 38 38 45 50 6.0	18 30 38 38 45 55 6.0 Fig. 9

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LO	
D _n	0.15	
LE	0.30	
ŌĒ	0.55	

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	Fig. 8			203		4	T _{amb} (°C)				TEST CONDITIONS		
				74HCT								WANTED DAME		
SYMBOL	PARAMETE	2.0 R 4.6 6.0		- 65 65	+25	8	-40	to +85	-40 to	+125	UNIT	V _{CC}	WAVEFORMS	
0.0		min.	typ.	max.	min.	max.	min.	max.						
t _{PHL} /	propagation D_n to \overline{Q}_n	delay	30	45 38	19	34	0	43	8 3	51	ns	4.5	Fig. 7	151191 1319
tPHL/ tPLH	propagation LE to $\overline{\Omega}_n$	delay	261	90 18	22	38		48		57	ns em	4.5	Fig. 8	J-TI
tPZH/ tPZL	3-state outp	ut enal	ole time		19	35	00	44	14	53	ns	4.5	Fig. 9	
tPHZ/ tPLZ	3-state outpool \overline{OE} to \overline{Q}_n	ut disa	ble time		18	30	7	38	A L	45	ns	4.5	Fig. 9	1477
t _{THL} / t _{TLH}	output trans	ition t	ime Rn		5	12	1 0	15		18	ns	4.5	Fig. 7	.82
t _W	LE pulse wid	2. dtb	En	16	5		20	3	24	35	ns	4.5	Fig. 8	/6
t _{su}	set-up time D _n to LE	0.0		10	3	6	13	3	15	- 8	ns	4.5	Fig. 10	
th	hold time D _n to LE			8	2		10		12		ns	4.5	Fig. 10	

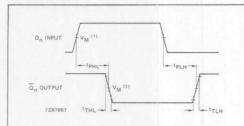


Fig. 7 Waveforms showing the data input (D_n) to output ($\overline{\text{O}}_{\text{n}}$) propagation delays and the output transition times.

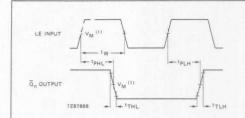


Fig. 8 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output $(\overline{\Omega}_n)$ propagation delays and the output transition times.

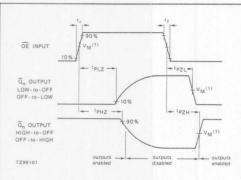


Fig. 9 Waveforms showing the 3-state enable and disable times.

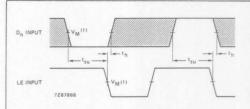


Fig. 10 Waveforms showing the data set-up and hold times for D_n input to LE input.

Note to Fig. 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

NAV PAR PARK



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Fig. 8: Waveform showing the latter enable injust to (LE) suites writing the latter enable injust to output (din). On provingation delays and the output contribution times.



Fig. 10. Mayeforms moveling the data set-up and hold tenant for Dr., input to the finance.

More in Fig. 10.
The entired areas indicate when the imputies increase to strongs for predictable output.

More U. A. waseforms

1. 190. Vin. - 50%, V₁ = GND to V_O

1. 190. Vin. - 51. V₁ V₁ = GND to 3 V

OCTAL D-TYPE FLIP-FLOP; POSITIVE EDGE-TRIGGER; 3-STATE; INVERTING

FEATURES

- 3-state inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- · Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT534 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT534 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable (OE) input are common to all flip-flops. The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition. When OE is LOW, the contents of the 8 flip-flops are available at the outputs. When OE is HIGH, the outputs go to the high impedance OFF-state. Operation of the OE input does not affect the state of

The "534" is functionally identical to the "374", but has inverted outputs.

the flip-flops.

			TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT	
t _{PHL} /	propagation delay CP to Q _n	C _L = 15 pF V _{CC} = 5 V	12	13	ns	
f _{max}	maximum clock frequency	S-STATE TO	61	40	MHz	
Cl	input capacitance	81 80	3.5	3.5	pF	
C _{PD} power dissipation capacitance per flip-flo		notes 1 and 2	19	19	pF	

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

- fi = input frequency in MHz fo = output frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}

 For HCT the condition is V_I = GND to V_{CC} 1.5 V

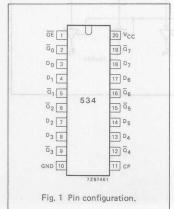
PACKAGE OUTLINES

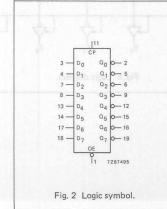
20-lead DIL; plastic (SOT146).

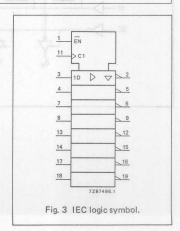
20-lead mini-pack; plastic (SO20; SOT163A).

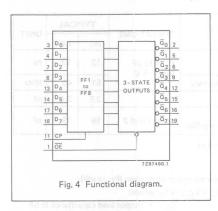
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	ŌĒ	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$\overline{\mathtt{Q}}_0$ to $\overline{\mathtt{Q}}_7$	3-state outputs
3, 4, 7, 8, 13, 14, 17, 18	D ₀ to D ₇	data inputs
10	GND	ground (0 V)
11 10	CP -	clock input (LOW-to-HIGH, edge-triggered)
20	Vcc	positive supply voltage









FUNCTION TABLE

ODED ATIMO MODEO	IN	IPU'	rs	INTERNAL	OUTPUTS
OPERATING MODES	ŌĒ	СР	Dn	FLIP-FLOPS	$\overline{\mathbf{Q}}_0$ to $\overline{\mathbf{Q}}_7$
load and read register	L	†	l h	L H (Afa)	H, (and
load register and disable outputs	Н	↑	l h	L H	Z Z

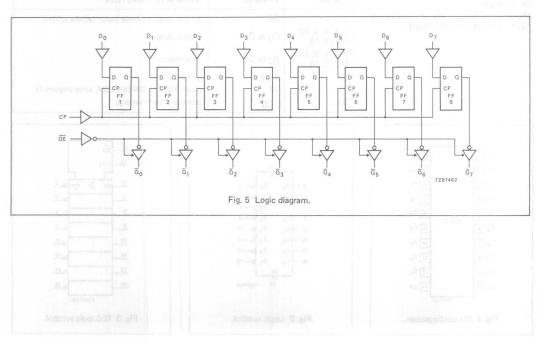
H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

= LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

Z = high impedance OFF-state ↑ = LOW-to-HIGH clock transition



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; Vilimat adr ni nevig si 1 to best tinu a rat (2013) sname vidgus messaipt landstible to sulev and wood elparent ni owark mainthead best tinu and yet autovants regard animately of

					T _{amb} (°C)					TEST CONDIT	ONS
SYMBOL	PARAMETER				74HC				UNIT	V	WAVEFORMS	
STINDOL	PANAMETER	+25		-40	-40 to +85		-40 to +125		V _{CC}	0.90		
		min.	typ.	max.	min.	max.	min.	max.			0.35	
^t PHL/ ^t PLH	propagation delay CP to $\overline{\Omega}_{n}$		41 15 12	165 33 28		205 41 35		250 50 43	ns a	2.0 4.5 6.0	Fig. 6	
t _{PZ.H} /2MO	3-state output enable time OE to $\overline{\Omega}_n$		33 12 10	150 30 26	(2°)	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
t _{PHZ} /	3-state output disable time OE to $\overline{\Omega}_n$	825	41 15 12	150 30 26	B+ or 0	190 38 33	8:	225 45 38	ns	2.0 4.5 6.0	Fig. 7	JOBMY
tTHL/ tTLH	output transition time	3	14 5 4	60 12 10	38	75 15 13	98	90 18 15	ns	2.0 4.5 6.0	Fig. 6	HT4 /TH8
tw	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20	or	ns	2.0 4.5 6.0	Fig. 6	1Z1 HZH/
t _{su}	set-up time D _n to CP	60 12 10	6 2 2		75 15 13		90 18 15	87	ns	2.0 4.5 6.0	Fig. 8	PUZ/ PHZ/
t _h	hold time D _n to CP	5 5 5	-3 -1 -1		5 5 5		5 5 5	3	ns	2.0 4.5 6.0	Fig. 8	THE
f _{max}	maximum clock pulse frequency	6.0 30 35	18 55 66	35	4.8 24 28	29	4.0 20 24	6 6	MHz	2.0 4.5 6.0	Fig. 6	W

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
ŌĒ	3 1.25 3 VAW 5
CP	0.90
Dn	0.35

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	4.5 Fig. 7	2.0			T _{amb} (°C)				akitina.	TEST CONDITIONS	hug:
	0.0		86,		74H	CT	97	ni -			NO CLED	
SYMBOL	PARAMETER O.S.	21	+25		-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
	0.0	min	typ.	max.	min.	max.	min.	max.			0E to 0 _B	
t _{PHL} /	propagation delay CP to $\overline{\mathbb{Q}}_n$	36	16	30	15	38	ST M	45	ns	4.5	Fig. 6	H
t _{PZH} / t _{PZL}	3-state output enable time OE to $\overline{\Omega}_n$	20	16	30		38		45	ns	4.5	Fig. 7	V
t _{PHZ} /	3-state output disable time OE to $\overline{\Omega}_n$	31	18	30		38		45	ns	4.5	Fig. 7	L/I
t _{THL} / t _{TLH}	output transition time	24	5	12		15		18	ns	4.5	Fig. 6	7
tw	clock pulse width HIGH or LOW	23	14	0.6	29	8.6	35	81 n	ns	4.5	Fig. 6	
t _{su}	set-up time D _n to CP	12	4	24	15	82	18	38 2	ns	4.5	Fig. 8	XAIT
th	hold time D _n to CP	5	-1		5		5		ns	4.5	Fig. 8	
f _{max}	maximum clock pulse frequency	22	36		18		15		MHz	4.5	Fig. 6	

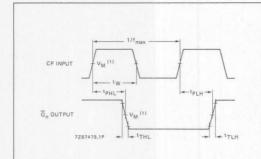


Fig. 6 Waveforms showing the clock (CP) to output $(\overline{\Omega}_n)$ propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

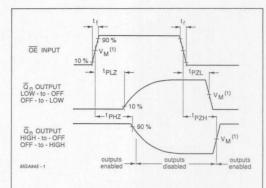


Fig. 7 Waveforms showing the 3-state enable and disable times.

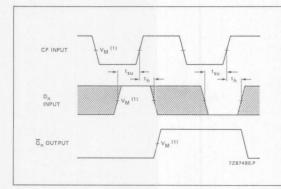


Fig. 8 Waveforms showing the data set-up and hold times for D_n input.

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

AC WAVEFORING



Fig. 8. (Weinform showing the stock (CE) to output (EL) propagation delays, the clock pates width, output transition times and the ris dimum. stock puter frequency.

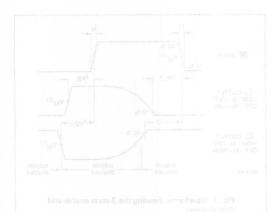


Fig. 8. Waveforms showing the date set-up and hold times for D₁₁ repn.

Note to Fig. 8 The shaded reas indicate when the input is cermitted to change for gredictable output serformence.

Note to AC varietisms $(1) \ HC + V_M = 50\%; V_1 = 6MD \text{ to } V_{10}C$ $(0) \ HC + V_M = 18 \ V_1V_1 = 6MD \text{ to } 3 \ V_2 = 18 \ V_1V_2 = 6MD \text{ to } 3 \ V_2 = 18 \ V_2 = 18$

OCTAL BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- Inverting outputs
- Output capability: bus driver
- · ICC category: MSI

has inverting outputs.

GENERAL DESCRIPTION

The 74HC/HCT540 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT540 are octal inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs \overline{OE}_1 and \overline{OE}_2 . A HIGH on \overline{OE}_n causes the outputs to assume a high impedance OFF-state. The "540" is identical to the "541" but

	FUNCTION TABLE	001101710110	TYF			
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT	
tPHL/	propagation delay A_n to \overline{Y}_n	C _L = 15 pF V _{CC} = 5 V	9	11	ns	
CI	input capacitance	₹2.1e	3.5	3.5	pF	
C _{PD} power dissipation capacitance per buffer		notes 1 and 2	39	44	pF	

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

f; = input frequency in MHz f_O = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

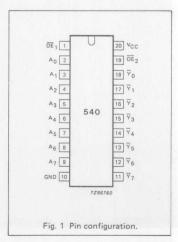
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

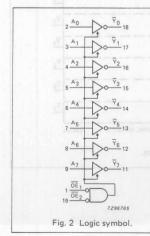
PACKAGE OUTLINES

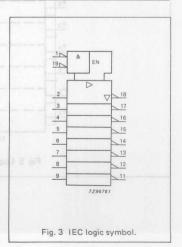
20-lead DIL: plastic (SOT146). 20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	
1, 19	$\overline{OE}_1, \overline{OE}_2$	output enable input (active LOW)	
2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₇	data inputs	
10	GND	ground (0 V)	
18, 17, 16, 15, 14, 13, 12, 11	∇ ₀ to ∇ ₇	bus outputs	
20	Vcc	positive supply voltage	







1 OE 19 OE 2

7296764 Fig. 4 Functional diagram.

FUNCTION TABLE

	INPUTS	OUTPUT	
ŌĒ ₁	ŌĒ ₂	An	\overline{Y}_{n}
L	LOY	o LA	H
L	and Lorenz	n.H.	L
X	Н	X	Z
H	X	X	Z

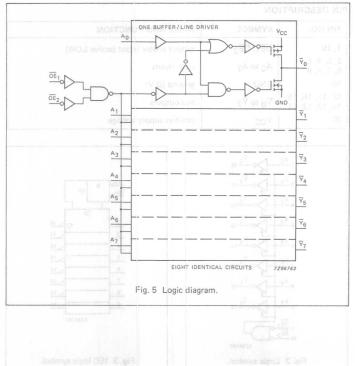
H = HIGH voltage level

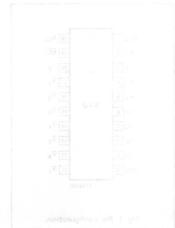
L = LOW voltage level

X = don't care

Z = high impedance OFF-state

	INPUTS	OUTPUT	
ŌĒ ₁	ŌĒ ₂	An	\overline{Y}_{n}
L	LATE	o LA	H
L	andlosas	n.H.	L
X	Н	X	Z
Н	X	X	Z





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", see collaboration of the DC characteristics and the DC characteristics are chapter to the DC characteristics and the DC characteristics are chapter to the DC characteristics and the DC characteristics are chapter to the DC characteristics are chapter to the DC characteristics.

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC

	T _{amb} (°C)								TEST CONDITIONS		
	74HC								1.0	BIDIRABUD	
PARAMETER	+25		-40 to +85 -40		-40 to	-40 to +125		VCC	WAVEFORMS		
	min.	typ.	max.	min.	max.	min.	max.				
propagation delay $A_n \text{ to } \overline{Y}_n$		30 11 9	100 20 17		125 25 21		150 30 26	ns ag	2.0 4.5 6.0	Fig. 6	
3-state output enable time $\overline{\text{OE}}_n$ to \overline{Y}_n		52 19 15	160 32 27	of) at	200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7	
3-state output disable time $\overline{\text{OE}}_n$ to \overline{Y}_n	125 165 165 1	61 22 18	160 32 27	or ()&	200 40 34	+25 yp. m	240 48 41	ns	2.0 4.5 6.0	Fig. 7	
output transition time	38	14 5 4	60 12 10	8	75 15 13	3 2	90 18 15	ns	2.0 4.5 6.0	Fig. 6	
ns 4.5 Fig. 7	€6			10		2 3		Tomic of	don's r	thZH, Ce th to A th	
	$\begin{array}{c} A_n \ to \ \overline{Y}_n \\ \\ \hline 3\text{-state output enable time} \\ \hline OE_n \ to \ \overline{Y}_n \\ \\ \hline 3\text{-state output disable time} \\ \hline OE_n \ to \ \overline{Y}_n \\ \\ \hline \text{output transition time} \end{array}$	$\begin{array}{c} \text{min.} \\ \\ \text{propagation delay} \\ A_n \text{ to } \overline{Y}_n \\ \\ \\ \text{3-state output enable time} \\ \\ \overline{OE}_n \text{ to } \overline{Y}_n \\ \\ \\ \text{3-state output disable time} \\ \\ \overline{OE}_n \text{ to } \overline{Y}_n \\ \\ \\ \text{output transition time} \\ \\ \end{array}$	$ \begin{array}{c c} +25 \\ \hline \text{min.} & \text{typ.} \\ \hline \\ \text{propagation delay} \\ A_n \text{ to } \overline{Y}_n \\ \hline \\ 3\text{-state output enable time} \\ \hline \\ \overline{OE}_n \text{ to } \overline{Y}_n \\ \hline \\ 3\text{-state output disable time} \\ \hline \\ \overline{OE}_n \text{ to } \overline{Y}_n \\ \hline \\ \text{output transition time} \\ \hline \\ \end{array} $	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$							

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". and advantage and a CO entraction of the DC characteristics are chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
OE ₁	1.50 VAW 3
OE ₂	1.00
An	1.40

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_1 = 50 \ pF$

SYMBOL PARAMETER 0,0 0,0 0,0 0,0 0,0 0,0 0,0 0,0 0,0 0,		52 180 (2°) dmbTo 240						amit a	dens t	TEST CONDITIONS		
			74HCT						UNIT	.,	WAVEFORMS	7263
		240	085 +25 00		-40 to +85		-40 to +125		amil e	V _C C	WAVEFORMS	
	min.	typ.	max.	min.	max.	min.	max.					
t _{PHL} /	propagation delay A_n to \overline{Y}_n	06 81	13	24		30	18 4	36	ns _{9.0}	4.5	Fig. 6	LIHIT!
t _{PZH} /	3-state output enable time $\overline{\text{OE}}_n$ to \overline{Y}_n		22	35		44		53	ns	4.5	Fig. 7	
t _{PHZ} /	3-state output disable time $\overline{\text{OE}}_n$ to \overline{Y}_n		23	35		44		53	ns	4.5	Fig. 7	
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6	

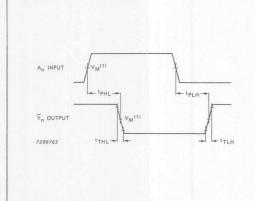


Fig. 6 Waveforms showing the input (A_n) to output (\overline{Y}_n) propagation delays and the output transition times.

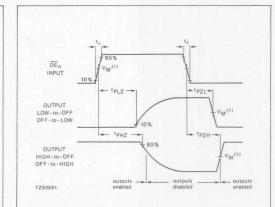


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

ALL WALL EFTORMS





Acte to AC worthing (4) PC - 12 V CC (4) PC CC (4) V CC (

OCTAL BUFFER/LINE DRIVER: 3-STATE

FEATURES

- Non-inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

has non-inverting outputs.

The 74HC/HCT541 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT541 are octal noninverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs OE₁ and OE₂. A HIGH on \overline{OE}_n causes the outputs to assume a high impedance OFF-state. The "541" is identical to the "540" but

SYMBOL	FUNCTION TABLE	CONDITIONS	TYF	LIBILT	
	PARAMETER	CONDITIONS	НС	нст	UNIT
t _{PHL} /	propagation delay A _n to Y _n	C _L = 15 pF V _{CC} = 5 V	10	12	ns
C _I	input capacitance	18 22	3.5	3.5	pF
C _{PD} power dissipation capacitance per buffer		notes 1 and 2	37	39	pF

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

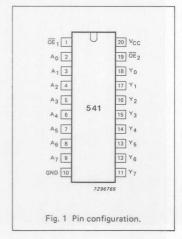
- 1. CPD is used to determine the dynamic power dissipation (P_D in μW): PD = CPD \times VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:
 - f; = input frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V
 - fo = output frequency in MHz $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is VI = GND to VCC For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 V$

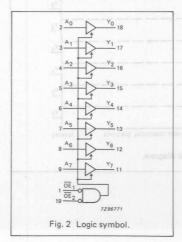
PACKAGE OUTLINES

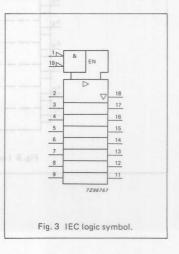
20-lead DIL: plastic (SOT146). 20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	OE ₁ , OE ₂	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₇	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	Y ₀ to Y ₇	bus outputs
20	Vcc	positive supply voltage







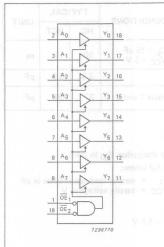


Fig. 4 Functional diagram.

FUNCTION TABLE

	OUTPUT		
OE ₁	ŌE ₂	An	Yn
L	L nY	27 E	LHUR
L	- Lacre	H	H
X	Н	X	Z
H	X	X	Z

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

ONE BUFFER/LINE DRIVER

VCC

Y0

Y0

Y1

Y2

Y3

Y4

Y4

Y6

Y7

EIGHT IDENTICAL CIRCUITS

7286768

Fig. 5 Logic diagram.

SERUTAGE

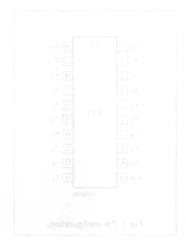
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MORTH I DESCRIPTION

The 2000 CEP1 are high-specifi-gate CNITS decreased are pin depart. CNITS decreased are pin of manufactured with law power Schottky. The Lost TLD They are specified in one, and the specified in one, the Squick State of the State of the State of the State or the state of the State of the State or the specified are of the specified are of SE, and SE2.

NAME of the STATE of the State or the cultipute to SE2 and the specified of the STATE. The STATE of the STA



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

				T _{amb} (°C)				1	TEST CONDITIO	NS	
					74H	С					COEPFICIENT	
SYMBOL	PARAMETER +25 -40 to +85 -40 to +125	UNIT	VCC	WAVEFORMS	100							
		min.	typ.	max.	min.	max.	min.	max.				nA
t _{PHL} /	propagation delay A _n to Y _n		33 12 10	115 23 20	(rain	145 29 25		175 35 30	ns	2.0 4.5 6.0	Fig. 6	
t _{PZH} /	3-state output enable time $\overline{\text{OE}}_{\text{n}}$ to Y_{n}	U	55 20 16	160 32 27	T	200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7	JOSMY
t _{PHZ} /	$\frac{3\text{-state}}{\overline{\text{OE}}_n}$ to $\frac{Y_n}{X_n}$	8	61 22 18	160 32 27	28+ 01 xem	200 40 34	xsm	240 48 41	ns	2.0 4.5 6.0	Fig. 7	
t _{THL} /	output transition time	in .	14	60 12	35	75 15	28	90 18	ns	2.0 4.5	Fig. 6	HI4
TLH	T.gi7 3.h		4	10	44	13	35	15	smi	6.0	Satate output I	/1924

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", and see that the section of the secti

Output capability: bus driver ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
ŌĒ1	1.50
OE ₂	1.00
An	0.70

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

			T _{amb} (°C)							TEST CONDITIONS		
SYMBOL PAR		+25			74HCT 00			UNIT	Vcc	WAVEFORMS		
	PARAMETER 0.0				-40 to +85		-40 to +125			V	WAVEFORINS	
	4.5 Fig. 7 6.0	min.	typ.	max.	min.	max.	min.	max.	nmn	Plantil		
t _{PHL} /	propagation delay	en	15	28	75	35	60	42	ns	4.5	Fig. 6	
t _{PZH} /	3-state output enable time $\overline{\text{OE}}_n$ to Y_n		21	35	21	44	01-1	53	ns	4.5	Fig. 7	
t _{PHZ} / t _{PLZ}	3-state output disable time $\overline{\text{OE}}_n$ to Y_n		21	35		44		53	ns	4.5	Fig. 7	
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6	

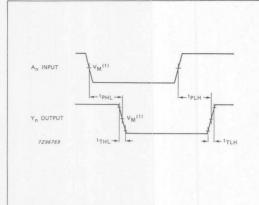


Fig. 6 Waveforms showing the input (A_n) to output (Y_n) propagation delays and the output transition times.

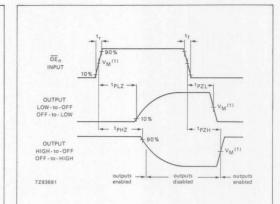
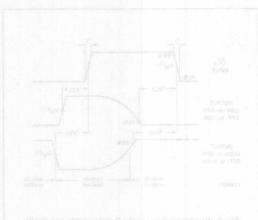


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.





Note to AC waveforms.

(1) HC.: V_{IM} = 50%; V_I = GND to V_{CC}.
HCT: V_{IM} = 1.3 V; V_{IM} GND to 3 V.

OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE; INVERTING

FEATURES

- 3-state inverting outputs for bus oriented applications
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessor
- Common 3-state output enable input
- · Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT563 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT563 are octal D-type transparent latches featuring separate D-type inputs for each latch and inverting 3-state outputs for bus oriented applications.

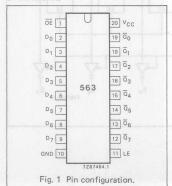
A latch enable (LE) input and an output enable (OE) input are common to all

The "563" is functionally identical to the "573", but has inverted outputs.

The "563" consists of eight D-type transparent latches with 3-state inverting outputs. The LE and $\overline{\text{OE}}$ are common to all latches.

When LE is HIGH, data at the D_{D} inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{\text{OE}}$ is LOW, the contents of the 8 latches are available at the outputs. When $\overline{\text{OE}}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{\text{OE}}$ input does not affect the state of the latches.



SYMBOL	212115	CONDITIONS	TYF	LINIT	
	PARAMETER	CONDITIONS	нс	НСТ	UNIT
tPHL/	propagation delay D_n , LE to \overline{Q}_n	C _L = 15 pF V _{CC} = 5 V	14	16	ns
CI	input capacitance	TUSTUS 8 m f	3.5	3.5	pF
C _{PD}	power dissipation capacitance per latch	notes 1 and 2	19	19	pF

$$GND = 0 \text{ V; } T_{amb} = 25 \, ^{\circ}\text{C; } t_r = t_f = 6 \text{ ns}$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$$
 where:

f_i = input frequency in MHz f_o = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

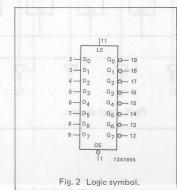
 Σ (C_L x V_{CC}² x f₀) = sum of outputs 2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} - 1.5 V

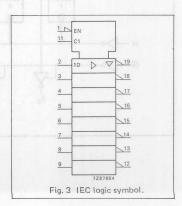
PACKAGE OUTLINES

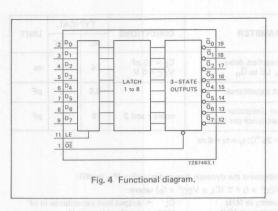
20-lead DIL; plastic (SOT146). 20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	D ₀ to D ₇	data inputs
11	LE	latch enable input (active HIGH)
1	ŌĒ	3-state output enable input (active LOW)
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12	$\overline{\mathbb{Q}}_0$ to $\overline{\mathbb{Q}}_7$	3-state latch outputs
20	Vcc	positive supply voltage







FUNCTION TABLE

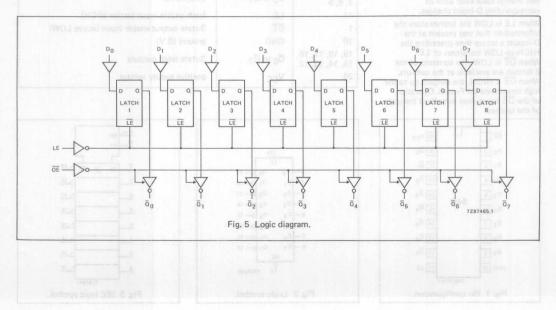
ODED ATIMO MODES	11	IPUT	S	INTERNAL	OUTPUTS
OPERATING MODES	ŌĒ	LE	Dn	LATCHES	$\overline{\mathbb{Q}}_0$ to $\overline{\mathbb{Q}}_7$
enable and read register	L	Н	L H	L HASSE	H.(S)
latch and read register	L	L L	l h	L H	H L
latch register and disable outputs	Н	L L	h	H H	Z Z

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE L = LOW voltage level

I = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition

Z = high impedance OFF-state



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

					T _{amb} (°C)			F	MAN.	TEST CONDIT	IONS
OVANDOL DADAMETED		74HC						LINUT	тивк	WAVEFORMS		
SYMBOL	PARAMETER	+25		-40 to +85		-40 to +125		UNIT	VCC	0.35		
		min.	typ.	max.	min.	max.	min.	max.			0.85 0.85 0E 1.25	
t _{PHL} /	propagation delay D_n to \overline{Q}_n		47 17 14	145 29 25		180 36 31		220 44 38	ns TOHM	2.0 4.5 6.0	Fig. 6	CHARA
t _{PHL} /	propagation delay LE to \overline{Q}_{Π}		47 17 14	145 29 25	10°1 _d	180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7	V 0 = 0 V
t _{PZH} /	3-state output enable time $\overline{\text{OE}}$ to $\overline{\text{Q}}_{\text{D}}$	125	47 17 14	150 30 26	TOHI For O	190 38 33	85	225 45 38	ns	2.0 4.5 6.0	Fig. 8	TOHMA
t _{PHZ} /	3-state output disable time $\overline{\text{OE}}$ to $\overline{\text{O}}_{\text{D}}$.XEE	50 18 14	150 30 26	m ai	190 38 33	an Jan	225 45 38	ns	2.0 4.5 6.0	Fig. 8	Vius
t _{THL} / t _{TLH}	output transition time	62	14 5 4	60 12 10		75 15 13	8 38	90 18 15	ns	2.0 4.5 6.0	Fig. 6	/JH4
t _W	enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	72.d /HZd
t _{su}	set-up time D _n to LE	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 9	PH2/ PLZ THI/
^t h	hold time D _n to LE	4 4 4	-6 -2 -2	2	4 4 4	2	4 4 4	81	ns	2.0 4.5 6.0	Fig. 9	HJT

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D _n	0.35
LE	0.65
ŌĒ	1.25

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)				TEST CONDITIONS		
	PARAMETER	06 74HCT 08 1 VI						UNIT	ite, est	WAVEFORMS		
SYMBOL	PARAMETER	8	+25		-40	to +85	-40 to	o +125	UNII	V _{CC}	WAVEFORWS	
		min.	typ.	max.	min.	max.	min.	max.	80 [1] 3		A Segreta dyrion	
t _{PHL} /	propagation delay D_n to $\overline{\Omega}_n$	81	18	30	35	38	4 26 8 60	45	ns	4.5	Fig. 6	
t _{PHL} /	propagation delay LE to $\overline{\mathbb{Q}}_n$	8	19	35	11	44	12	53	ns	4.5	Fig. 7	
t _{PZH} /	3-state output enable time $\overline{\text{OE}}$ to $\overline{\text{O}}_{n}$		20	35	00	44	1	53	ns	4.5	Fig. 8	
t _{PHZ} / t _{PLZ}	3-state output disable time \overline{OE} to $\overline{\mathbb{Q}}_n$		22	35		44	1	53	ns	4.5	Fig. 8	
^t THL [/] ^t TLH	output transition time		5	12		15	a-	18	ns	4.5	Fig. 6	
tw	enable pulse width HIGH	16	5	P E	20	4	24	- B	ns	4.5	Fig. 7	
t _{su}	set-up time D _n to LE	10	3		13		15		ns	4.5	Fig. 9	
th	hold time D _n to LE	5	-1		5		5		ns	4.5	Fig. 9	

AC WAVEFORMS

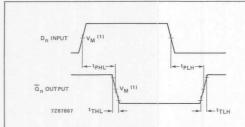


Fig. 6 Waveforms showing the data input (D_n) to output ($\overline{\rm O}_{\rm n}$) propagation delays and the output transition times.

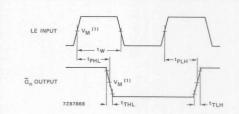


Fig. 7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output $(\overline{\Omega}_n)$ propagation delays and the output transition times.

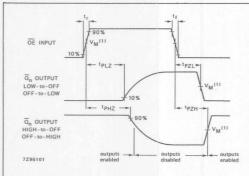


Fig. 8 Waveforms showing the 3-state enable and disable times.

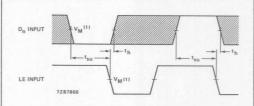


Fig. 9 Waveforms showing the data set-up and hold times for D_n input to LE input

Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

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OCTAL D-TYPE FLIP-FLOP; POSITIVE-EDGE TRIGGER; 3-STATE; INVERTING

FEATURES

- 3-state inverting outputs for bus oriented applications
- 8-bit positive-edge triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT564 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT564 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable (OE) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition. When OE is LOW, the contents of the 8 flip-flops are available at the outputs. When OE is HIGH, the outputs go to the high impedance OFF-state. Operation of the OE input does not affect the state of the flip-flops.

The "564" is functionally identical to the "574", but has inverting outputs. The "564" is functionally identical to the "534", but has a different pinning.

O)/MPOI	PUNCTION TABLE	CONDITIONS	TYP	UNIT		
SYMBOL	PARAMETER	CONDITIONS	нс	нст	ONT	
t _{PHL} /	propagation delay \square CP to $\overline{\Omega}_n$	C _L = 15 pF V _{CC} = 5 V	15 127	16 62	ns	
f _{max}	maximum clock frequency	A CC = 2 A			MHz	
CI	input capacitance	ar gii	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	27	27	pF	

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

PD = CPD \times VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

f; = input frequency in MHz fo = output frequency in MHz

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is VI = GND to VCC

VCC = supply voltage in V

CL = output load capacitance in pF

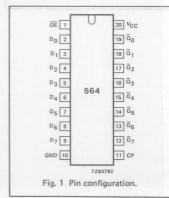
For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 \text{ V}$

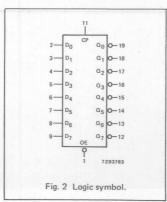
PACKAGE OUTLINES

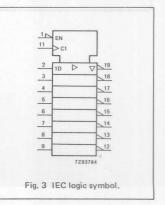
20-lead DIL; plastic (SOT146). 20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	ŌĒ	3-state output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D ₀ to D ₇	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
19, 18, 17, 16, 15, 14, 13, 12	$\overline{\Omega}_0$ to $\overline{\Omega}_7$	3-state flip-flop outputs
20	Vcc	positive supply voltage







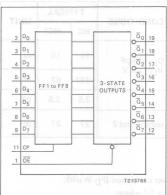


Fig. 4 Functional diagram.

FUNCTION TABLE

ODED ATIMO MODEO		INPUTS		INTERNAL	OUTPUTS	
OPERATING MODES	ŌĒ	СР	D _n	FLIP-FLOPS	$\overline{\mathbb{Q}}_0$ to $\overline{\mathbb{Q}}_7$	
load and read register	L L	†	l sis	renime <mark>gand 3 st</mark> rion H	nego Lini	
load register and disable outputs	H	†	l h	L 18M V	Z Z	

H = HIGH voltage level

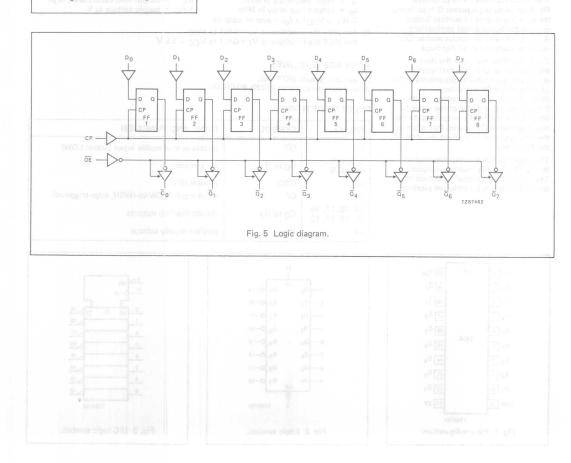
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

Z = high impedance OFF-state

↑ = LOW-to-HIGH clock transition



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pFd eldet adt ni novora tomoritoro basel time

					T _{amb} (°C)					TEST CONDITIO	ONS
OVMOOL	DADAMETED	74HC							,	WAVEFORMS		
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			1.00	
t _{PHL} /	propagation delay CP to $\overline{\Omega}_{n}$		50 18 14	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 6	
t _{PZH} /wo	3-state output enable time $\overline{\text{OE}}$ to $\overline{\text{O}}_n$		44 16 13	140 28 24	(0°)	175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8	
t _{PHZ} /	3-state output disable time \overline{OE} to $\overline{\mathbb{Q}}_n$	25	50 18 14	135 27 23	+ 07 0	170 34 29	es	205 41 35	ns	2.0 4.5 6.0	Fig. 8	YMBOL
t _{THL} /	output transition time	1	14 5 4	60 12 10	44	75 15 13	38	90 18 15	ns	2.0 4.5 6.0	Fig. 6	/JHs
tw	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20	er .	ns	2.0 4.5 6.0	Fig. 6	HZe /HZe
t _{su}	set-up time D _n to CP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7	PHZ/ PLZ THL/
t _h	hold time D _n to CP	5 5 5	0 0 0	27	5 5 5	23	5 5 5	8 8	ns	2.0 4.5 6.0	Fig. 7 (50/5	HIT
f _{max}	maximum clock pulse frequency	6.0 30 35	38 115 137	Bì	4.8 24 28	ar	4.0 20 24	2 3	MHz	2.0 4.5 6.0	Fig. 6	DE

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
OE	0.80
D ₀ to D ₇	0.25
CP	1.00

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

	8.01 Fig. 8				T _{amb} (°C)		31		ddano	TEST CONDITIONS
		0.8		74HCT							
SYMBOL	4.6 Fig. 8		+25		-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS
-		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} /	propagation delay CP to $\overline{\Omega}_{\Pi}$		19	35	13	44	31 i	53	ns	4.5	Fig. 6
t _{PZH} /	3-state output enable time $\overline{\text{OE}}$ to $\overline{\Omega}_n$		19	35		44		53	ns	4.5	Fig. 8
t _{PHZ} /	3-state output disable time $\overline{\text{OE}}$ to $\overline{\Omega}_n$		19	30		38		45	ns	4.5	Fig. 8
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6
t _W	clock pulse width HIGH or LOW	18	8	8	23	8	27	0	ns	4.5	Fig. 6
t _{su}	set-up time Dn to CP	12	3	4.0 20	15	4.8	18	(E) (E)	ns	4.5	Fig. 7
th	hold time D _n to CP	3	-2	992	3		3	LL."	ns	4.5	Fig. 7
f _{max}	maximum clock pulse frequency	27	56		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

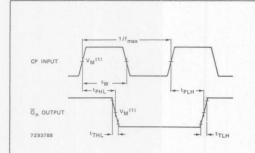


Fig. 6 Waveforms showing the clock (CP) to output $(\overline{\Omega}_n)$ propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

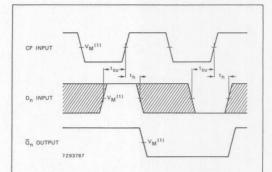


Fig. 7 Waveforms showing the data set-up and hold times for the data input $(D_{\rm n})$.

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

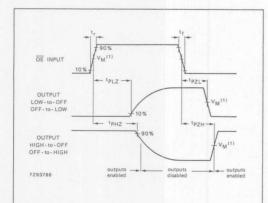


Fig. 8 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

AC WAVEFORIVE

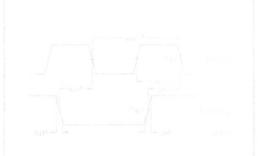


Fig. 5. Receiving showing the clock (CP) to output (Ω_n) prove than deady, the curving pulse width, the output transfer at times and the maximum clock pulse frequency.



Fig. 7. Waveforms showing the data set-up and hold time for the data input (Ω_{Ω}) .

Ninte to Fig. 7

The shaded areas indicers when the input is permitted to change for predictable output performance.



Fig. 6. waveforce showing the 3 state enable and disable times.

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HCT: VM - 60%; VI = GND to VCC.

OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE

FEATURES OF THE PROPERTY OF TH

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors/microcomputers
- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the "563" and "373"
- Output capability: bus driver
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT573 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT573 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable (OE) input are common to all latches.

The "573" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{\text{OE}}$ is LOW, the contents of the 8 latches are available at the outputs. When $\overline{\text{OE}}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{\text{OE}}$ input does not affect the state of the latches. *(continued on next page)*

OE 1	U	20 VCC
D ₀ 2		19 00
D ₁ 3		18 Q ₁
D ₂ 4		17 Q ₂
D ₃ 5	570	16 Q3
D ₄ 6	573	15 Q ₄
D ₅ 7		14 Q ₅
D ₆ 8		13 Q ₆
D ₇ 9		12 Q ₇
GND 10		11 LE
GND 10	7Z878	

SYMBOL		CONDITIONS	TYF	UNIT		
	PARAMETER	CONDITIONS	НС	нст	CIVII	
t _{PHL} /	propagation delay D _n to Q _n LE to Q _n	C _L = 15 pF V _{CC} = 5 V	14 15	17 15	ns ns	
CI	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per latch	notes 1 and 2	26	26	pF	

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

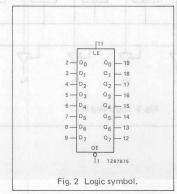
- fi = input frequency in MHz
- CL = output load capacitance in pF
- f_0 = output frequency in MHz VCC = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

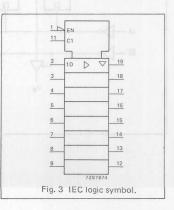
PACKAGE OUTLINES

20-lead DIL; plastic (SOT146). 20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	D ₀ to D ₇	data inputs
11 1	LE OE	latch enable input (active HIGH) 3-state output enable input (active LOW)
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12	Q ₀ to Q ₇	3-state latch outputs
20	VCC	positive supply voltage





01 18 3 D₁ 02 17 Q3 16 LATCH 3-STATE 04 15 6 D4 1 to 8 OUTPUTS 7 D₅ Q₅ 14 D₆ Q₆ 13 Q₇ 12 Fig. 4 Functional diagram. L. CPD is used to determine the dynam

GENERAL DESCRIPTION

The "573" is functionally identical to the "563" and "373", but the "563" has inverted outputs and the "373" has a different pin arrangement.

FUNCTION TABLE

OPERATING MODES	11	NPUT	rs	INTERNAL	OUTPUTS
OPERATING MODES	OE LE Dn		LATCHES	Q ₀ to Q ₇	
enable and read register (transparent mode)	L	Н	L. H	H H .(Ata)	L 2 1146).H c (5020, 501
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H	L L	d a	na bi <mark>l</mark> an	Z JOB

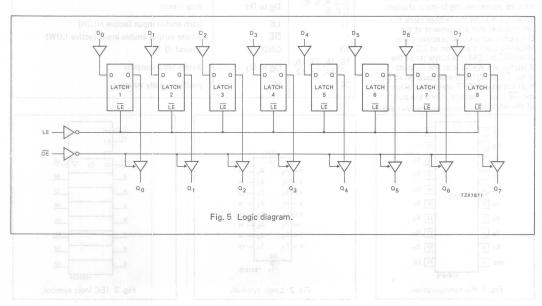
H = HIGH voltage level energy bine more lifes sof

prior to the HIGH-to-LOW LES bas Juan 1991 slast transition

L = LOW voltage level

L = LOW voltage level
L = LOW voltage level one set-up time
prior to the HIGH-to-LOW LE transition

Z = high impedance OFF-state



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC and add an energy of the best time and (2014) the rice yights the exemple fancishes to enter add. GND = 0.V: to = to = 6 no: Ct = 50 no.

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

					T _{amb} (°C)				CAR	TEST CONDITI	ONS
SYMBOL	PARAMETER				74H	С			UNIT	V	WAVEFORM	s go
SAMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	88.0 a. 1 a. 2	
		min.	typ.	max.	min.	max.	min.	max.				
^t PHL [/] ^t PLH	propagation delay D _n to Q _n		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6	
^t PHL [/]	propagation delay LE to O _n		50 18 14	150 30 26	(3") -6	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
tPZH/	3-state output enable time OE to Q _n	951	44 16 13	140 28 24	For Op	175 35 30	25	210 42 36	ns	2.0 4.5 6.0	Fig. 8	TORMA
t _{PHZ} /	3-state output disable time OE to Q _n	-X00	55 20 16	150 30 26	14	190 38 33	E 0	225 45 38	ns	2.0 4.5 6.0	Fig. 8	
tTHL/ tTLH	output transition time	81	14 5 4	60 12 10	4	75 15 13	8 38	90 18 15	ns	2.0 4.5 6.0	Fig. 6	
tW	enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	/ZH4 7Z8 /HZ8
t _{su}	set-up time D _n to LE	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 9	PLZ THL/ TLH
^t h	hold time B.M. Property of the LE	5 5 5	3 1 1	2	5 5 5	8	5 5 5	18	ns	2.0 4.5 6.0	Fig. 9	W
	ns 4.5 Fig. 9			15	1	91		13 7			Sepup drift Do to LE	613

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. Fig. 3.1 A A A A D A To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D _n 2M6	0.35 0.65 1.25

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V; } t_r = t_f = 6 \text{ ns; } C_L = 50 \text{ pF}$

		in 8			T _{amb} (°C)				delay	TEST CONDITION	S
01/14001	PARAMETER 0.5	0.0		3	74H	т	6 P E		UNIT	1/	WAVEFORMS	
SYMBOL	FARAMETER 555		+25		-40 to +85		-40 t	o +125	Oivii	V _{CC}	GIBO STORES	
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay D _n to Q _n	an 3- 81	20	35	38	44	95 9 95 9	53	ns	4.5	Fig. 6 10	PLZ
t _{PHL} /	propagation delay LE to Q _n	10 8 8	18	35	78	44	4 60	53	ns	4.5	Fig. 7	
t _{PZH} / t _{PZL}	3-state output enable time OE to Q _n		17 0	30	a	38	į.	45 08	ns	4.5	Fig. 8	
t _{PHZ} /	3-state output disable tim OE to Ω _n	е	18	30		38		45	ns	4.5	Fig. 8	
t _{THL} / t _{TLH}	output transition time	a l	5	12		15		18	ns	4.5	Fig. 6	E/B
t _W	enable pulse width HIGH	16	5	W 68 00	20	8 . 8	24	5 S	ns	4.5	Fig. 7	d
t _{su}	set-up time D _n to LE	13	7		16		20		ns	4.5	Fig. 9	
t _h	hold time D _n to LE	9	4		11		14		ns	4.5	Fig. 9	

AC WAVEFORMS

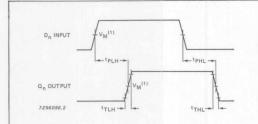


Fig. 6 Waveforms showing the data input (D_n) to output (Q_n) propagation delays and the output transition times.

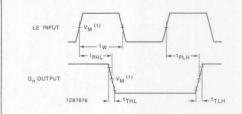


Fig. 7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Ω_n) propagation delays and the output transition times.

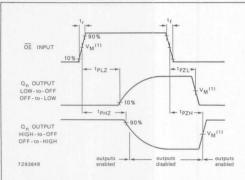


Fig. 8 Waveforms showing the 3-state enable and disable times.

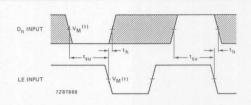


Fig. 9 Waveforms showing the data set-up and hold times for $\mathsf{D}_{\mathsf{\Pi}}$ input to LE input.

Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.









OCTAL D-TYPE FLIP-FLOP; POSITIVE EDGE-TRIGGER; 3-STATE

FEATURES

- 3-state non-inverting outputs for bus oriented applications
- 8-bit positive edge-triggered register
- Common 3-state output enable input
 Independent register and 3-state
- buffer operation
- Output capability: bus driver
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT574 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT574 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and non-inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable (OE) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.
When \overline{OE} is LOW, the contents of the 8 flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

The "574" is functionally identical to the "564", but has non-inverting outputs. The "574" is functionally identical to the "374", but has a different pinning.

OVANDO	. FUNCTION TABLE	CONDITIONS	TYP	LIMIT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
t _{PHL} /	propagation delay CP to Ω _n	C _L = 15 pF	14	15	ns
f _{max}	maximum clock frequency	V _{CC} = 5 V	123	76	MHz
CI	input capacitance	SISTATE OUTPUTS OR 15	3.5	3.5	pF
C _{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	22	25	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes and an amelian and a series and about a

- 1. CPD is used to determine the dynamic power dissipation (PD in μ W):
 - $PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$ where:
 - f; = input frequency in MHz f_O = output frequency in MHz
 - VCC = supply voltage in V

CL = output load capacitance in pF

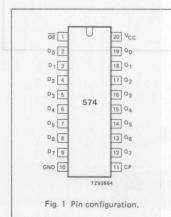
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} – 1.5 V

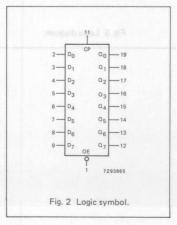
PACKAGE OUTLINES

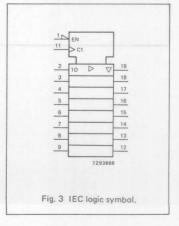
20-lead DIL; plastic (SOT146). 20-mini-pack; plastic (SO20; SOT163A).

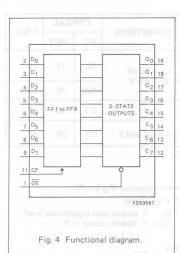
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 0	ŌĒ	3-state output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D ₀ to D ₇	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
19, 18, 17, 16, 15, 14, 13, 12	Q ₀ to Q ₇	3-state flip-flop outputs
20	VCC	positive supply voltage









FUNCTION TABLE

ODEDATING MODES		INPUTS	107.2	INTERNAL	OUTPUTS
OPERATING MODES	ŌĒ	q) CP	Dn	FLIP-FLOPS	Q ₀ to Q ₇
load and read	L N	1	l ald	Finale output ena H	Countrol :
load register and month disable outputs	H H	↑ C	l h	L souper	Z Z

H = HIGH voltage level

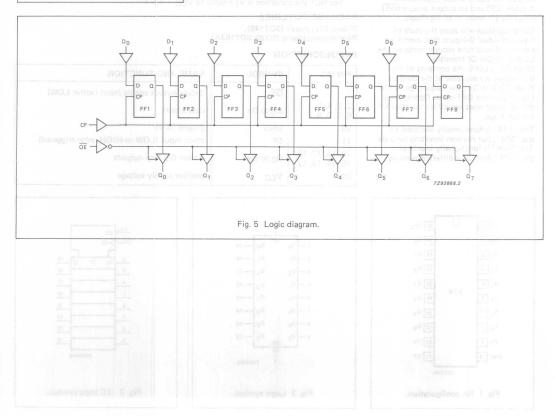
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

Z = high impedance OFF-state 2010//

1 = LOW-to-HIGH clock transition



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

					Tamb (°C)				TEST CONDITIONS		
0.440.01					74H0	:			LIBUT	110	V _{CC} WAVEFORMS	
SYMBOL	PARAMETER		+25		-40 1	to +85	-40 to	+125	UNIT			
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay CP to Q _n		47 17 14	150 30 26		190 35 33		225 45 38	ns Aq	2.0 4.5 6.0	Fig. 6	
t _{PZH} ///OT	3-state output enable time OE to Q _n		44 16 13	140 28 24	(0°) d	175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7	
t _{PHZ} /	3-state output disable time OE to Q _n	125	39 14 11	125 25 21	10 to 1	155 31 26	-25	190 38 32	ns	2.0 4.5 6.0	Fig. 7	
tTHL/ tTLH	output transition time	- 0	14 5 4	60 12 10	1-4	75 15 13	m Ay	90 18 15	ns	2.0 4.5 6.0	Fig. 6	/JH4
tw	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6	/HZ9
t _{su}	set-up time D _n to CP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8	LHT/
th	hold time D _n to CP	5 5 5	0 0	20	5 5 5	100	5 5 5	7 88	ns	2.0 4.5 6.0	Fig. 8 Apola	H3T
f _{max}	maximum clock pulse frequency	6.0 30 35	37 112 133	81	4.8 24 28		4.0 20 24	12 3	MHz	2.0 4.5 6.0	Fig. 6	w

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D _n	0.5
OE	1.25
CP	1.5

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_1 = 50 pF$

		n S	2		T _{amb} (°C)	88	31	lime	dano 1	TEST CONDITIONS	
	0.0	1 6			74HC	Т						
SYMBOL		8	88 +25		-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS	
	0.8	min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay CP to Q _n	8 8	18	33	21	41	12	50	ns	4.5	Fig. 6	
t _{PZH} /	3-state output enable time ΘE to Q _n	m	19	33	0	41		50	ns	4.5	Fig. 7	
t _{PHZ} /	3-state output disable time $\overline{\text{OE}}$ to Ω_{n}		16	28		35		42	ns	4.5	Fig. 7	
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6	
t _W	clock pulse width HIGH or LOW	16	7	8 5	20	8	24	0 6	ns	4.5	Fig. 6	
t _{su}	set-up time 0.5 D _n to CP	12	3	4.2	15	4.	18	E 0,0	ns	4.5	Fig. 8	
th	hold time D _n to CP	5	-1	22	5	82.	5	51 52	ns	4.5	Fig. 8	
f _{max}	maximum clock pulse frequency	30	69		24		20		MHz	4.5	Fig. 6	

AC WAVEFORMS

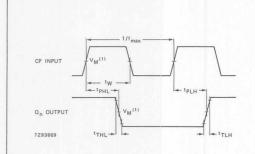


Fig. 6 Waveforms showing the clock input (CP) pulse width, the CP input to output (Ω_{Π}) propagation delays, the output transition times and the maximum clock pulse frequency.

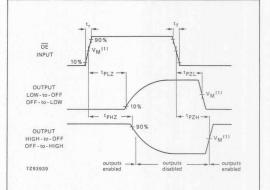


Fig. 7 Waveforms showing the 3-state enable and disable times. $\,$

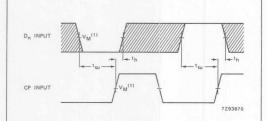


Fig. 8 Waveforms showing the data set-up and hold times for D_n input to CP input.

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

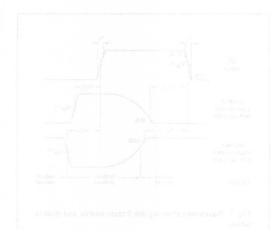
Note to AC waveforms

(1) HC : V_M = 50%; V_l = GND to V_{CC} . HCT: V_M = 1.3 V; V_l = GND to 3 V.

2M SCHEWALL DA



Fig. 3. We informs showing the cook input (CR) pulsewidth, the off-input relations for below. The majors of the major in all process and the maximum short pulse requires.





The shade whee shadoute when the input is permitted to a super early detable output performance.

our to AC waveforms

1 HO : Vig = 50%; Vj = CIND to Voc.

HOT Vig = 53V; Vj = CIND to Voc.

4-BIT FULL ADDER WITH FAST CARRY

FEATURES

- Adds two decimal numbers
- · Full internal look-ahead
- · Fast ripple carry for economical expansion
- · Output capability: standard
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT583 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JECEC standard no. 7A.

The 74HC/HCT583 are high-speed 4-bit BCD full adders with internal carry look-ahead. They accept two 4-bit decimal numbers (A₀ to A₃ and B₀ to B₃) and a carry input (CIN).

The "583" generates the decimal sum outputs (Σ_0 to Σ_3) and a carry output (C_{n+4}) if the sum is greater than 9.

If an addition of two BCD numbers produce a number greater than 9, a valid BCD number and a carry will result. For input values larger than 9, the number is converted from binary to BCD. Binary to BCD conversion occurs by grounding one set of inputs, An or Bn and applying a 4-bit binary number to the other set of inputs. If the input is between 0 and 9, a BCD number occurs at the output. If the binary input falls between 10 and 15, a carry term is generated. Both the carry term and the sum are the BCD equivalent of the binary input. Converting binary numbers greater than 16 may be achieved by cascading "583s".

See the "283" for the binary version.

SYMBOL	DADAMETER	CONDITIONS	TYP	LIBUT	
	PARAMETER	CONDITIONS	НС	нст	UNIT
^t PHL [/] ^t PLH	propagation delay C _{IN} to C _{n+4} A _n , B _n to C _{n+4}	C _L = 15 pF V _{CC} = 5 V	20 23	23 27	ns ns
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	116	120	pF

$$GND = 0 \text{ V}; T_{amb} = 25 \,^{\circ}\text{C}; t_r = t_f = 6 \text{ ns}$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

fi = input frequency in MHz fo = output frequency in MHz C_L = output load capacitance in pF V_{CC} = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is VI = GND to VCC For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 V$

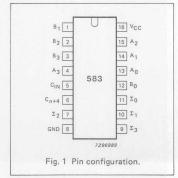
PACKAGE OUTLINES

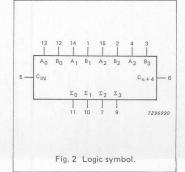
16-lead DIL; plastic (SOT38Z).

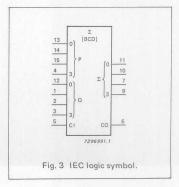
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

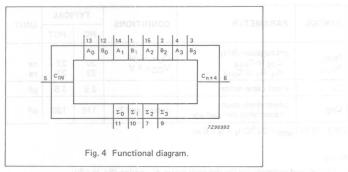
PIN NO.	SYMBOL	NAME AND FUNCTION	
5	CIN	carry input	
6	Cn+4	carry output	
8	GND	ground (0 V)	
11, 10, 7, 9	Σ_0 to Σ_3	sum outputs	
12, 1, 2, 3	B ₀ to B ₃	B operand inputs	
13, 14, 15, 4	A ₀ to A ₃	A operand inputs	
16	Vcc	positive supply voltage	







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in input in quancy in MHz $C_{\rm L} = {
m output}$ lead capacitation in pR $C_{\rm L} = {
m output}$ the quancy in MHz ${
m Vgc} = {
m supply yolthigh}$ in ${
m Vgc} = {
m vgc} \times {
m Vgc}^2 \times {
m I}_{\rm G} = {
m supply}$ and all outputs

Tech The condition is V) = GND to Vigg = 1.5 V

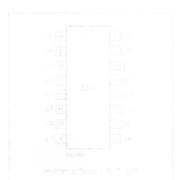
PRIMITION SEATON

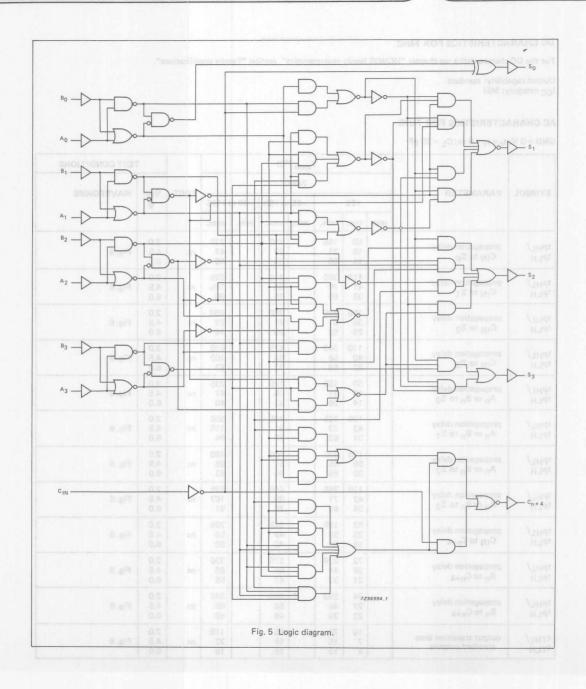
1811 or CH1; plastic (\$0738Z).

Girud : I'mi paolo plastic (SOTR) SOT (OSA)

MORTSHROSSILLSIE







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

		100			T _{amb} (°C)					TEST CONDITIONS	
0)/445.01					74H	С					WAVEFORMS	
SYMBOL	PARAMETER		+25		-40	to +85	-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay C_{1N} to Σ_0		50 18 14	155 31 26	F	195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} /	propagation delay C_{1N} to Σ_1		113 41 33	350 70 60		440 88 75		525 105 90	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} /	propagation delay C_{1N} to Σ_2		100 36 29	305 61 52		380 76 65		460 92 78	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} /	propagation delay C_{IN} to Σ_3		110 40 32	340 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} /	propagation delay A_n or B_n to Σ_0		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} /	propagation delay A_n or B_n to Σ_1		120 43 34	365 73 62		455 91 77		550 110 94	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay A_n or B_n to Σ_2		105 38 30	325 65 55		405 81 69		490 98 83	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} /	propagation delay A_n or B_n to Σ_3		116 42 34	355 71 60		445 89 76		535 107 91	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay C _{IN} to C _{n+4}		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay A _n to C _{n+4}		72 26 21	220 44 37	Ī	275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} /	propagation delay B _n to C _{n+4}	7.28431	74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 6	
t _{THL} /	output transition time standard outputs		19 7 6	75 15 13	gio dia	95 19 16	B	110 22 19	ns	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current $\{\Delta I_{CC}\}$ for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A _n , B _n	0.4

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)				TEST CONDITIONS		
CVMDOL	PARAMETER				74HC	т			UNIT	.,	WAVEFORMS	
SYMBOL	PARAMETER	+25			-40	to +85	-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay C _{IN} to Σ ₀		20	34		43		51	ns	4.5	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay C_{1N} to Σ_1		40	68		85		102	ns	4.5	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay C_{1N} to Σ_2		38	65		81		98	ns	4.5	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay C _{IN} to Σ ₃		38	65		81		98	ns	4.5	Fig. 6	
t _{PHL} /	propagation delay A_n or B_n to Σ_0		22	37		46		56	ns	4.5	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay A_n or B_n to Σ_1		43	73		91		110	ns	4.5	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay A_n or B_n to Σ_2		40	68		85		102	ns	4.5	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay A_n or B_n to Σ_3		41	70		88		105	ns	4.5	Fig. 6	
t _{PHL} /	propagation delay C _{IN} to C _{n+4}		27	46		58		69	ns	4.5	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay A _n to C _{n+4}		31	53		66		80	ns	4.5	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay B _n to C _{n+4}		30	51		64		77	ns	4.5	Fig. 6	
t _{THL} /	output transition time standard outputs		7	15		19		22	ns	4.5	Fig. 6	

AC WAVEFORMS

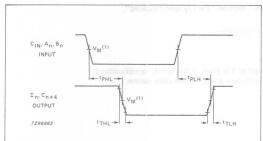


Fig. 6 Waveforms showing the inputs $(C_{IN},\,A_n,\,B_n)$ to the outputs $(\Sigma_n,\,C_{n+4})$ propagation delays and the output transition times.

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Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

74HC/HCT594

FEATURES

- Synchronous serial input and output
- · 8-bit parallel output
- Shift and storage register have independent direct clear and clocks
- 100 MHz (typ.)
- · Output capability:
 - parallel outputs: bus driver
 - serial outputs: standard
- I_{cc} category: MSI

APPLICATIONS

- Serial-to parallel data conversion
- · Remote control holding register

DESCRIPTION

The 74HC/HCT594 are high-speed, Si-gate CMOS devices, and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74HC/HCT594 contain an 8-bit, non-inverting, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clears are provided on both the shift and storage registers. A serial output (Q_7) is provided for cascading purposes.

Both the shift and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register will always be one count pulse ahead of the storage register.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25 \, ^{\circ}\text{C}$; $t_r = t_f = 6 \, \text{ns}$.

OVALDOL	DADAMETER	CONDITIONS	TYP	UNIT		
SYMBOL	PARAMETER	CONDITIONS	НС	НСТ	UNIT	
t _{PHL} /t _{PLH}	propagation delay	C _L = 15 pF; V _{CC} = 5 V	Of Land			
	SH _{CP} to Q ₇ '	V _{cc} = 5 V	13	15	ns	
	ST _{CP} to Q _n	symbol.	13	15	ns	
	SH _R to Q _n		11	14	ns	
	\overline{ST}_R to Q_n		11	14	ns	
f _{max}	maximum clock frequency SH _{CP} , ST _{CP}	ROSEO	100	100	MHz	
Cı	input capacitance	olumbus etch falleren	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	84	89	pF	

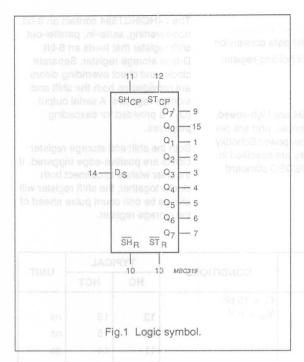
Notes

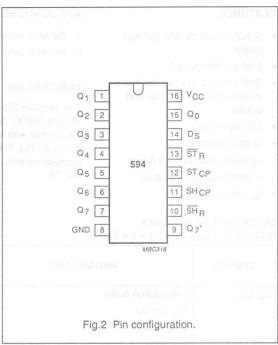
- C_{PD} is used to determine the dynamic power dissipation (P_D in μW). P_D = C_{PD} x V_{CC}² x f_i + Σ(C_L x V_{CC}² x f_o), where: f_i = input frequency in MHz;
 - fo = output frequency in MHz;
 - $\Sigma(C_1 \times V_{CC}^2 \times f_0) = \text{sum of the outputs};$
 - C₁ = output load capacitance in pF;
 - V_{cc} = supply voltage in V.
- 2. For HC, the condition is $V_1 = GND$ to V_{CC} .
 - For HCT, the condition is $V_1 = GND$ to $v_{CC} 1.5 V$.

ORDERING INFORMATION

EXTENDED TYPE	PACKAGES									
NUMBER	PINS	PIN POSITION	MATERIAL	CODE						
PC74HC/HCT594P	16	DIL	plastic	SOT38C, P						
PC74HC/HCT594T	16	SO	plastic	SOT109A						

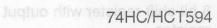
74HC/HCT594

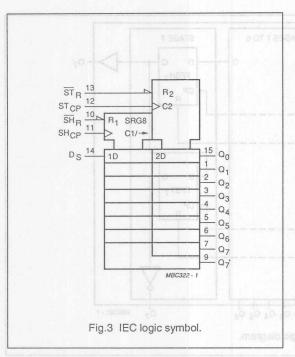


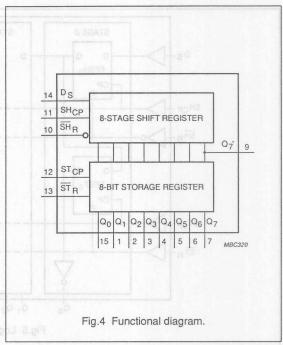


PINNING

SYMBOL	PIN	DESCRIPTION	men clock frequen
Q ₀ to Q ₇	15 & 1 to 7	parallel data outputs), nou capacitance
GND	8	ground (0 V)	Compressipation cap
Q ₇ '	9	serial data output	zato.
SH _R	10	shift register reset (active LOW)	
SH _{CP}	11	shift register clock input	C _{PO} is used to determine the dynamic t = beautismuse of an MHz;
ST _{CP}	12	storage register clock input	(= subject the gual ox in MHz;
STR	13	storage register reset active (LOW)	X(C, Y, X, X, + sum of the olupute
Ds	14	serial data input	C _L = nutper lase expacitance in pE _L
V _{cc}	16	supply voltage	V _{oc} = supply vollage in V. For IC, one condition is V _i = GND to







FUNCTION TABLE

		INPUT	S		OUT	PUTS	FUNCTION TO SOME						
SH _{CP}	ST _{CP}	SHR	STR	Ds	Q,'	Q _n	FUNCTION						
X	X	L	X	X	L	NC	a LOW level on SH _R only affects the shift registers.						
X	X	X	L	X	NC	L	a LOW level on \overline{ST}_R only affects the storage registers.						
X	1	L	Н	X	L	L	empty shift register loaded into storage register.						
1	X	Н	X	Н	Q ₆ '	NC	logic HIGH level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q_6 ') appears on the serial output $(Q_7$ ').						
X	1	Н	Н	X	NC	Q _n '	contents of shift register stages (internal Q_n) are transferred to the storage register and parallel output stages.						
1	1	Н	Н	X	Q ₆ n	Q _n '	contents of shift register shifted through. Previous contents of shift register transferred to the storage register and the parallel output stages.						

H = HIGH voltage level

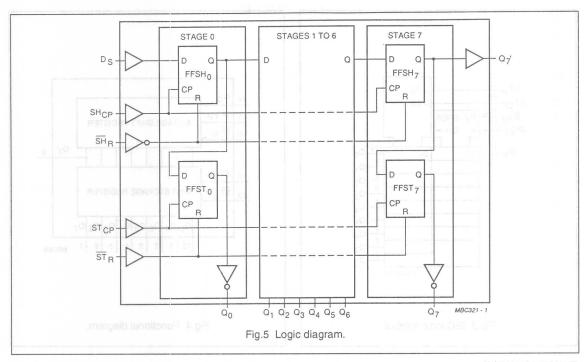
L = LOW voltage level

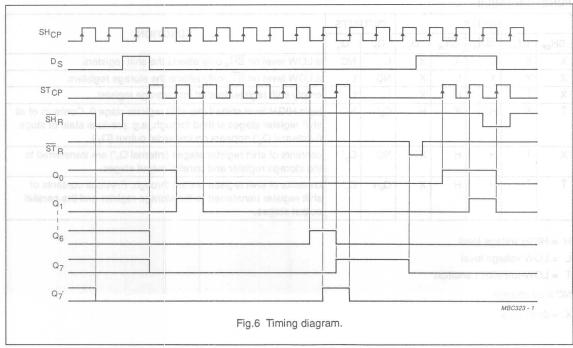
1 = LOW-to-HIGH transition

NC = no change

X = don't care.

74HC/HCT594





74HC/HCT594

DC CHARACTERISTICS FOR 74HC

For the DC characteristics, see chapter 'HCMOS family characteristics', section 'Family specifications'.

Output capability: parallel outputs, bus driver; serial output, standard.

Icc category: MSI.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_t = 6 \text{ ns}$; $C_L = 50 \text{ pF}$.

	0.S zn -	7.5		65	T _{amb} (°C	()			emit la		TEST IDITIONS
SYMBOL	PARAMETER	e+	+25	FF	-40 1	to +85	-40 t	0 +125	UNIT	V _{cc}	WAVE-
	- MHz 2.0	MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	olo mu	(V)	FORMS
t _{PHL} /t _{PLH}	propagation delay	(2)	44	150	-	185	æ	225	ns (2.0	Fig.7
	SH _{CP} to Q ₇ '	12	16	30	- 1	37	88	45	ns	4.5	
		-	14	26	-	31	-	38	ns	6.0	
	propagation delay	-	44	150	-	185	-	225	ns	2.0	Fig.8
	ST _{CP} to Q _n	-	16	30	-	37	-	45	ns	4.5	
		-	14	26	-	31	-	38	ns	6.0	
t _{PHL}	propagation delay	-	39	150	-	185	-	225	ns	2.0	Fig.11
	SH _R to Q ₇ '	-	14	30	-	37	-	45	ns	4.5	
		-	12	26	-	31	-	38	ns	6.0	
	propagation delay	-	39	125	-	155	-	185	ns	2.0	Fig.12
	\overline{ST}_R to Q_n	-	14	25	-	31	-	37	ns	4.5	
		-	12	21	-	26	-	31	ns	6.0	
t _w	shift clock pulse width	80	10	-	100	-	120	-	ns	2.0	Fig.7
	HIGH or LOW	16	4	-	20	-	24	-	ns	4.5	
		14	3	-	17	-	20	-	ns	6.0	
	storage clock pulse	80	10	-	100	-	120	-	ns	2.0	Fig.8
	width HIGH or LOW	16	4	-	20	-	24	-	ns	4.5	
		14	3	-	17	-	20	-	ns	6.0	
	shift and storage reset	80	14	-	100	-	120	-	ns	2.0	Figs 11
	pulse width HIGH or LOW	16	5	-	20	-	24	-	ns	4.5	and 12
	LOVV	14	4	-	17	-	20	-	ns	6.0	
t _{su}	set-up time D _s to SH _{CP}	100	10	-	125	-	150	-	ns	2.0	Fig.9
		20	4	-	25	-	30	-	ns	4.5	
		17	3	-	21	-	26	-	ns	6.0	
	set-up time SH _R to ST _{CP}	100	14	-	125	-	150	-	ns	2.0	Fig.10
		20	5	-	25	-	30	-	ns	4.5	
		17	4	-	21	-	26	-	ns	6.0	
	set-up time	100	17	-	125	-	150	-	ns	2.0	Fig.8
	SH _{CP} to ST _{CP}	20	6	-	25	-	30	-	ns	4.5	
		17	5	-	21	-	26	-	ns	6.0	

74HC/HCT594

	,'an	oljeofic	ega ylın	tion Fan			T _{amb} (°C)			aoilah		TEST IDITIONS
SYMBOL	P	ARAME	ETER		+2	25	a Jun-4	0 to +85	-40	to +125	UNIT	V _{cc}	WAVE-
				MII	N. TY	P. MA	X. MIN	I. MAX	. MIN	. MAX.		(V)	FORMS
t _n	hold tin	ne D _s to	SH _{CP}	25 5 4	-8 -3 -2	-	30 6 5	-	6 –	35 7 6	- ns 4.5	4.5	Fig.9 Анано о
t _{remaldOFFIC}	remova SH _R to ST _R to	SH _{CP} ,	251+125	50 10 9	-14 -5	10) 	65 13 11	25	75 15 13	- - 837:	ns ns	2.0 4.5 6.0	Figs 11 and 12
f _{max}	maximu	ım cloc	k	6.0	30	.VIII/A	4.8	SYT .	4.0	1_	MHz	2.0	Figs 7
Tig.7	frequer SH _{CP} o	ncy an	225	30 35	92		24 28	94	20 24	elay –	MHz MHz	4.5	and 8

74HC/HCT594

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics, see chapter 'HCMOS family characteristics', section 'Family specifications'.

Output capability: parallel outputs, bus driver; serial output, standard.

Icc category: MSI.

Note to HCT types

The value of additional quiescent supply current $(\Delta I_{\rm CC})$ for a unit load of 1 is given in the family specifications. To determine $\Delta I_{\rm CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT					
D _s	0.25					
SH _R	1.50					
SH _{CP}	1.50					
ST _{CP}	1.50					
STR	1.50					

AC CHARACTERISTICS FOR 74HCT GND = 0 V; t_r = t_t = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	erupruo 60			T _{amb} (°C)				TEST CONDITIONS		
		+25			-40 to +85		-40 to +125		UNIT	V _{cc}	WAVE-
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		(V)	FORMS
t _{PHL} /t _{PLH}	propagation delay SH _{CP} to Q ₇ '	evsW	18	32	-	40	-	48	ns	4.5	Fig.7
	propagation delay ST _{CP} to Q _n	je ded	18	32	= (q; XD)	40	shin <u>o</u> li sys, the	48	ns	4.5	Fig.8
t _{PHL}	propagation delay SH _R to Q ₇ '	-	17	30	-	38	ine mu	45	ns	4.5	Fig.11
	propagation delay	-	17	30	-	38	-	45	ns	4.5	Fig.12
t _w	shift clock pulse width HIGH or LOW	16	4	-	20	-	24	-	ns	4.5	Fig.7
	storage clock pulse width HIGH or LOW	16	4	-	20	-	24		ns	4.5	Fig.8
	shift and storage reset pulse width HIGH or LOW	16	6	-	20		24	-	ns	4.5	Figs 11 and 12
t _{su}	set-up time D _s to SH _{CP}	20	4	-	25		30		ns	4.5	Fig.9
	set-up time SH _R to ST _{CP}	20	6	-	25	-	30	-	ns	4.5	Fig.10
	set-up time SH _{CP} to ST _{CP}	20	7	-	25	-	30	-	ns	4.5	Fig.8
t _h	hold time D _S to SH _{CP}	5	-3	-	6	-	7	-	ns	4.5	Fig.9
t _{rem}	removal time SH _R to SH _{CP} , ST _R to ST _{CP}	10 270	-5	-	13	-	15	- /-	ns	4.5	Figs 11 and 12
f _{max}	maximum clock frequency SH _{CP} or ST _{CP}	30	92	-	24	-	20	-	MHz	4.5	Figs 7 and 8

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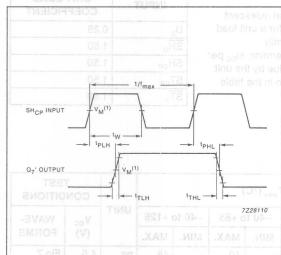


Fig.7 Waveforms showing the shift clock (SH_{CP}) to output (Q₇') propagation delays, the shift clock pulse width and the maximum shift clock frequency.

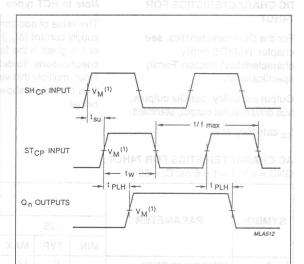


Fig.8 Waveforms showing the storage clock (ST_{cP}) to output (Q_n) propagation delays, the storage clock pulse width, maximum storage clock frequency and the shift clock to storage clock set-up time.

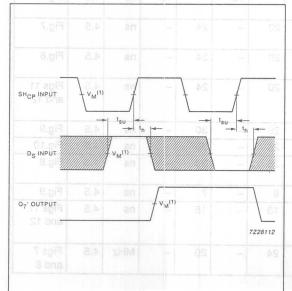


Fig.9 Waveforms showing the data set-up and hold times for the D_S input.

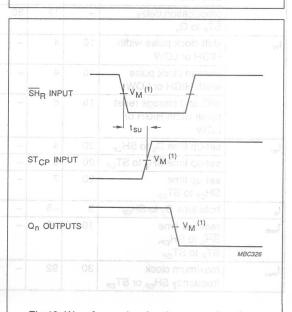


Fig.10 Waveforms showing the set-up time from shift reset (\overline{SH}_R) to storage clock (ST_{CP}) .

8-bit shift register with output register

74HC/HCT594

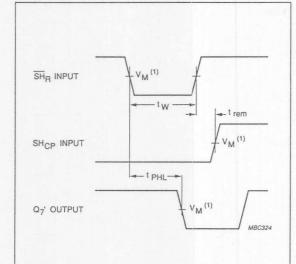
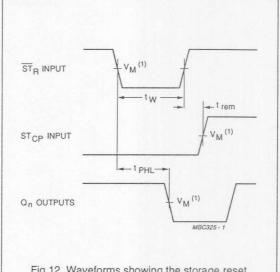


Fig.11 Waveforms showing the shift reset (\overline{SH}_R) pulse width, the shift reset to output (Q_7') propagation delay and the shift reset to shift clock (SH_{CP}) removal time.



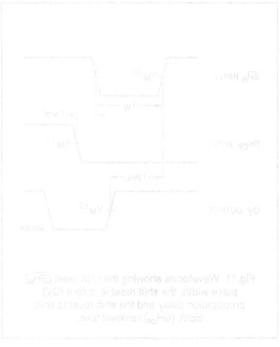
 $\begin{array}{ll} \underline{\mbox{Fig.12}} & \mbox{Waveforms showing the storage reset} \\ (\overline{\mbox{ST}}_{\mbox{\scriptsize R}}) & \mbox{pulse width, the storage reset to outputs} \\ (\mbox{Q}_{\mbox{\scriptsize n}}) & \mbox{propagation delay and the storage reset to} \\ & \mbox{storage clock } (\mbox{ST}_{\mbox{\scriptsize CP}}) & \mbox{removal time.} \end{array}$

Note (1)

HC: V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-bit shift register with outpureqister

74HC/HCT594





Note (1)

NC: V_{ve} = 50%; V_e = CND to V_{co}. HTC. V_{ve} = 1.3 V; V_e = GND to 3 V

8-bit serial-in/serial or parallel-out shift and lells and lells and 18 74HC/HCT595 register with output latches; 3-state

FEATURES

- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typ) shift out frequency
- Output capability:
 - parallel outputs; bus driver
 - serial output; standard
- I_{cc} category: MSI.

APPLICATIONS .nothinging night tig

- Serial-to-parallel data conversion
- Remote control holding register.

DESCRIPTION

The 74HC/HCT595 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The "595" is an 8-stage serial shift register with a storage register and 3-state outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the SH_{CP} input. The data in each register is transferred to the storage register on a positive-going transition of the ST_{CP} input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (D_s) and a serial standard output (Q7) for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register

stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input (OE) is LOW.

QUICK REFERENCE DATA

 $GND = 0 \text{ V}; T_{amb} = 25 \text{ °C}; t_r = t_f = 6 \text{ ns}.$

SYMBOL	ck input	shift register of	T	40H		
	PARAMETER	CONDITIONS	НС	нст	UNIT	
t _{PHL} /t _{PLH}	propagation delay SH _{CP} to Q ₇ ' ST _{CP} to Q _n MR to Q ₇ '	C _L = 15 pF 09 V _{CC} = 5 V	16 17 14	21 20 19	ns ns ns	
f _{max}	maximum clock frequency SH _{CP} , ST _{CP}		100	57	MHz	
Cı	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	115	130	pF	

Notes

 C_{PD} is used to determine the dynamic power dissipation (P_{D} in μW):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_1 \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz C_L = output load capacitance in pF f_o = output frequency in MHz V_{cc} = supply voltage in V $\Sigma(C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$

For HC the condition is $V_1 = GND$ to V_{CC} For HCT the condition is $V_1 = GND$ to $V_{CC} - 1.5 \text{ V}$.

ORDERING INFORMATION

EXTENDED TYPE		PACKAGE								
NUMBER	PINS	PIN POSITION	MATERIAL	CODE						
74HC/HCT595N	16	DIL ^M 81	plastic	SOT38Z						
74HC/HCT595D	16	SO16	plastic	SOT109A						

8-bit serial-in/serial or parallel-out shift a two-tells and to laine register with output latches; 3-state

74HC/HCT595

Stages. The storage register BRINNIP

SYMBOL	PIN	DESCRIPTION
Q ₀ - Q ₇	15, 1 - 7	parallel data output
GND	8	ground (0 V)
Q ₇ '	9	serial data output
MR	10	master reset (active LOW)
SH _{CP}	,gy:11	shift register clock input
ST _{CP}	12	storage register clock input
ŌĒ	13	output enable (active LOW)
D _s	14	serial data input
V _{cc}	16	positive supply voltage

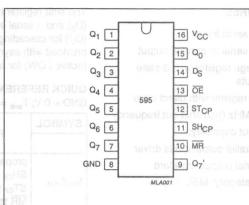
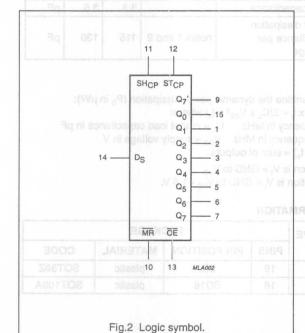


Fig.1 Pin configuration. anomabuse



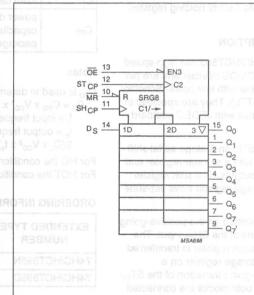
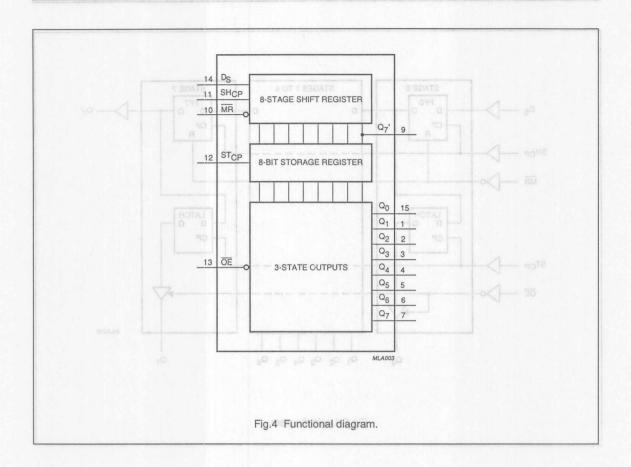
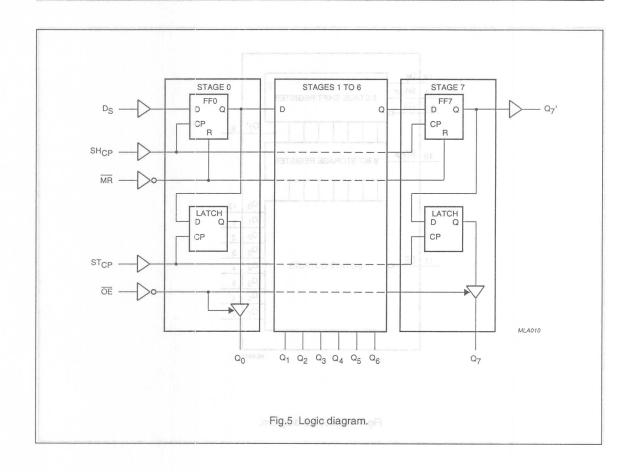


Fig.3 IEC logic symbol.

8-bit serial-in/serial or parallel-out shift and two-leafs to 15 74HC/HCT595 register with output latches; 3-state



8-bit serial-in/serial or parallel-out shift register with output latches; 3-state register with output latches; 3-state



8-bit serial-in/serial or parallel-out shift register with output latches; 3-state 74HC/HCT595

FUNCTION TABLE

		INPUTS			OU	PTUTS	FUNCTION
SH _{CP}	ST _{CP}	ŌĒ	MR	Ds	Q ₇ '	Qn	FUNCTION
X	x	111	1	x		NC	a LOW level on MR only affects the shift registers
X	1	L	L	X	L	L	empty shift register loaded into storage register
X	x	н	LA	x	The state of the s	Z	shift register clear. Parallel outputs in high-impedance OFF-state
†	X	L	Н	Н	Q ₆ '	NC	logic high level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q ₆ ') appears on the serial output (Q ₇ ')
X	A Companie Or Fra	L	н	x	NC	Q _n '	contents of shift register stages (internal Q _n ') are transferred to the storage register andparallel output stages
1	1	L	Н	x	Q ₆ '	Q _n '	contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages.

HIGH voltage level

LOW voltage level

LOW-to-HIGH transition

HIGH-to-LOW transition

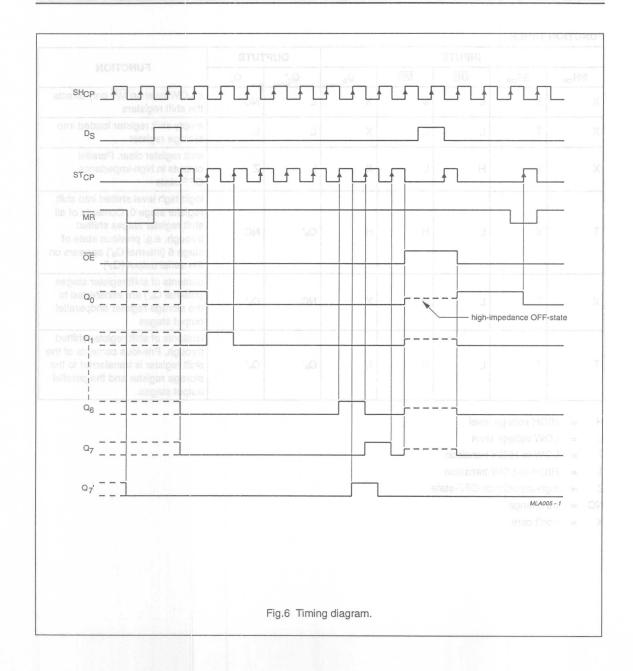
Z high-impedance OFF-state

NC = no change

don't care.

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74HC/HCT595



8-bit serial-in/serial or parallel-out shift 74HC/HCT595 register with output latches; 3-state

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Output capability: parallel outputs, bus driver; serial output, standard Icc category: MSI.

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF.$

			J		T _{amb (°C})				TEST	CONDITION
SYMBOL	PARAMETER		+25			to +85	-40 to	0 +125	UNIT	V _{cc}	WAVEFORMS
	ly specifications".	MIN	TYP	MAX	MIN	MAX	MIN	MAX	rio eea	(V)	WAVEFORMS
t _{PHL} /t _{PLH}	propagation delay SH _{CP} to Q ₇ '	-	52 19 15	160 32 27	ut star	200 40 34	ver, se	240 48 41	ns ns ns	2.0 4.5 6.0	Fig.7
t _{PHL} /t _{PLH}	propagation delay ST _{CP} to Q _n	_ _ _	55 20 16	175 35 30	- - inu s r	220 44 37	- manus	265 53 45	ns ns ns	2.0 4.5 6.0	Fig.8 H of sto
t _{PHL}	propagation delay MR to Q ₇ '	- - -	47 17 14	175 35 30	nput,4n	220 44 37	the ta	265 53 45	ns ns ns	2.0 4.5 6.0	Fig.10) vd suls
t _{PZH} /t _{PZL}	3-state output enable time OE to Qn	_ _ _	47 17 14	150 30 26	- -QAO FARIO	190 38 33	-	225 45 38	ns ns ns	2.0 4.5 6.0	Fig.11
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Qn	-	41 15 12	150 30 26	- a	190 38 33	- - -	225 45 38	ns ns ns	2.0 4.5 6.0	Fig.11
t _w	shift clock pulse width HIGH or LOW	75 15 13	17 6 5	-	95 19 16	T L	110 22 19	- - -	ns ns ns	2.0 4.5 6.0	Fig.7
t _w	storage clock pulse width HIGH or LOW	75 15 13	11 4 3	-	95 19 16	-	110 22 19	- - -	ns ns ns	2.0 4.5 6.0	Fig.8
t _w	master reset pulse width LOW	75 15 13	17 6.0 5.0	-	95 19 16	-	110 22 19	-	ns ns ns	2.0 4.5 6.0	Fig.10
t _{su}	set-up time D _s to SH _{CP}	50 10 9.0	11 4.0 3.0	- - -	65 13 11	-	75 15 13	- - -	ns ns ns	2.0 4.5 6.0	Fig.9
t _{su}	set-up time SH _{CP} to ST _{CP}	75 15 13	22 8 7	- - -	95 19 16	_ _ _	110 22 19	- - -	ns ns ns	2.0 4.5 6.0	Fig.8
t _h	hold time D _S to SH _{CP}	3 3 3	-6 -2 -2	-	3 3 3	- - -	3 3 3	- - -	ns ns ns	2.0 4.5 6.0	Fig.9
t _{rem}	removal time MR to SH _{CP}	50 10 9	-19 -7 -6	-	65 13 11	-	75 15 13	-	ns ns ns	2.0 4.5 6.0	Fig.10

8-bit serial-in/serial or parallel-out shift the two leading to 1810 74HC/HCT595 register with output latches; 3-state

SYMBOL PAF			T _{amb (°C)}								TEST CONDITION	
	PARAMETER	med notice and he			-40 to +85		-40 to +125		UNIT	V _{cc}	For the DD chart	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	stugtue	(V)	WAVEFORMS	
	maximum clock	6	30	-	4.8	-	4	- ou	MHz	2.0	CCHARACTE	
f _{max}	pulse frequency SH _{CP} or ST _{CP}	30 35	91	-	24 28	_	20 24	- 146	MHz MHz	4.5 6.0	Figs 7 and 8	

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: parallel outputs, bus driver; serial output, standard Icc category: MSI.

Note to HCT types

The value of additional quiescent supply current (Δl_{cc}) for a unit load of 1 is given in the family specifications. To determine ΔI_{cc} per input, multiply this value by the unit load coefficient shown in the table below.

 $GND = 0 V; t_r = t_r = 6 ns; C_1 = 50 pF$

		1.42	UGI	-	961		CAN	GF P.	G.P.L.	- 0 1, 4 - 4 - 0
		1.7		DAD	JNIT LO			arı		INPUT
		14		IENT	OEFFIC	C		SU		INPUT
		41	150	-	0.25	-	225	Sti	2.0	Ds
		E1	90 ac		1.50		68	20	0.8	MR
		117		20	1.50	OFF		271	ne	SH _{CP}
	75	-			1.50	99		en	4.5	ST _{CP}
		3			1.50	811		SUI	0.8	ŌĒ
		11		95	1100	otri		an	0.8	

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF.$

					T _{amb (°C})				TES	T CONDITION
SYMBOL	PARAMETER		+25	- xem 1		o +85	-40 to	+125	UNIT	V _{cc}	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX		(V)	WAVEFORIVIS
t _{PHL} /t _{PLH}	propagation delay SH _{CP} to Q ₇ '	-	25	42	-	53	-	63	ns	4.5	Fig.7
t _{PHL} /t _{PLH}	propagation delay ST _{CP} to Q _n	_neq 1	24	40	T NU	50	-	60	ns	4.5	Fig.8
t _{PHL}	propagation delay MR to Q ₇ '	-	23	40	1	50	TUST	60	ns	4.5	Fig.10
t _{PZH} / t _{PZL}	3-state output enable time OE to Q _n	-	21	35	-	44	-	53	ns	4.5	Fig.11
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Qn	-	18	30	-	38	-	45	ns	4.5	Fig.11
t _w	shift clock pulse width HIGH or LOW	16	6	propa	20	tuo ot numi	24	l <u>o</u> pio ei	ns	4.5	Fig.7
t _w	storage clock pulse width HIGH or LOW	16	5	-	20	-	24	-	ns	4.5	Fig.8
t _w	master reset pulse width LOW	20	8	-	25	-	30	-	ns	4.5	Fig.10
t _{su}	set-up time D _S to SH _{CP}	16	5	- /	20 (1)	17	24	SHOP	ns	4.5	Fig.9
t _{su}	set-up time SH _{CP} to ST _{CP}	16	8	-	20	100 le-	24	-	ns	4.5	Fig.8
t _h	hold time Ds to SHCP	3	-2	-/-	3	-	3	-	ns	4.5	Fig.9
t _{rem}	removal time MR to SH _{CP}	10	-7	#	13	-	15	STOP	ns	4.5	Fig.10
f _{max}	maximum clock pulse frequency SH _{CP} or ST _{CP}	30	52		24	-	20	-	MHz	4.5	Figs 7 and 8

8-bit serial-in/serial or parallel-out shift line two letter to lane register with output latches; 3-state

74HC/HCT595

AC WAVEFORMS

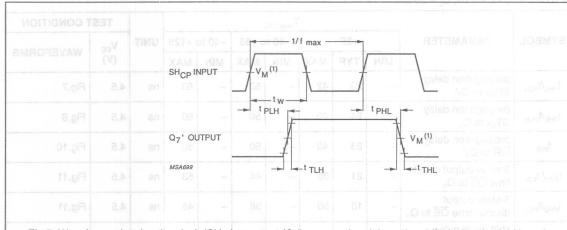


Fig.7 Waveforms showing the clock (SH_{CP}) to output (Q₇') propagation delays, the shift clock pulse width and maximum shift clock frequency.

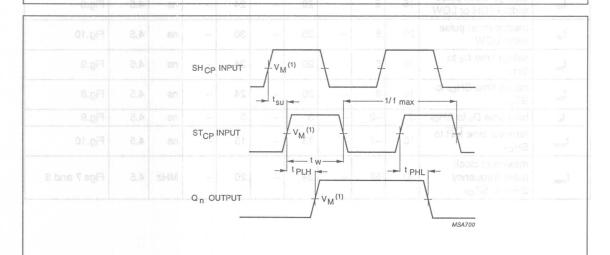
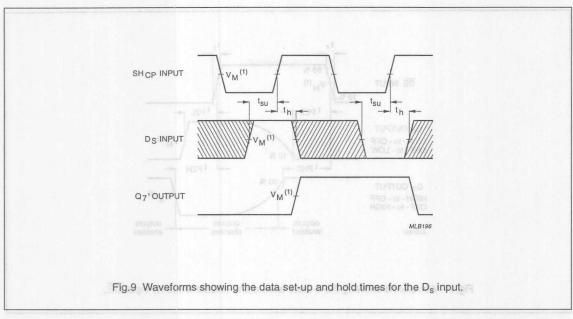
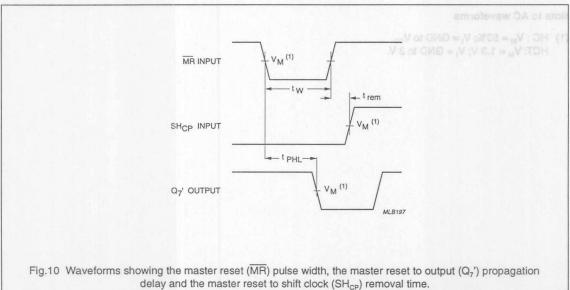


Fig.8 Waveforms showing the storage clock (ST_{CP}) to output (Q_n) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time.

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

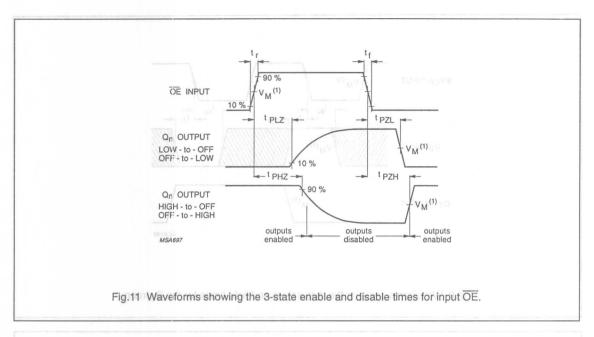
74HC/HCT595





8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74HC/HCT595



Note to AC waveforms

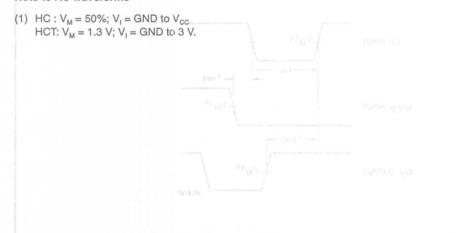


Fig 10. Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_r) propagation delay and the master reset to shift clock ($SH_{\rm re}$) removal time.

8-BIT SHIFT REGISTER WITH INPUT FLIP-FLOPS

FEATURES

- 8-bit parallel storage register inputs
- Shift register has direct overriding load and clear
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT597 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky (TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT597 consist each of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive edge-triggered clocks. The shift register also has direct load (from storage) and clear inputs.

			TYF	30 NI		
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT	
t _{PHL} /	propagation delay SHCP to Q STCP to Q PL to Q		17 25 21	20 29 26	ns ns ns ns ns	
f _{max}	maximum clock frequency SHCP	riotz sobe	96	83	MHz	
CI	input capacitance of basel fall	616Q	3.5	3.5	pF E	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	29	32	pF	

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

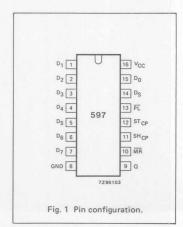
$$\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$$

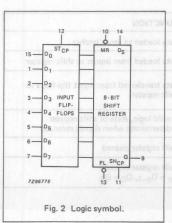
For HCT the condition is
$$V_I = GND$$
 to $V_{CC} - 1.5 V$

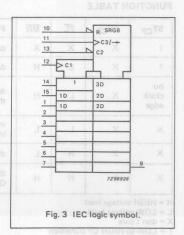
PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

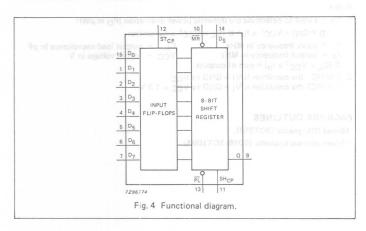






PIN DESCRIPTION

PIN NO.	HCT	SYMBOL	NAME AND FUNCTION
8 9 10 11 12	20 28 28 83	GND Q MR SHCP STCP	ground (0 V) serial data output asynchronous reset input (active LOW) shift clock input (LOW-to-HIGH, edge-triggered) storage clock input (LOW-to-HIGH, edge-triggered)
13 3		PL	parallel load input (active LOW)
14 15, 1, 2, 4, 5, 6,		D _S D ₀ to D ₇ V _{CC}	parallel data inputs positive supply voltage



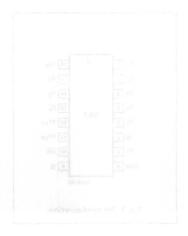
FUNCTION TABLE

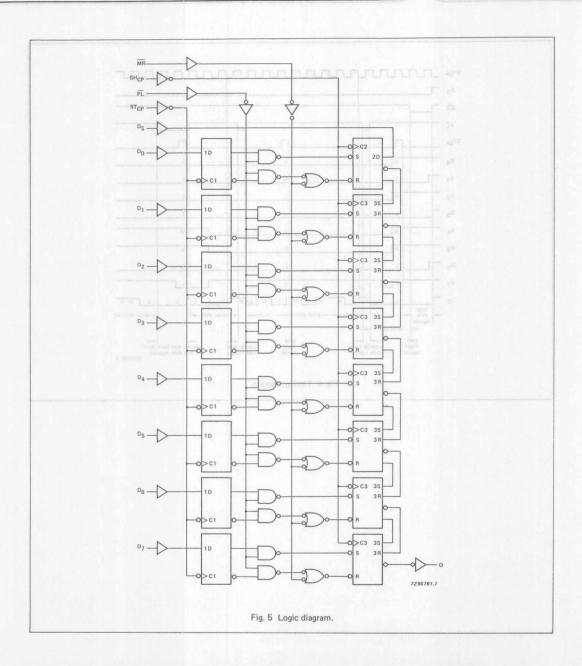
STCP	SHCP	PL	MR	FUNCTION
†	X	X	X	data loaded to input latches
↑	×	Las	Н	data loaded from inputs to shift register
no clock edge	X 48	Lai	Н	data transferred from input flip-flops to shift register
X	×	L	L	invalid logic, state of shift register indeterminate when signals removed
X	X	Н	L	shift register cleared
X	454 1	Н	Н	shift register clocked $Q_n = Q_{n-1}, Q_0 = D_S$

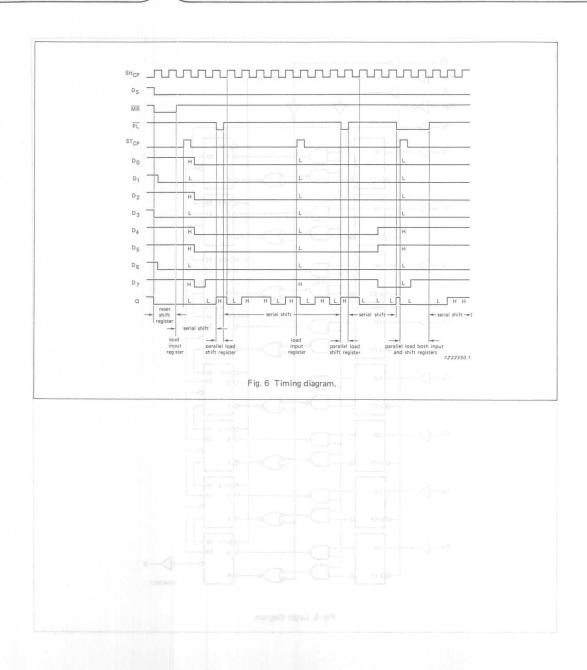
H = HIGH voltage level
L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH CP transition







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

					- 2	T _{amb} (°C)			3	1	TEST CONDITIONS	
	Fig. 11		in .		8	74H	С		1-	UNIT	V	WAVEFORMS	
SYMBOL	PARAMETER			+25	a	-40	to +85	-40 t	o +125	UNII	V _{CC}		
	Fig. 11		min.	typ.	max.	min.	max.	min.	max.	07.03		hold time PL, Dg to SH	
t _{PHL} /	propagation del	ay ay	VI:	55 20 16	175 35 30		220 44 37		265 53 45	ns Von	2.0 4.5 6.0	Fig. 7 mixsm	
^t PHL	propagation del	ay		58 21 17	175 35 30		220 44 37		265 53 45	ns TOH	2.0 4.5 6.0	Fig. 8	
t _{PHL} /	propagation del	ay	amosqs	80 29 23	250 50 43	592, 2	315 63 54	staff0 y	375 75 64	ns	2.0 4.5 6.0	Fig. 7	
t _{PHL} /	propagation del	ay	intel s	69 25 20	215 43 37	to be	270 54 46	not to	325 65 55	ns mus yla	2.0 4.5 6.0	Fig. 9	
tTHL/ tTLH	output transitio	on time	ilds) s	19 7 6	75 15 13	SIGNITS	95 19 16	ilinu an	110 22 19	ns	2.0 4.5 6.0	Fig. 9	
t _W	ST _{CP} pulse wid		80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7 83.0	
t _W	SH _{CP} pulse wid	lth /	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
t _W	MR pulse width		80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	
tw	PL pulse width		80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9	
t _{rem}	removal time MR to SH _{CP}		60 12 10	-3 -1 -1		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 10	
t _{su}	set-up time D _n to ST _{CP}		60 12 10	8 3 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 11	
t _{su}	set-up time DS to SHCP		60 12 10	11 4 3		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 11	
t _{su}	set-up time PL to SH _{CP}		60 12 10	11 4 3		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 12	

AC CHARACTERISTICS FOR 74HC (Cont'd)

SYMBOL		T _{amb} (°C)								Т	EST CONDITIONS
	DADAMETER									V	WAVEFORMS
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC	
		min.	typ.	max.	min.	max.	min.	max.		= 50 ps	
^t h	hold time D _n to ST _{CP}	5 5 5	-3 -1 -1		5 5 5	resub 749	5 5 5		ns	2.0 4.5 6.0	Fig. 11
^t h	hold time PL, DS to SHCP	5 5 5	-6 -2 -2	nim	5 5 5	aini .	5 5 5	g v.	ns	2.0 4.5 6.0	Fig. 11
f _{max}	maximum pulse frequency SHCP	6.0 30 35	29 87 104		4.8 24 28		4.0 20 24	88 88 81	MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard Output capability: standard ICC category: MSI

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	COEFFICIENT	0.8				
DS D _n PL, MR	0.25 0.30 1.50	2.0 4.5 6.0				
ST _{CP} , SH _{CF}		2,0 4,6 8,0				

AC WAVEFORMS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

					T _{amb} (°C)				L wante	EST CONDITIONS	
0)/14001	10,00	10399			74HC	Т	1		UNIT	V	WAVEFORMS	
SYMBOL	PARAMETER	+25			-40 to +85 -40		-40 to	0+125	UNIT	V _{CC}	WAVEFORMS	
)—————————————————————————————————————	min.	typ.	max.	min.	max.	min.	max.			1 H20 1+	
t _{PHL} /	propagation delay SH _{CP} to Q	BASE TO SERVICE	23	40		50		60	ns	4.5	Fig. 7	
^t PHL	propagation delay MR to Ω		28	49		61		74	ns	4.5	Fig. 8	
tpHL/	propagation delay ST _{CP} to Q	sefore on del	33	57		71	elug qg	86	ns	4.5	Fig. 7	
t _{PHL} /	propagation delay PL to Q		30	52		65		78	ns	4.5	Fig. 9	
t _{THL} /	output transition time		7	15		19	-	22	ns	4.5	Fig. 9	
t _W	SHCP pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 7	
t _W	ST _{CP} pulse width HIGH or LOW	16	6		20		24	ra-11/g ³	ns	4.5	Fig. 7	
t _W	MR pulse width LOW	25	14		31		38		ns	4.5	Fig. 8	
t _W	PL pulse width LOW	20	10		25		30	14	ns	4.5	Fig. 9	
t _{rem,goH}	removal time MR to SHCP	12	-2	019	15	ne	18	to C. d suspus	ns	4.5	Fig. 10	
t _{su}	set-up time D _n to ST _{CP}	12	5		15		18		ns	4.5	Fig. 11	
t _{su}	set-up time DS to SHCP	12	2		15		18		ns	4.5	Fig. 11	
t _{su}	set-up time PL to SHCP	12	4	M1 10	15		18		ns	4.5	Fig. 12	
th	hold time D _n to ST _{CP}	5	-1		5	-	5		ns	4.5	Fig. 11	
t _h	hold time PL, DS to SHCP	5	-2	to HE	5		5		ns	4.5	Fig. 11	
f _{max}	maximum pulse frequency SHCP	30	75	14155	24		20		MHz	4.5	Fig. 7	

AC WAVEFORMS

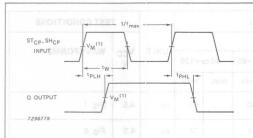
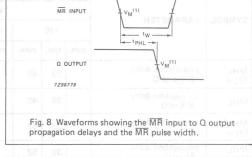


Fig. 7 Waveforms showing the SH_{CP} and ST_{CP} inputs to Q output propagation delays, the SH_{CP} and ST_{CP} pulse widths and maximum clock pulse frequency.



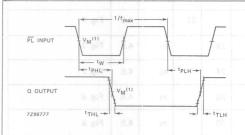


Fig. 9 Waveforms showing the \overline{PL} input to Ω output propagation delays, \overline{PL} pulse width and output transition times

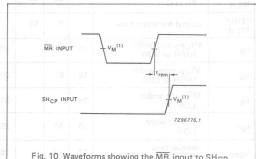


Fig. 10 Waveforms showing the $\overline{\rm MR}$ input to SHCP, STCP removal times.

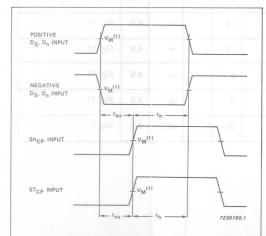


Fig. 11 Waveforms showing hold and set-up times for DS, Dn inputs to SHCP, STCP inputs.

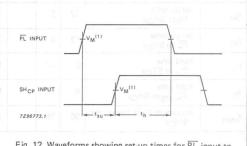


Fig. 12 Waveforms showing set-up times for \overline{PL} input to SH_{CP} input.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL BUS TRANSCEIVER; 3-STATE; INVERTING

FEATURES

- Octal bidirectional bus interface
- Inverting 3-state outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT640 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT640 are octal transceivers featuring inverting 3-state bus compatible outputs in both send and receive directions.

The "640" features an output enable (OE) input for easy cascading and a send/receive (DIR) for direction control. OE controls the outputs so that the buses are effectively isolated.

The "640" is similar to the "245" but has inverting outputs.

	PIN DESCRIPTION	CONDITIONS	TYF	UNIT	
SYMBOL	PARAMETER OM MIS	CONDITIONS	нс	нст	UNIT
^t PHL [/] ^t PLH	propagation delay A _n to B _n ; B _n to A _n	C _L = 15 pF V _{CC} = 5 V	9	9	ns
Cl	input capacitance		3.5	3.5	pF
C _{1/O}	input/output capacitance		10	10	pF
C _{PD}	power dissipation capacitance per transceiver	notes 1 and 2	35	35	pF

GND = 0 V;
$$T_{amb} = 25 \, ^{\circ}C$$
; $t_r = t_f = 6 \, \text{ns}$

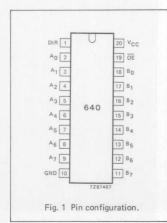
Notes

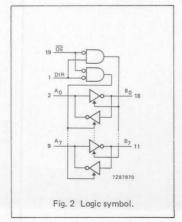
- 1. CPD is used to determine the dynamic power dissipation (PD in μW):
 - $PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$ where: $f_1 = input frequency in MHz$ CL = outp
 - f_0 = output frequency in MHz Σ (C_L x V_{CC}² x f_0) = sum of outputs
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

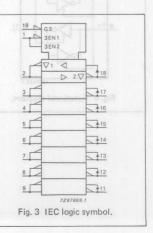
ORDERING INFORMATION/PACKAGE OUTLINES

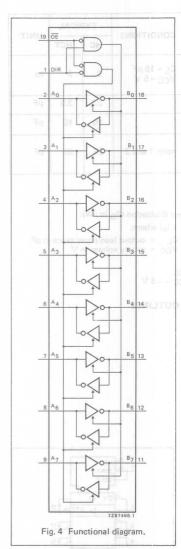
20-lead DIL; plastic (SOT146).

20-lead mini-pack; plastic (SO20; SOT163A).









PIN DESCRIPTION

gratian.	SYMBOL BARAL	 Vota) bidilectional bus interface
PIN NO.	SYMBOL	NAME AND FUNCTION
1 valso noise 2, 3, 4, 5, 6, 7, 8, 9	DIR A ₀ to A ₇	direction control REM MARKER SIGN * data inputs/outputs
10 18, 17, 16, 15, 14, 13, 12, 11	GND B ₀ to B ₇	ground (0 V) generation and the High Court of the Series and the High Court of the Series and the High Court of the High
19 rousquais 20 rag sonad		output enable input (active LOW) positive supply voltage

FUNCTION TABLE

in	puts	inputs/outputs					
ŌĒ	DIR	An	Bn				
L	L	A=B inputs	inputs R=Ā				
Н	X	Z	Z				

H = HIGH voltage level L = LOW voltage level

ORDERING INFORMA care AMBORNI BUIRBORO

Z = high impedance OFF-state





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC and add not exercise the best time and (p) of the best visible to exceed an TGND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF index add not exercise best time and (q) are the properties of th

					T _{amb} (°C)				QA	TEST CONDIT	IONS
					74HC	;				TMan	1191303	
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	VCC	WAVEFORM	IS nA
		min.	typ.	max.	min.	max.	min.	max.			0.80	
t _{PHL} /	propagation delay A _n to B _n ; B _n to A _n		30 11 9	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 5	
^t PZH [/]	3-state output enable time OE, DIR to A _n ; OE, DIR to B _n		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6	
tPHZ/	3-state output disable time OE, DIR to A _n ; OE, DIR to B _n		50 18 14	150 30 26	TON	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6	YMBOL
tTHL/ tTLH	output transition time	25	14 5 4	60 12 10	sim .e	75 15 13	em lo	90 18 15	ns	2.0 4.5 6.0	Fig. 5	
	s 4,5 Fig. 5	3 1	33		28		22	11		yels	propagation o	VJH9 PLIS

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

Note to HCT types

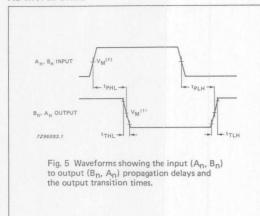
The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. F2IR31DARAHODA To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below $a = 10 \text{ cm} \text{ a} = 10 \text{ cm} \text{$

INPUT	UNIT LO												
9													
A _n B _n OE	1.50	33V											
OE DIR	1.50 0.90												
	Fig. 5	2.0 4.5 6.0				115 23 20							
	ACTERISTICS $t_r = t_f = 6 \text{ ns; C}$	0.3	ICT										
		2.0		228		T _{amb}	(°C)	oar	na	time	eluszih i	TEST CONDIT	IONS
SYMBOL	PARAMETER		2.5)	45 38		74H	СТ	30 28	18	UNIT	V _{CC}	WAVEFORM	S
				09+2	5	-40	to +85	-40	to +125		V	***************************************	
	Pig. 5	4.5	mir	n. typ	o. max	G-11	max.	min.	max.		mit neil	output transi	HAT.
t _{PHL} /	propagation d A _n to B _n ; B _n to A _n	elay		11	22		28		33	ns	4.5	Fig. 5	
t _{PZH} /	3-state output OE, DIR to I	An;	ne	18	30		38		45	ns	4.5	Fig. 6	
t _{PHZ} /	3-state output OE, DIR to I	An;	ne	19	30		38		45	ns	4.5	Fig. 6	
tTHL/	output transit	ion time		5	12		15		18	ns	4.5	Fig. 5	

Fig. 5

tTLH

AC WAVEFORMS



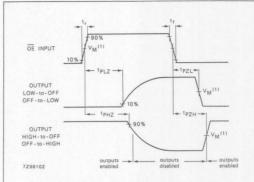


Fig. 6 Waveforms showing the 3-state enable and disable times,

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

MEWAVEFORE





Fig. 6 Waveforms showing the 3-state enable and disable times.

(V. 1856 – g. V. 1. O.H. () 7. SV. () = k. V. (1. O.H.

OCTAL BUS TRANSCEIVER; 3-STATE; TRUE/INVERTING

FEATURES

- Octal bidirectional bus interface
- True and inverting 3-state outputs
- Output capability: bus driver
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT643 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT643 are octal transceivers featuring true and inverting 3-state bus compatible outputs in both send and receive directions.

The "643" features an output enable (OE) input for easy cascading and a send/receive (DIR) for direction control. OE controls the outputs so that the buses are effectively isolated.

FUNCTION TABLE

INF	PUTS	INPUTS/OUTPUTS					
ŌĒ	DIR	An	B _n				
L L H	L H X	A = B inputs Z	inputs B = A Z				

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

			TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	ONT	
^t PHL/ ^t PLH	propagation delay An to Bn; inverting Bn to An; true	C _L = 15 pF V _{CC} = 5 V	7 8	8 ⁸¹⁰	ns ns	
CI	input capacitance	87.00	3.5	3.5	pF	
C _{1/O}	input/output capacitance		10	10	pF	
C _{PD}	power dissipation capacitance per transceiver	notes 1 and 2	42	44	pF	

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x VCC^2 x f_i + Σ (CL x VCC^2 x f_o) where:

f; = input frequency in MHz

CL = output load capacitance in pF

fo = output frequency in MHz $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$ VCC = supply voltage in V

2. For HC the condition is VI = GND to VCC For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 V$

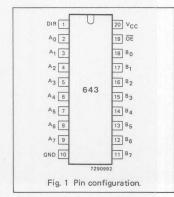
PACKAGE OUTLINES

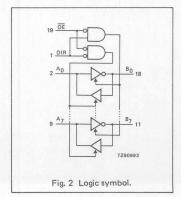
20-lead DIL; plastic (SOT146).

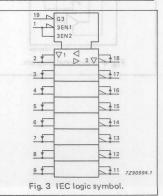
20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₇	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B ₀ to B ₇	data inputs/outputs
19	ŌĒ	output enable input (active LOW)
20	Vcc	positive supply voltage







19 OE

6 A₄

B₀ 18

B₁ 17

B₂ 16 attle =

B4 14

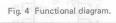
B₅ 13

B₆ 12











748

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC met aft of moving at 1 to be of tinu a vot ($_{OOL}$) the rub yigges traced up fanotible to automatic GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF all at aft of covers transition be all tinu at a $_{C}$ at the vigorities around a soft moving the object of the vigorities around a soft moving the object of the vigorities are consistent of the vigorities and vigorities are consistent of the vigorities are consistent of the vigorities and vigorities are consistent of the vigorities are consistent of the vigorities and vigorities are consistent of the vigoriti

			T _{amb} (°C)										TEST CONDITIONS	
	PARAMETER			74HC								neioliffece		
SYMBOL				+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORM	
				min.	typ.	max.	min.	max.	min.	max.			1.50	
tPHL/ tPLH	propagation delay An to Bn; inverting				25 9 7	90 18 15		115 23 20		135 27 23	ns TOMAS	2.0 4.5 6.0	Fig. 5	ARAHO O
tPHL/	propagation delay B _n to A _n ; non-inverting (true)			28 10 8	90 18 15	(13°)	115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 6	ND = Q V;	
tPZH/ tPZL	3-state outpool	An;	tirne	125	39 14 11	150 30 26	TOH!	190 38 33	05	225 45 38	ns	2.0 4.5 6.0	Fig. 7	SYMBOL
t _{PHZ} /	3-state output disable time OE, DIR to An; OE, DIR to Bn		time	náx	44 16 13	150 30 26	m la	190 38 33	qp. m	225 45 38	ns	2.0 4.5 6.0	Fig. 7	
t _{THL} /	output trans	ition tim	e	0.	14 5 4	60 12 10		75 15 13	2 0	90 18 15	ns	2.0 4.5 6.0	Figs 5 and 6	HJ9
d.gr= c.e z		-0.5	35			82		3 23			ng (true	Bn to Ani non-invertic	HTd	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", see solubles see shall selected and see solubles and selected and selected selected and selected selected and selected selec

Output capability: bus driver

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. Talkato ARAHO DA To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

unit load coefficient
1.50
0.40
1.50
0.90

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

		23			Tamb (°C)					g (true	TEST CONDITION	VS -
SYMBOL	2.0 4.5 - Fla.1	00174HCT 081 88						UNIT		WAVEFORMS	Versa	
	PARAMETER	88	+25	+25		-40 to +85		-40 to +125		V _{CC}	WAVEFORIVIS	
	2.0 ns 4.5 Fig. 7	min.	typ.	max.	min.	max.	min.	max.	samit s	deall; r	or Buc To	Shot
t _{PHL} /	propagation delay A _n to B _n ; inverting	88	10	20	7.5	25	3 26	30	ns	4.5	Fig. 5	714 T
^t PHL/	propagation delay B _n to A _n ; non-inverting (true)	10	13	23	27	29		35	ns	4.5	Fig. 6	
tPZH/ tPZL	3-state output enable time $\overline{\text{OE}}$, DIR to A_n ; $\overline{\text{OE}}$, DIR to B_n		16	30		38		45	ns	4.5	Fig. 7	
t _{PHZ} /	3-state output disable time OE, DIR to A _n ; OE, DIR to B _n		17	30		38		45	ns	4.5	Fig. 7	
tTHL/ tTLH	output transition time		5	12		15		18	ns	4.5	Figs 5 and 6	

AC WAVEFORMS

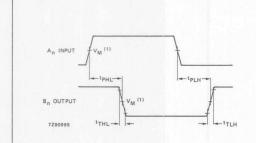
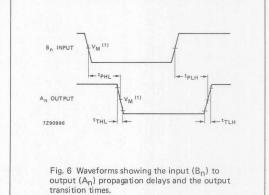


Fig. 5 Waveforms showing the input (A_n) to output (B_n) propagation delays and the output transition times.



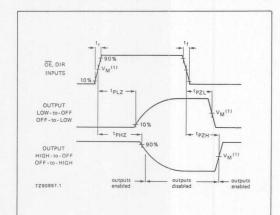


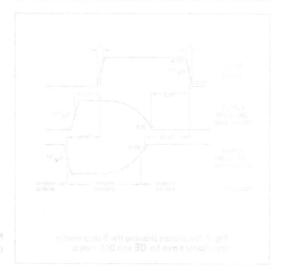
Fig. 7 Waveforms showing the 3-state enable and disable times for $\overline{\text{OE}}$ and DIR inputs.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.







OCTAL BUS TRANSCEIVER/REGISTER; 3-STATE

FEATURES

- Independent register for A and B
- Multiplexed real-time and stored data
- Output capability: bus driver
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT646 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT646 consist of bus transceiver circuits with 3-state outputs. D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the "A" or "B" bus will be clocked into the registers as the appropriate clock (CPAB and CPBA) goes to a HIGH logic level. Output enable (OE) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the "A" or "B" register, or in both. The select source inputs (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when OE is active (LOW). In the isolation mode (OE = HIGH), "A" data may be stored in the "B" register and/or "B" data may be stored in the "A" register. (continued on next page) also all beldens availe on anothern tugal and among RIO

SYMBOL	DADAMETED	CONDITIONS	TYF	IN DE	
	PARAMETER	CONDITIONS	нс	нст	UNIT
t _{PHL} /	propagation delay A _n , B _n to B _n , A _n	C _L = 15 pF - V _{CC} = 5 V	11 11	13	ns
f _{max}	maximum clock frequency	ACC = 2 A	69	85	MHz
CI	input capacitance	AZ Ada	3.5	3.5	pF
CPD power dissipation capacitance per channe		notes 1 and 2	30	33	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_0)$$
 where:

f; = input frequency in MHz fo = output frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

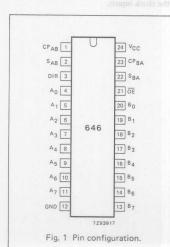
 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

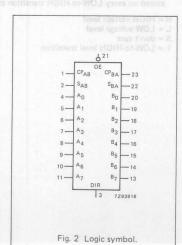
2. For HC the condition is VI = GND to VCC For HCT the condition is $V_I = GND$ to VCC - 1.5 V

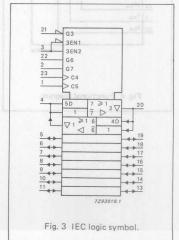
PACKAGE OUTLINES

24-lead DIL; plastic (SOT101A).

24-lead mini-pack; plastic (SO24; SOT137A).







PIN DESCRIPTION

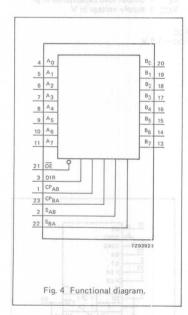
PIN NO.	SYMBOL	NAME AND FUNCTION	
1 87 87 2	CP _{AB}	A to B clock input (LOW-to-HIGH, edge-triggered) select A to B source input	HTq1 71Hd1
3 3 141/4 38	S _{AB} DIR	direction control input	
4, 5, 6, 7, 8, 9, 10, 11	A ₀ to A ₇	A data inputs/outputs	
12 20, 19, 18, 17, 16, 15, 14, 13	GND B ₀ to B ₇	ground (0 V) B data inputs/outputs	
21	ŌĒ	output enable input (active LOW)	
22	SBA	select B to A source input	
23	CPBA noisecie	B to A clock input (LOW-to-HIGH, edge-triggered)	
24	VCC terenty	positive supply voltage	

GENERAL DESCRIPTION

When an output function is disabled, the input function is still enabled and may be used to store and transmit data.

Only one of the two buses, A or B, may be driven at a time.

The "646" is functionally identical to the "648", but has non-inverting data paths.



FUNCTION TABLE

		Z SI DINI	PUTS			DATA	1/0 *	FUNCTION	
ŌĒ	DIR	CPAB	CPBA	S _{AB}	SBA	A ₀ to A ₇	B ₀ to B ₇		
Н	X	H or L	H or L ↑	X	X	input	input	isolation store A and B data	
L	L L	×	X H or L	X	L H	output	input	real-time B data to A bus stored B data to A bus	
L L	H H	X H or L	X	L H	X	input 6	output	real-time A data to B bus stored A data to B bus	

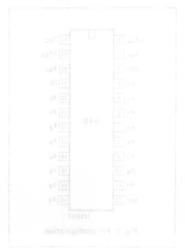
* The data output functions may be enabled or disabled by various signals at the $\overline{\text{OE}}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

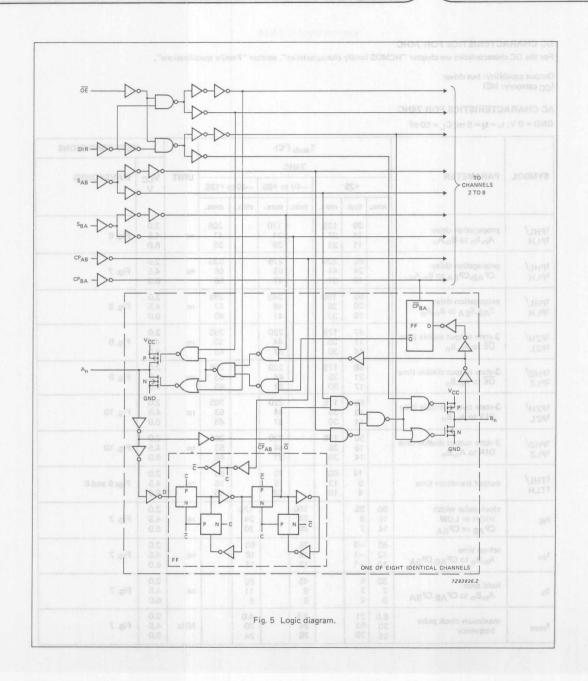
H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH level transition





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

					T _{amb} (°C)			-0(TEST CONDITIONS		
0)/14001	DADAMETER				74H	С			UNIT	6	WAVEFORMS	
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		ONT	V _{CC}	WATER OF THE	
		min.	typ.	max.	min.	max.	min.	max.		-1-		
t _{PHL} /	propagation delay A _n ,B _n to B _n ,A _n		39 14 11	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} /	propagation delay CPAB,CPBA to Bn,An		66 24 19	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 7	
t _{PHL} /	propagation delay SAB,SBA to B _n ,A _n		55 20 16	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 8	
t _{PZH} /	3-state output enable time OE to A _n ,B _n		47 17 14	175 35 30		220 44 37	0-	265 53 45	ns	2.0 4.5 6.0	Fig. 9	
t _{PHZ} /	3-state output disable time OE to A _n ,B _n		58 21 17	175 35 30		220 44 37	J.E.	265 53 45	ns	2.0 4.5 6.0	Fig. 9	
t _{PZH} /	3-state output enable time DIR to A _n ,B _n		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 10	
t _{PHZ} /	3-state output disable time DIR to A _n ,B _n		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 10	
t _{THL} /	output transition time		14 5 4	60 12 10	-0<1-	75 15 13	7,00	90 18 15	ns	2.0 4.5 6.0	Figs 6 and 8	
t _W	clock pulse width HIGH or LOW CP _{AB} or CP _{BA}	80 16 14	25 9 7		100 24 20		120 24 20	- r 9	ns	2.0 4.5 6.0	Fig. 7	
t _{su}	set-up time A _n ,B _n to CP _{AB} ,CP _{BA}	60 12 10	-3 -1 -1		75 15 13		90 18 15	>	ns	2.0 4.5 6.0	Fig. 7	
^t h	hold time A _n ,B _n to CP _{AB} ,CP _{BA}	35 7 6	6 2 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 7	
f _{max}	maximum clock pulse frequency	6.0 30 35	21 63 75	, onysig	4.8 24 28	g. S. Ld	4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
SAB, SBA	0.60
A ₀ to A ₇ and	0.75
B ₀ to B ₇	

INPUT	UNIT LOAD COEFFICIENT
CP _{AB} , CP _{BA}	1.50
OE DIR	1.50 1.25

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V; } t_r = t_f = 6 \text{ ns; } C_L = 50 \text{ pF}$

	opagation delays.	ig n/s.		100 01	T _{amb} (°C)				TEST CONDITIONS		
		74HCT								.,	WAVEFORMS	
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
	m _{av} .	min.	typ.	max.	min.	max.	min.	max.	-			
tPHL/	propagation delay A _n ,B _n to B _n ,A _n		16	30		38		45	ns	4.5	Fig. 6	
t _{PHL} /	propagation delay CPAB,CPBA to Bn,An		23	44		55	E)81 +	66	ns	4.5	Fig. 7	
tPHL/	propagation delay SAB,SBA to Bn,An		26	46		58	:01 p	69	ns ni si	4.5	Fig. 8 Wall 8 grid	
tPZH/	3-state output enable time OE to A _n ,B _n		21	40		50		60	ns	4.5	Fig. 9	
t _{PHZ} / t _{PLZ}	3-state output disable time OE to A _n ,B _n		20	35		44		53	ns	4.5	Fig. 9	
tPZH/	3-state output enable time DIR to An,Bn	Wayoti 3-state	21	40	-	50		60	ns	4.5	Fig. 10	
t _{PHZ} / t _{PLZ}	3-state output disable time DIR to A _n ,B _n		21	35		44	(DMV)	53	ns	4.5	Fig. 10	
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Figs 6 and 8	
t _W	clock pulse width HIGH or LOW CPAB or CPBA	16	8		20		24	- 5	ns	4.5	Fig. 7	
t _{su}	set-up time A _n ,B _n to CP _{AB} ,CP _{BA}	12	3		15		18		ns	4.5	Fig. 7	
th	hold time A _n ,B _n to CP _{AB} ,CP _{BA}	5	1		5		5	1-5	ns	4.5	Fig. 7	
f _{max}	maximum clock pulse frequency	30	77		24	TO BEE	20		MHz	4.5	Fig. 7	

AC WAVEFORMS

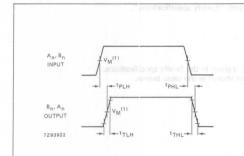


Fig. 6 Waveforms showing the input A_n , B_n to output B_n , A_n propagation delays and the output transition times.

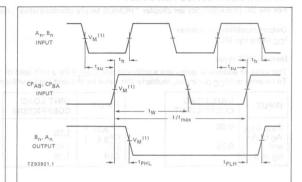


Fig. 7 Waveforms showing the A_n , B_n to CP_{AB} , CP_{BA} set-up and hold times, clock CP_{AB} , CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB} , CP_{BA} to output B_n , A_n propagation delays.

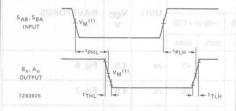


Fig. 8 Waveforms showing the input S_{AB} , S_{BA} to output B_n , A_n propagation delays and output transition times.

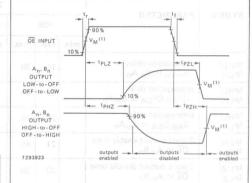


Fig. 9 Waveforms showing the input $\overline{\text{OE}}$ to output A_n,B_n 3-state enable and disable times.

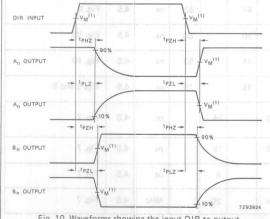
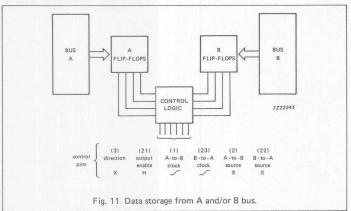


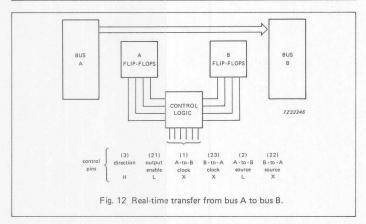
Fig. 10 Waveforms showing the input DIR to output A_n , B_n 3-state enable and disable times.

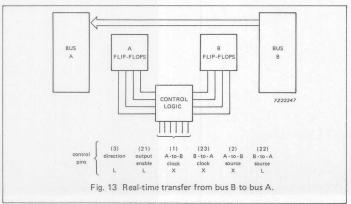


(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

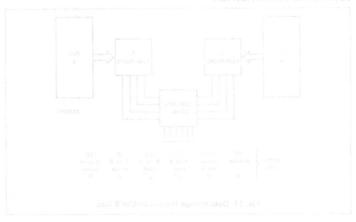
APPLICATION INFORMATION

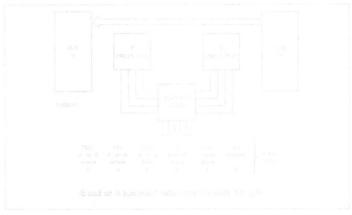


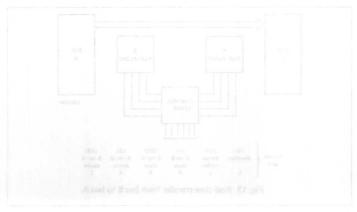




APPELLOW TO STATE STREET, AND APPEARING







OCTAL BUS TRANSCEIVER/REGISTER; 3-STATE; INVERTING

FEATURES

- Independent register for A and B buses
- Multiplexed real-time and stored data
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT648 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT648 consist of bus transceiver circuits with 3-state inverting outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the "A" or "B" bus will be clocked into the registers as the appropriate clock (CPAB and CPBA) goes to a HIGH logic level. Output enable (OE) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the "A" or "B" register, or in both. The select source inputs (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when \overline{OE} is active (LOW). In the isolation mode (\overline{OE} = HIGH), " \overline{A} " data may be stored in the "B" register and/or "B" data may be stored in the "A" register. (continued on next page)

		CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER GMA BI	CONDITIONS	нс	нст	ONTI	
t _{PHL} /	propagation delay \overline{A}_n , \overline{B}_n to \overline{B}_n , \overline{A}_n	C _L = 15 pF V _{CC} = 5 V	11	11	ns	
f _{max}	maximum clock frequency	ACC - 2 A	75	88	MHz	
CI	input capacitance	do A VA	3.5	3.5	pF	
C _{PD}	power dissipation (V 0) be capacitance per channel	notes 1 and 2	30	31	pF S	

GND = 0 V;
$$T_{amb} = 25 \,^{\circ}\text{C}$$
; $t_r = t_f = 6 \, \text{ns}$

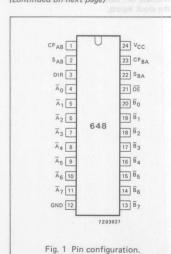
1. CPD is used to determine the dynamic power dissipation (P_D in μW):

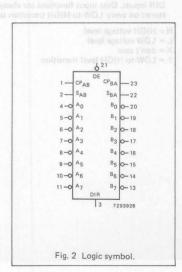
$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$$
 where:

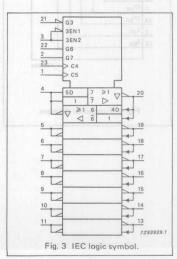
- fi = input frequency in MHz fo = output frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$ 2. For HC the condition is VI = GND to VCC For HCT the condition is VI = GND to VCC - 1.5 V

PACKAGE OUTLINES

24-lead DIL; plastic (SOT101A). 24-lead mini-pack; plastic (SO24; SOT137A).







PIN DESCRIPTION

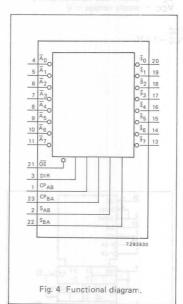
PIN NO.	SYMBOL	NAME AND FUNCTION
1 in 1:	CPAB	A to B clock input (LOW-to-HIGH, edge-triggered)
2	SAB	select A to B source input
3 25 88	DIR	direction control input
4, 5, 6, 7, 8, 9, 10, 11	\overline{A}_0 to \overline{A}_7	Ā data inputs/outputs
12	GND	ground (0 V) notesqlaib (1990)
20, 19, 18, 17, 16, 15, 14, 13	$\overline{\mathtt{B}}_{0}$ to $\overline{\mathtt{B}}_{7}$	B data inputs/outputs
21	ŌĒ	output enable input (active LOW)
22	SBA	select B to A source input
23	CPBA	B to A clock input (LOW-to-HIGH, edge-triggered)
24	VCC	positive supply voltage * * * * * * * * * * * * * * * * * * *

GENERAL DESCRIPTION (Cont'd)

When an output function is disabled, the input function is still enabled and may be used to store and transmit data.

Only one of the two buses, A or B, may be driven at a time.

The "648" is functionally identical to the "646", but has inverting data paths.



FUNCTION TABLE

		VIIIN	PUTS			DATA	1/0 *	(Alumatemie bas (BC
ŌĒ	DIR	CPAB	CPBA	S _{AB}	SBA	\overline{A}_0 to \overline{A}_7	\overline{B}_0 to \overline{B}_7	FUNCTION
H H	X	H or L ↑	H or L		X	input	input	isolation store \overline{A} and \overline{B} data
L L	L L	X	X H or L	X	L H	output	input	real-time B data to A bus stored B data to A bus
L L	H	X H or L	×	L H	X	input	output	real-time Ā data to B bus stored Ā data to B bus

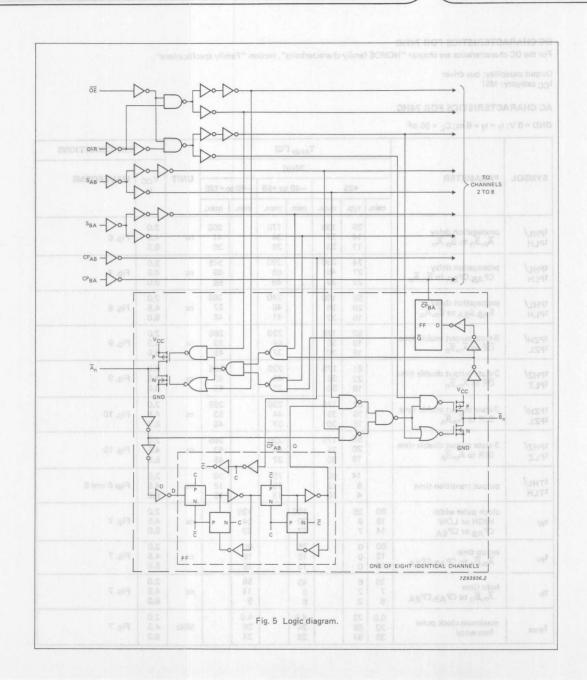
* The data output functions may be enabled or disabled by various signals at the $\overline{\text{OE}}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH level transition



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)					TEST CONDITIONS	
				9-	74H	С				(]- <	WAVEFORMS	
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORING	
		min.	typ.	max.	min.	max.	min.	max.		1		
t _{PHL} /	propagation delay $\overline{A}_n, \overline{B}_n$ to $\overline{B}_n, \overline{A}_n$		39 14 11	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} /	propagation delay CPAB,CPBA to B _n ,A _n		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 7	
t _{PHL} /	propagation delay_SAB,SBA to Bn,An		55 20 16	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 8	
t _{PZH} / t _{PZL}	3-state output enable time \overline{OE} to $\overline{A}_n, \overline{B}_n$		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9	
t _{PHZ} /	3-state output disable time OE to $\overline{A}_n, \overline{B}_n$		61 22 18	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9	
t _{PZH} /	3-state output enable time DIR to $\overline{A}_n, \overline{B}_n$		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 10	
t _{PHZ} /	3-state output disable time DIR to $\overline{A}_n, \overline{B}_n$		55 20 16	175 35 30	D'	220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 10	
t _{THL} /	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 6 and 8	
tw	clock pulse width HIGH or LOW CPAB or CPBA	80 16 14	25 9 7	1	100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
t _{su}	set-up time A _n ,B _n to CP _{AB} ,CP _{BA}	60 12 10	0 0 0	15	75 15 13		90 18 15	0-	ns	2.0 4.5 6.0	Fig. 7	
th	hold time A _n ,B _n to CP _{AB} ,CP _{BA}	35 7 6	6 2 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 7	
f _{max}	maximum clock pulse frequency	6.0 30 35	22 68 81	ensup.	4.8 24 28	⊒ 8 g	4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
SAB, SBA Ao to A7)	0.60
\overline{B}_0 to \overline{B}_7	0.75

INPUT	UNIT LOAD COEFFICIENT
CPAB, CPBA OE DIR	1.50 1.50 1.25

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

					T _{amb} (°C)				TEST CONDITIONS		
0)/140.01	PARAMETER				74HCT				- ·	.,	WAVEFORMS	
SYMBOL		+25		-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS		
	f. ma	min.	typ.	max.	min.	max.	min.	max.			ton sust -	
t _{PHL} /	propagation delay $\overline{A}_n, \overline{B}_n$ to $\overline{B}_n, \overline{A}_n$		14	27		34		41	ns	4.5	Fig. 6	, A E TURTUO
t _{PHL} /	propagation delay CPAB,CPBA to Bn,An		25	46		58	11,371	69	ns	4.5	Fig. 7	7251636
t _{PHL} /	propagation delay SAB,SBA to Bn,An		20	38		48	0.5	57	ns	4.5	Fig. 8	Fig. 8 output
t _{PZH} / t _{PZL}	3-state output enable time \overline{OE} to $\overline{A}_n, \overline{B}_n$		21	40		50		60	ns	4.5	Fig. 9	
t _{PHZ} / t _{PLZ}	$\frac{3\text{-state output disable time}}{\overline{\text{OE}}}$ to $\overline{A}_n, \overline{B}_n$		20	35		44		53	ns	4.5	Fig. 9	TURN SIG
tPZH/	3-state output enable time DIR to $\overline{A}_n, \overline{B}_n$	avolci state i	20	40		50		60	ns	4.5	Fig. 10	
t _{PHZ} /	3-state output disable time DIR to $\overline{A}_n, \overline{B}_n$		21	35		44	(2) _M (2)	53	ns	4.5	Fig. 10	TUTTUO ,
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Figs 6 and 8	
t _W	clock pulse width HIGH or LOW CPAB or CPBA	16	7		20		24		ns	4.5	Fig. 7	TURTUD "A
t _{su}	set-up time Ā _n ,B̄ _n to CP _{AB} ,CP _{BA}	12	2		15		18		ns	4.5	Fig. 7	memo "8
th	hold time $\overline{A}_{n}, \overline{B}_{n}$ to CP_{AB}, CP_{BA}	5	0		5		5	1 14-	ns	4.5	Fig. 7	
f _{max}	maximum clock pulse frequency	30	80		24	catesx.	20	4	MHz	4.5	Fig. 7	Theybo 98

AC WAVEFORMS

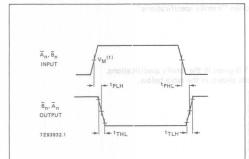


Fig. 6 Waveforms showing the input $\overline{A}_n, \overline{B}_n$ to output $\overline{B}_n, \overline{A}_n$ propagation delays and the output transition times.

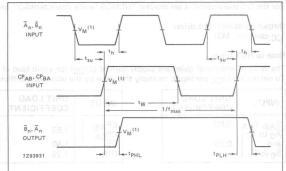


Fig. 7 Waveforms showing the \overline{A}_n , \overline{B}_n to CP_{AB} , CP_{BA} set-up and hold times; clock CP_{AB} , CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB} , CP_{BA} to output \overline{B}_n , \overline{A}_n propagation delays.

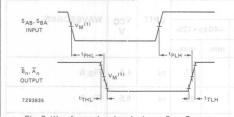


Fig. 8 Waveforms showing the input SAB.SBA to output $\overline{B}_n,\overline{A}_n$ propagation delays and output transition times.

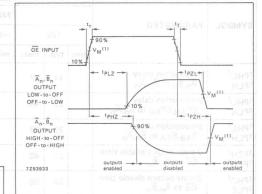


Fig. 9 Waveforms showing the input \overline{OE} to output \overline{A}_{n} , \overline{B}_{n} 3-state enable and disable times.

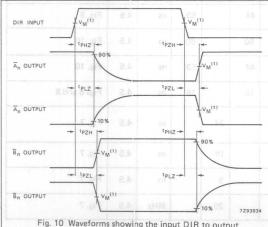
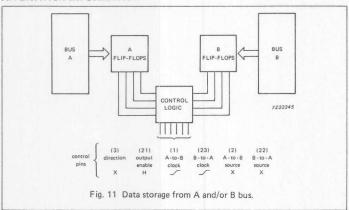


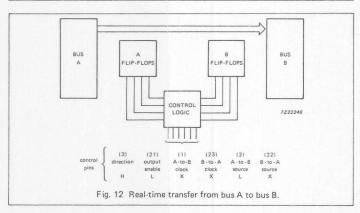
Fig. 10 Waveforms showing the input DIR to output \overline{A}_n , \overline{B}_n 3-state enable and disable times.

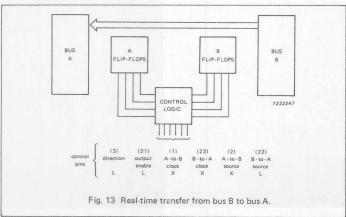


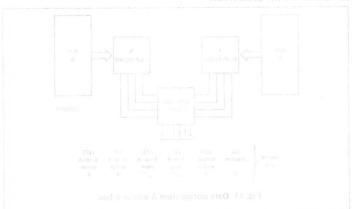
(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_{M} = 1.3 \text{ V}$; $V_{I} = \text{GND to } 3 \text{ V}$.

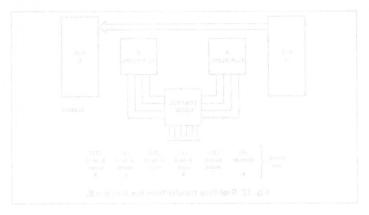
APPLICATION INFORMATION

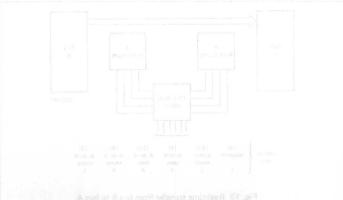












Octal bus transceiver/register; 3-state

74HC/HCT652

FEATURES

- Multiplexed real-time and stored data
- Independent register for A and B buses
- Independent enables for A and B buses
- · 3-state
- · Output capability: Bus driver
- Low power consumption by CMOS technology
- · Icc category: MSI.

APPLICATIONS

· Bus interfaces.

DESCRIPTION

The 74HC/HCT652 are high-speed SI-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with Jedec standard no. 7A.

The 74HC/HCT652 consist of 8 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and central circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the "A" or "B" or both buses, will be stored in the internal registers, at the appropiate clock pins (CPAB or CP_{BA}) regardless of the select pins $(S_{AB} \text{ and } S_{BA})$ or output enable $(OE_{AB} \text{ and } \overline{OE}_{BA})$ control pins. Depending on the select inputs SAB and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the output enable pins this operating mode permits. The output enable pins OEAB and OEBA determine the operation mode of the transceiver. When OEAB is LOW, no data transmission from A, to B, is possible and when \overline{OE}_{RA} is HIGH, there is no data transmission from B_n to A_n possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns; $V_{CC} = 4.5$ V; $C_L = 50$ pF.

SYMBOL	PARAMETER	CONDITIONS	TYP	ICAL	UNIT	
STIVIBUL	PANAMETER	-impedance	НС	нст	nil aud 1	
ene Juquo Iqri atab A	propagation delay A _n /B _n to B _n /A _n	This type		13	ns	
t _{PLH} /t _{PHL}	propagation delay CP _{AB} /CP _{BA} to B _n /A _n	function. transfer	18	20	ns	
	propagation delay S_{AB}/S_{BA} to B_n/A_n	B' bus and to the "A" The			ns	
t _{PZH} /t _{PZL}	3-state output enable time OE _{AB} /OE _{BA} to B _n /A _n	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	14	15		
t _{PHZ} /t _{PLZ}	3-state output disable time OE _{AB} /OE _{BA} to B _n /A _n	t the clock t highly rise and fall		kes tire	ns	
f _{max}	maximum clock frequency		92	92	MHz	
Cı	input capacitance	20V 148	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per channel	notes 1 and 2	26	28	pF	

Notes

- 1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W): $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V;
- Σ (C_L x V_{CC}² x f_o) = sum of the outputs. 2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} - 1.5 V

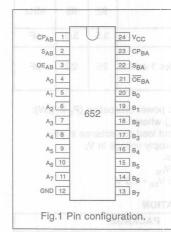
ORDERING AND PACKAGE INFORMATION

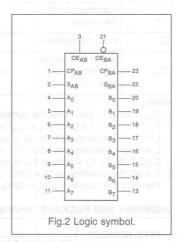
TYPE NUMBER	FIGAZ EX	PA	PACKAGE				
THE NOMBER	PINS	PIN POSITION	MATERIAL	CODE			
74HC/HCT652N	24	DIL	plastic	SOT101L			
74HC/HCT652D	24	SO	plastic	SOT137A			

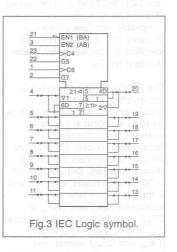
D-type flip-flops by simultaneously enabling OE_{AB} and OE_{BA}. In this configuration each output reinforces its input. Thus when all other data sources to the two sets of bus lines are at high-impedance, each set of the bus lines will remain at its last state. This type differs from the HC/HCT646 in one extra bus-management function. This is the possibility to transfer stored "A" data to the "B" bus and transfer stored "B" data to the "A" bus at the same time. The examples at the application information demonstrate all bus management functions. Schmitt-trigger action in the clock inputs makes the circuit highly tolerant to slower clock rise and fall times.

PINNING

SYMBOL	PIN	DESCRIPTION
CP _{AB}	1	A to B clock input
S _{AB}	2	select A to B source input
OE _{AB}	3	output enable A to B input
A ₀ A ₇	411	A data inputs/outputs
GND	12	ground (0 V)
B ₇ B ₀	1320	B data inputs/outputs
OE _{BA}	21	output enable B to A input
S _{BA}	22	select B to A source input
CP _{BA}	23	B to A clock input
V _{cc}	24	positive supply voltage







Octal bus transceiver/register; 3-state sta 8 netalger/neview 74HC/HCT652

FUNCTION TABLE

		INPU	TS			DATA	A I/O *	OPERATION OR FUNCTION
OEAB	OEBA	CPAB	CP _{BA}	SAB	SBA	A ₁ THRU A ₈	B ₁ THRU B ₈	HC/HCT652
L	Н	H or L	H or L	X	X	lan. d	Innut	Isolation
L	Н	1	1	X	X	Input	Input	Store A and B data
X	Н	1	H or L	X	X	Input	Not specified	Store A, Hold B
Н	Н	1	1	L	X	Input	Output	Store A in both registers
L	Χ	H or L	1	X	X	Not specified	Input	Hold A, Store B
L	L	1	1	X	L	Output	Input	Store B in both registers
L	L	X	X	Х	L	Output	Immud	Real Time B Data to A Bus
L	L	X	H or L	X	Н	Output	Input	Stored B Data to A Bus
Н	Н	X	X	L	X	Innut	Output	Real Time A Data to B Bus
Н	Н	H or L	X	Н	X	Input	Output	Stored A Data to B Bus
Н	L	H or L	H or L	Н	Н	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

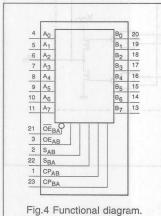
The data output functions may be enabled or disabled by various signals at \overline{OE}_{BB} inputs. Data input functions are always enabled, i.e., data at the bus inputs will de stored on every LOW-to-HIGH transition on the clock inputs.

H = HIGH voltage level

L = LOW voltage level

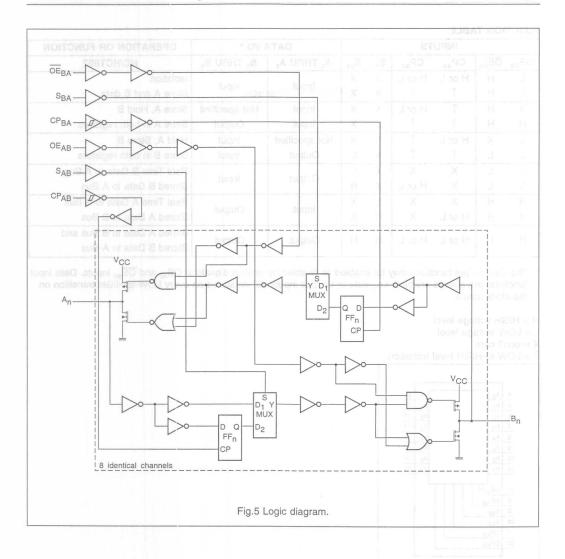
X = don't care

↑ = LOW-to-HIGH level transition



Octal bus transceiver/register; 3-state ala 8 malaige movies

74HC/HCT652



Octal bus transceiver/register; 3-state siz-8 policiper/review 74HC/HCT652

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Output capability: bus driver I_{cc} category: MSI.

AC CHARACTERISTICS FOR 74HC GND = 0 V: t = t = 6 ns: C₁ = 50 pF.

	n in the table below.	show	licient	leop bi	T _{amb} (°	C)	d sulav	aldt vi	geturni	,iuq	TEST CONDITIONS
SYMBOL	PARAMETER		+25		-40 t	0 +85	-40 to	+125	UNIT	V _{cc}	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	T	(V)	WAVEFORMS
	propagation dolay	-	44	135	-	170	-	205	1	2.0	GV-0 48 48
t_{PHL}/t_{PLH}	propagation delay	-	16	27	-	34	-	41	ns	4.5	Fig.6
	A_n , B_n to B_n , A_n	-	13	23	-	29	_	35		6.0	d 0.76
	propagation delay	-	61	190	-	240	-	285		2.0	,8 of
t _{PHL} /t _{PLH}		-	22	38	-	48	-	57	ns	4.5	Fig.7
	CP _{AB} , CP _{BA} to B _n , A _n	-	18	32	-	41	_	48	1000	6.0	710 x
		-	63	195	-	245	_	295		2.0	
t _{PHL} /t _{PLH}	propagation delay	_	23	39	-	49	_	59	ns	4.5	Fig.8
THE TEN	S_{AB} , S_{BA} to B_n , A_n	-	18	33	-	42	_	50		6.0	
	3-state output enable	-	47	150	_	190	-	225	= 50	2.0	n 8 = J = J .V 0 = 0
t _{PZH} /t _{PZL}	time	-	17	30	7250A	38	-	45	ns	4.5	Fig.9
120 120	OE _{AB} , \overline{OE}_{BA} to A _n , B _n	-	14	26	(0.7	33		38		6.0	
SWELL	3-state output disable	081	41	150	T 01	190	- 99	225		2.0	HETOMARA9 JOSH
t _{PHZ} /t _{PLZ}	time (V)	.XA	15	30	ANN J	38	MM-9Y	45	ns	4.5	Fig.9
	OE _{AB} , OE _{BA} to A _n , B _n	-	12	26	-	33	-	38		6.0	noitspagarq
		-	14	60	-	75	_	90		2.0	- Bot B LA No
t _{THL} /t _{TLH}	output transition time	-	5	12	-	15	T F	18	ns	4.5	Figs 6, 8
	Vigni die Ten	-80	4	10	-	13	- 63	15	,A	6.0	EFRIH OP IN CP EN B
	clock pulse width	80	17	-	100	-	120	-		2.0	nedspagero
t _w	HIGH or LOW	16	6		20	1 9	24	-	ns	4.5	Fig.7
	CP _{AB} or CP _{BA}	14	5	-	17	-	20	-	eld	6.0	John offste-E
	set-up time	100	17	-	125	8	150			2.0	emit make
t _{su}		20	6	-	25	-	30	-	ns	4.5	
	A_n , B_n to CP_{AB} , CP_{BA}	17	5	-	21	-	26	-	alde	6.0	Garage output
	hold time	25	-8	-	30	- + 8	35			2.0	emit selfes
t _h	A _n , B _n to CP _{AB} , CP _{BA}	5	-3	-	6	-	7	-	ns	4.5	Fig.7
	n, Dn to OI AB, OF BA	4	-2	7.7	5	7.5	6	-	em	6.0	tienen fuutuol
	maximum clock pulse	6.0	16	-	4.8	-	4.0	-	+	2.0	u dolum slambi
f _{max}	frequency frequency	30	83	-	24	ic T	20	-0.5	MHz	4.5	Fig.7
	requericy	35	98	-	28	-	24	-	1 1 3	6.0	90 to 90

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Output capability: bus driver I_{CC} category: MSI.

Note to the HCT types

The value of additional quiescent supply current (Δl_{CC}) for a unit load of 1 is given in the family specifications. To determine Δl_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
S _{AB} , S _{BA}	0.75
A ₀ to A ₇ and B ₀ to B ₇	8.6 Fig.6 0.0 27.0
CP _{AB} , CP _{BA}	1.50 Tel 8.4 ar
OE _{AB}	1.50
\overline{OE}_{BA}	1.50

AC CHARACTERISTICS FOR 74HCT

	AS A.5 Pig.9				T _{amb} (°C)				Т	EST CONDITIONS
SYMBOL	PARAMETER	açı	+25	- 10	-40 t	0 +85	-40 to	+125	UNIT	V _{cc}	WAVEFORMS
	ns 4.5 Fig.9	MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		(V)	WAVEFORIUS
t _{PHL} /t _{PLH}	propagation delay A _n , B _n to B _n , A _n	88	16	27	8	34	2 2	41	ns	4.5	Fig.6
t _{PHL} /t _{PLH}	propagation delay CP _{AB} , CP _{BA} to B _n , A _n	8)	23	39		49	7 0 1 p	59	ns	4.5	Fig.7
t _{PHL} /t _{PLH}	propagation delay S_{AB} , S_{BA} to B_n , A_n		27	46		55	- 1	66	ns	4.5	Fig.8
t _{PZH} /t _{PZL}	3-state output enable time OE_{AB} , \overline{OE}_{BA} to A_n , B_n		18	33	8	41	71	50	ns	4.5	Fig.9
t _{PHZ} /t _{PLZ}	3-state output disable time OE _{AB} , OE _{BA} to A _n , B _n		16	35	_	44	8	53	ns	4.5	Fig.9
t _{THL} /t _{TLH}	output transition time	-	5	12	-	15	-2	18	ns	4.5	Fig.6, 8
t _w	Clock pulse width HIGH or LOW CP _{AB} or CP _{BA}	16	6	-	20	2 2	24	36 S	ns	4.5	Fig.7suport
t _{su}	set-up time A _n , B _n to CP _{AB} , CP _{BA}	10	5	-	13	-	15	-	ns	4.5	Fig.7
t _h	hold time A _n , B _n to CP _{AB} , CP _{BA}	5	-2	-	6	-	8	-	ns	4.5	Fig.7
f _{max}	maximum clock pulse frequency	30	83	-	24	-	20	-	MHz	4.5	Fig.7

Octal bus transceiver/register; 3-state

74HC/HCT652

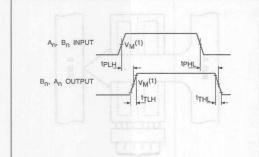


Fig.6 Waveforms showing the input A_n , B_n to output B_n , A_n propagation delay times and the output transition times.

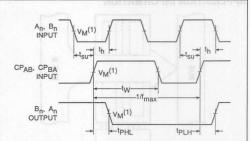


Fig.7 Waveforms showing the A_n , B_n to CP_{AB} , CP_{BA} set-up and hold times, clock CP_{AB} , CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB} , CP_{BA} to output B_n , A_n propagation delays.

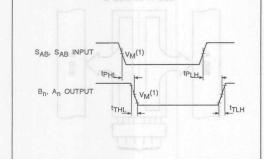


Fig.8 Waveforms showing the input S_{AB} , S_{BA} to output B_n , A_n propagation delay times and the output transition times.

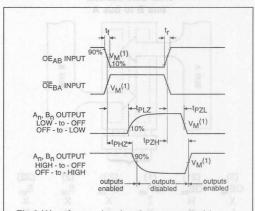
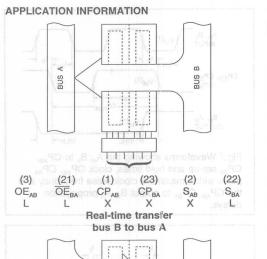


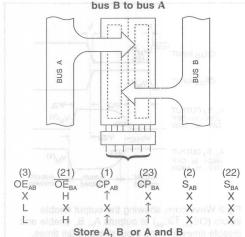
Fig.9 Waveforms showing the output enable inputs (\overline{OE}_{AB} , \overline{OE}_{BA}) to outputs A_n , B_n enable and disable times and the input rise and fall times.

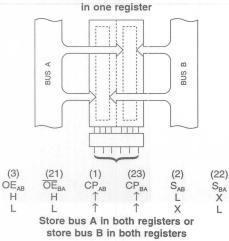
Note to the AC waveforms

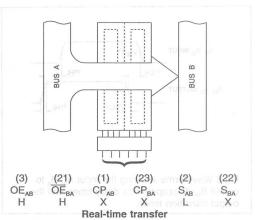
(1) HC: $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3$ V; $V_I = GND$ to 3 V.

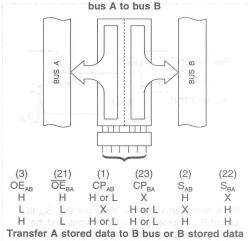
Octal bus transceiver/register; 3-state sta-8 petalogomevias 74HC/HCT652

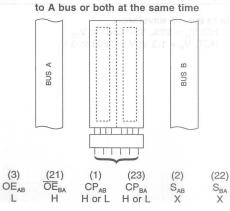












4 x 4 REGISTER FILE: 3-STATE

FEATURES

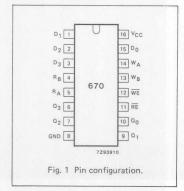
- Simultaneous and independent read and write operations
- Expandable to almost any word size and bit length
- Output capability: bus driver

GENERAL DESCRIPTION

The 74HC/HCT670 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT670 are 16-bit 3-state register files organized as 4 words of 4 bits each. Separated read and write address inputs (R_A, R_B and W_A, W_B) and enable inputs (RE and WE) are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs (D $_0$ to D $_3$). The W $_A$ and W $_B$ inputs determine the location of the stored word. When the WE input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the WE input is LOW. Data supplied at the inputs will be read out in true (noninverting) form from the 3-state outputs (Ω_0 to Ω_3). D_n and W_n inputs are inhibited when \overline{WE} is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual read address inputs (R $_{A}$ and R $_{B}$). The addressed word appears at the four outputs when the RE is LOW. Data outputs are in the high impedance OFF-state when RE is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

(continued on next page)



SYMBOL	PARAMETER	CONDITIONS	TYF	PICAL	115117
n aspiyab be	Punta .	CONDITIONS	нс	нст	UNIT
t _{PHL} /	propagation delay D _n to Q _n	C _L = 15 pF V _{CC} = 5 V	23	23	ns
Cl	input capacitance	ONA ZHIÇTEJ SUR ENABLE COUIC	3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	122	124	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

 $PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$ where:

 $\begin{array}{ll} f_i &=& \text{input frequency in MHz} \\ f_0 &=& \text{output frequency in MHz} \\ \Sigma \; (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs} \end{array}$

 C_L = output load capacitance in pF V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

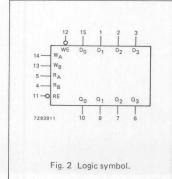
PACKAGE OUTLINES

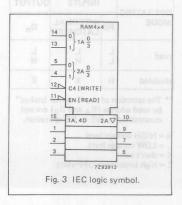
16-lead DIL; plastic (SOT38Z).

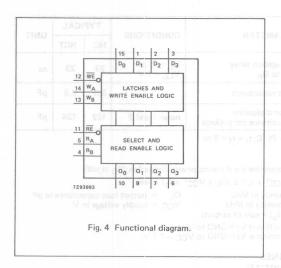
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
5, 4 8	R _A , R _B	read address inputs ground (0 V)
10, 9, 7, 6	Q ₀ to Q ₃	data outputs
11	RE	3-state output read enable input (active LOW)
12	WE	write enable input (active LOW)
14, 13	WA, WB	write address inputs
15, 1, 2, 3	D ₀ to D ₃	data inputs
16	Vcc	positive supply voltage







GENERAL DESCRIPTION (Cont'd)

Design of the read enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the enable and address inputs of each device in parallel.

WRITE MODE SELECT TABLE

OPERATING	INP	UTS	INTERNAL
MODE	WE	D _n	LATCHES*
write data	L L	L H	L H (V 0)
data latched	Н	X	no change

* The write address (W_A and W_B) to the "internal latches" must be stable while WE is LOW for conventional operation.

READ MODE SELECT TABLE

OBEDATING		INPUTS	OUTPUT
OPERATING MODE	RE	INTERNAL LATCHES**	Qn
read	L L	L H	L H
disabled	Н	X	Z

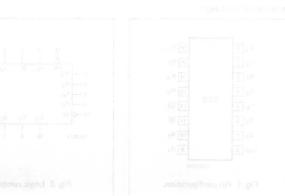
** The selection of the "internal latches" by read address (RA and RB) are not constrained by WE or RE operation.

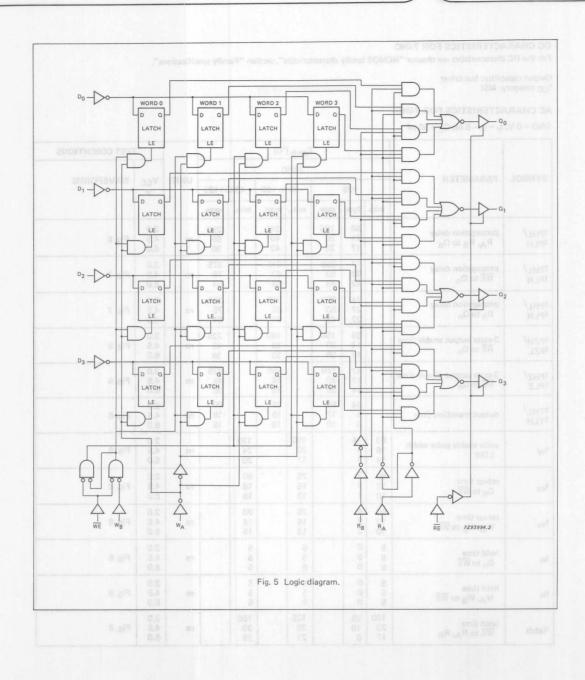
H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

					T _{amb} (°C)) 				TEST CONDITIONS
		74HC								.,	WAVEFORMS
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		ATER	
t _{PHL} /	propagation delay R _A , R _B to Q _n		58 21 17	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6
t _{PHL} /	propagation delay WE to On		77 28 22	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 7
t _{PHL} /	propagation delay D _n to Q _n		74 27 22	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 7
t _{PZH} /	3-state output enable time RE to Qn		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t _{PHZ} /	3-state output disable time RE to Qn		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
tW	write enable pulse width LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t _{su}	set-up time D _n to WE	60 12 10	3 1 1		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t _{su}	set-up time W _A , W _B to WE	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t _h	hold time D _n to WE	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
th	hold time W _A , W _B to WE	5 5 5	0 0	TIETHS	5 5 5	1 d _g/2	5 5 5		ns	2.0 4.5 6.0	Fig. 8
[†] latch	latch time WE to R _A , R _B	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D _n WE, W _A	0.25 0.40
WB	0.60

INPUT	UNIT LOAD COEFFICIENT
RA	0.70
RR	1.10
RE	1.35

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		T _{amb} (°C)									TEST CONDITIONS	
	BARAMETER.	74HCT					UNIT	\/				
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
093311	cluble output performance.	min.	typ.	max.	min.	max.	min.	max.			- 147	
tPHL/	propagation delay R _A , R _B to Ω _n	Sawed tett st who who	21	40		50		60	ns	4.5	Fig. 6	
t _{PHL} /	propagation delay WE to Qn	mediar his par	28	50		63	9- 67-	75	ns	4.5	Fig. 7	
t _{PHL} /	propagation delay D _n to Q _n	LOW	27	50		63		75	ns	4.5	Fig. 7	
t _{PZH} /	$\frac{3\text{-state output enable time}}{\text{RE to }\Omega_n}$		18	35		44		53	ns	4.5	Fig. 9	
t _{PHZ} /	3-state output disable time \overline{RE} to Ω_n	tab bo to both	19	35		44	Patr	53	ns	4.5	Fig. 9	
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6	
t _W	write enable pulse width LOW	18	9		23		27	T.	ns	4.5	Fig. 8	
t _{su}	set-up time D _n to WE	12	4		15		18		ns	4.5	Fig. 8	
t _{su}	set-up time W _A , W _B to WE	12	-2		15		18		ns	4.5	Fig. 8	
t _h	hold time D _n to WE	5	-1		5		5	150° +	ns	4.5	Fig. 8	
t _h	hold time W _A , W _B to WE	5	0		5		5		ns	4.5	Fig. 8	
^t latch	latch time WE to RA, RB	25	11		31	(138) belo	38	100	ns	4.5	Fig. 8	

AC WAVEFORMS

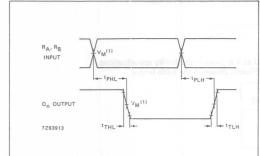


Fig. 6 Waveforms showing the read address input (R_A , R_B) to output (C_n) propagation delays and output transition times.

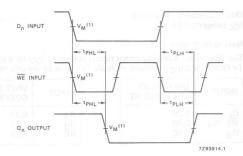
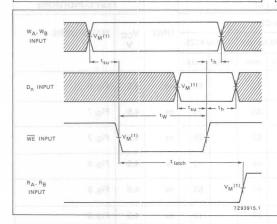


Fig. 7 Waveforms showing the write enable input (WE) and data input (D_n) to output (Q_n) propagation delays, and the write enable pulse width.



Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

The time allowed for the internal output of the latch to assume the state of the new data (1_{latch}) is important only when attempting to read from a location immediately after that location has received new data. This parameter is measured from the falling edge of WE to the rising edge of RA or RB, RE must be LOW.

Fig. 8 Waveforms showing the write address input (W_A, W_B) and data input (D_n) to write enable (\overline{WE}) set-up, hold and latch times.

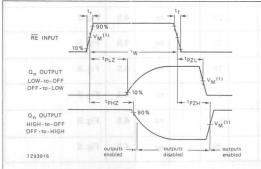


Fig. 9 Waveforms showing the read enable ($\overline{\text{RE}}$) to output (Ω_{D}) enable and disable times, and the read enable pulse width.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

8-BIT MAGNITUDE COMPARATOR

FEATURES

- Compare two 8-bit words
- Output capability: standard
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT688 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT688 are 8-bit magnitude comparators. They perform comparison of two 8-bit binary or BCD words.

The output provides $\overline{P} = \overline{Q}$.

SYMBOL	242445752	CONDITIONS	TYF	UNIT	
	PARAMETER	CONDITIONS	НС	нст	UNII
tPHL/ tPLH	propagation delay $P_{n}, \Omega_{n} \text{ to } \overline{P} = \overline{\Omega}$ E to $\overline{P} = \overline{\Omega}$	C _L = 15 pF V _{CC} = 5 V	17 8	17 12	ns ns
C _I	input capacitance		3.5	3.5	pF
CPD power dissipation capacitance per package		notes 1 and 2	30	30	pF

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

Notes

- 1. CPD is used to determine the dynamic power dissipation (PD in μ W): PD = CPD x VCC² x f₁ + Σ (CL x VCC² x f₀) where:
 - fi = input frequency in MHz fo = output frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

 Σ (C_L × V_{CC}² × f_O) = sum of outputs

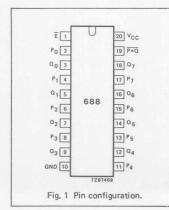
2. For HC the condition is $V_I = GND$ to V_{CC} For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5$ V

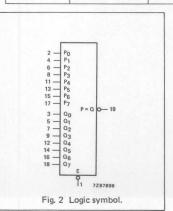
PACKAGE OUTLINES.

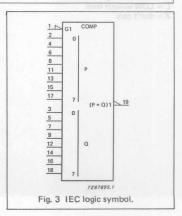
20-lead DIL; plastic (SOT146). 20-lead mini-pack; plastic (SO20; SOT163A).

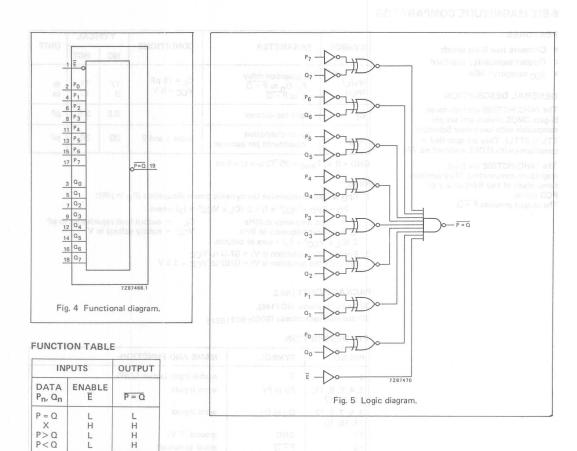
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION				
1 0<- 1	Ē	enable input (active LOV	V)	HAL		
2, 4, 6, 8, 11, 13, 15, 17	P ₀ to P ₇	word inputs				
3, 5, 7, 9, 12, 14, 16, 18	Q ₀ to Q ₇	word inputs				
10	GND	ground (0 V)				
19	$\overline{P} = \overline{Q}$	equal to output				
20	Vcc	positive supply voltage				









H = HIGH voltage level L = LOW voltage level

X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

				T _{amb} (°C)							TEST CONDITIONS						
CVAADOL	DADAMETER						74H	С	He.			ENT	COEFFIC	INPUT			
SYMBOL PARAMETER				+25		-40	to +85	-40 t	o +125	UNIT	VCC	WAVEFORM	10 10				
			n	in.	typ.	max.	min.	max.	min.	max.			0.35				
t _{PHL} /	propagation de P _n , Q _n to P =	elay = Q			55 20 16	170 34 29		215 43 37		255 51 43	ns TOHA	2.0 4.5 6.0	Fig. 6	ARAHO S			
tPHL/	propagation de E to P = Q	elay			28 10 8	120 24 20	24	24	24	(D°)	150 30 26		180 36 ns 31	ns	2.0 4.5 6.0	0 ten 8 = yt = yt; V 8 = 00 Fig. 7	
tTHL/ tTLH	output transiti	on time	THE	35	19 7 6	75 15 13	TOI 8+ or (95 19 16	-	110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7	YMBOL			
							43										

-bit magnituda comparater

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
Pn	0.35
Qn	0.35
Ē.	0.70

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	0.8	T _{amb} (°C)			8		TEST CONDITIONS				
SYMBOL	PARAMETER	0	11		74H0	СТ	27	er	UNIT		WAVEFORMS
STIVIBUL	MBOL PARAMETER		+25		-40 to +85 -40		-40 t	-40 to +125		V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} /	propagation delay P_n , Q_n to $\overline{P} = \overline{Q}$		20	34		43		51	ns	4.5	Fig. 6
t _{PHL} /	$\frac{\text{propagation delay}}{\text{E to P = Q}}$		18	24		30		36	ns	4.5	Fig. 7
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

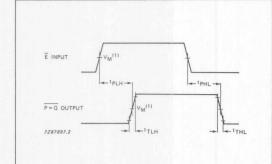


Fig. 6 Waveforms showing the enable input (\overline{E}) to the equal to output $(\overline{P}=\overline{Q})$ propagation delays and the output transition times.

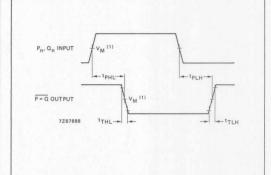


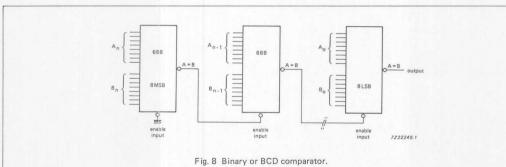
Fig. 7 Waveforms showing the word inputs (P_n, Q_n) to the equal to output ($\overline{P}=\overline{Q}$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

Two or more "688" 8-bit magnitude comparators may be cascaded to compare binary or BCD numbers of more than 8 bits. An example is shown in Fig. 8.



AC WAVEFORMS



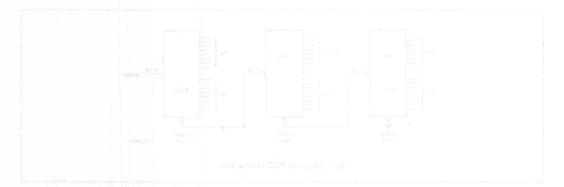


Fig. 7. Waveforms showing the word inputs $(P_{\rm H}, P_{\rm H})$ to the equal to output $(P \neq 0)$ propagation delays and the output, transition times.

Note to AL waveforms (1) HC + 1M = 50%; V₁

APPLICATION INFORMATION

Two or note "686" 8-bit magnitude o imparators may be discalled to compare binary or bCD numbers of more than 8 bits. An exemple is shown in Fig. 8.



DUAL 4-INPUT NOR GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT4002 are high-speed Si-gate CMOS devices and are pin compatible with "4002" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT4002 provide the 4-input NOR function.

	BURNETION FABRE	CONDITIONS	TYF		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
tPHL/ tPLH	propagation delay nA, nB, nC, nD to nY	C _L = 15 pF V _{CC} = 5 V	9	11	ns
CI	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per gate	notes 1 and 2	16	22	pF

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

f_i = input frequency in MHz f_o = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} -1.5 V

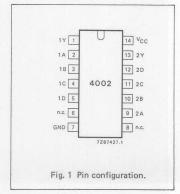
PACKAGE OUTLINES

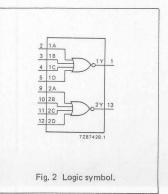
14-lead DIL; plastic (SOT27).

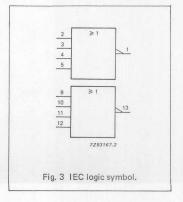
14-lead mini-pack; plastic (SO14; SOT108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1Y, 2Y	data outputs
2, 9	1A, 2A	data inputs
3, 10	1B, 2B	data inputs
4, 11	1C, 2C	data inputs
5, 12	1D, 2D	data inputs
6, 8	n.c.	not connected
7	GND	ground (0 V)
14	VCC	positive supply voltage







2 1A 3 1B 4 10 5 1D 9 2A 10 2B 11 20

Fig. 4 Functional diagram.

FUNCTION TABLE

	INP	OUTPUT		
nA	nB	nC	nD	nY
r _{A.u.}	en Ela i	m Lan .	L	H _{d2}
H X X	X H X	X X H X	X X X H	L I

H = HIGH voltage level

L = LOW voltage level

X = don't care

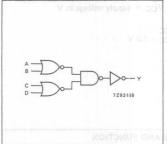


Fig. 5 Logic diagram 74HC4002 (one gate).

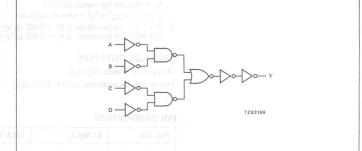
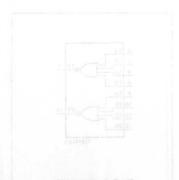


Fig. 6 Logic diagram 74HCT4002 (one gate).







DC CHARACTERISTICS FOR 74HC

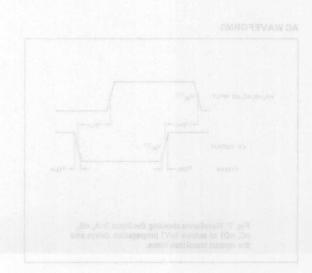
For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \ V$; $t_r = t_f = 6 \ ns$; $C_L = 50 \ pF$ which is the inverse of three sections and with a section of the section

	PARAMETER	T _{amb} (°C)								ah A	TEST CONDITIONS	
SYMBOL										TUENT	WAVEFORMS	
		+25		-40	-40 to +85 -40 to		o +125	UNIT	V _{CC}	WAVEFORMS An An		
		min.	typ.	max.	min.	max.	min.	max.			40,0	
t _{PHL} /	propagation delay nA, nB, nC, nD to nY		30 11 9	100 20 17		125 25 21		150 30 26	ns HA	2.0 4.5 6.0	Fig. 7.3TOARAHO	
t _{THL} //O	output transition time		19 7 6	75 15 13	(0°) (95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7	



DC CHARACTERISTICS FOR 74HCT

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: SSI

Output capability: standard

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

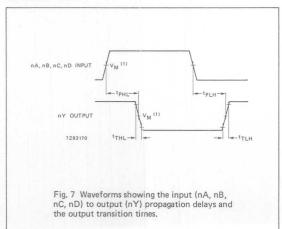
INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC, nD	0.45

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		101	T _{amb} (°C)				en	TEST CONDITIONS			
	0.8	I IS	74HCT							.,	WANTEGRAG
SYMBOL PARAME	PARAMETER		+25		-40 t	to +85	-40 t	o +125	UNIT	UNIT VCC WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} /	propagation delay nA, nB, nC, nD to nY		13	22		28		33	ns	4.5	Fig. 7
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 7

AC WAVEFORMS



Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL 4-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER

FEATURES

• Output capability: standard

· ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4015 are high-speed Si-gate CMOS devices and are pin compatible with the "4015" of the "40008" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4015 are dual edgetriggered 4-bit static shift registers (serial-to-parallel converters). Each shift register has a serial data input (1D and 2D), a clock input (1CP and 2CP), four fully buffered parallel outputs (1Q₀ to 1Q₃ and 2Q₀ to 2Q₃) and an overriding asynchronous master reset (1MR and 2MR). Information present on nD is shifted to the first register position, and all data in the register is shifted one position to the right on the LOW-to-HIGH transition of nCP. A HIGH on nMR clears the register and forces nQ₀ to nQ₃ to LOW, independent of nCP and nD.

SYMBOL	PARAMETER	CONDITIONS	TYF	UNIT		
STIVIBUL	PARAMETER	CONDITIONS	НС	нст	ONT	
tPHL/ 0 0 tPLH 10	propagation delay nCP to nΩ _n	C _L = 15 pF V _{CC} = 5 V	16	18	ns	
f _{max} maximum clock frequence		ACC = 2 A	110	74	MHz	
CI	input capacitance	Et ODS	3.5	3.5	pF	
CPD power dissipation capacitance per register		notes 1 and 2	35	40	pF	

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

f; = input frequency in MHz f_O = output frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

 Σ (C_L x V_{CC}² x f_o) = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

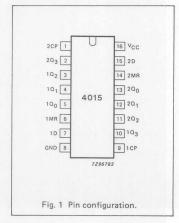
PACKAGE OUTLINES

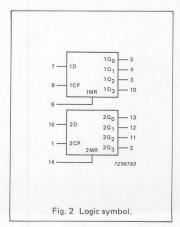
16-lead DIL; plastic (SOT38Z).

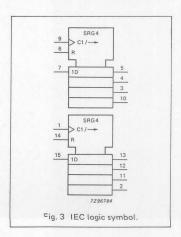
16-lead mini-pack; plastic (SO16; SOT109A).

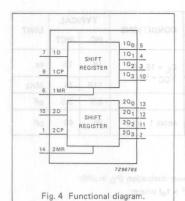
PIN DESCRIPTION

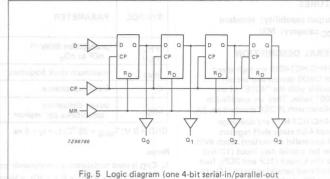
PIN NO.	SYMBOL	NAME AND FUNCTION
5, 4, 3, 10 6, 14	1Q ₀ to 1Q ₃ 1MR, 2MR	flip-flop outputs asynchronous master reset inputs (active HIGH)
7, 15 8	1D, 2D GND	serial data inputs ground (0 V)
9, 1	1CP, 2CP	ground (U V) clock inputs (LOW-to-HIGH, edge-triggered)
13, 12, 11, 2 16	2Q ₀ to 2Q ₃ V _{CC}	flip-flop outputs positive supply voltage











FUNCTION TABLE

	11	NPU	TS	OUTPUTS						
n	nCP	nD nMR D1 L D2 L D3 L D4 L		nQ ₀	nQ1	nΩ ₂	nQ3			
1 2 3 4	↑ ↑ ↑			D ₁ D ₂ D ₃ D ₄	X D ₁ D ₂ D ₃	X X D ₁ D ₂	X X X D ₁			
	×	X	Н	L	no cl	nange L	Lio e			

H = HIGH voltage level L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH clock transition ↓ = HIGH-to-LOW clock transition

n = number of clock pulse transitions

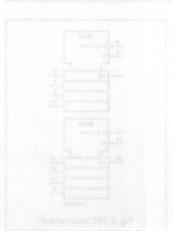
Dn = either HIGH or LOW and overlaged evisions

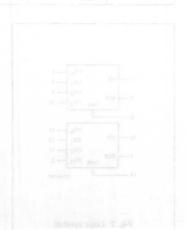
APPLICATIONS AND SHOP OF A

Serial-to-parallel converter

shift register).

- Buffer stores 25 ALTO 30 AND AS
- General purpose register







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

			T _{amb} (°C)							TEST CONDITIONS		
		74HC								TIA	COEFFICIEN	
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	Vcc	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			1.50	
t _{PHL} /	propagation delay nCP to nQ _n		52 19 15	175 35 30		220 44 37		265 53 45	ns _{Ra} c	2.0 4.5 6.0	Fig. 6	
tPHL 20	propagation delay nMR to nQ _n		44 16 13	175 35 30	a°) di Tahi	220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7	
t _{THL} /	output transition time	125 max.	19 7 6	75 15 13		95 19 16	+25 yp. a	110 22 19	ns	2.0 4.5 6.0	Fig. 6	
tW	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17	i	120 24 20		ns	2.0 4.5 6.0	Fig. 6	
tw	master reset pulse width	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
^t rem	removal time nMR to nCP 3.4	60 12 10	17 6 5	2	75 15 13		90 18 15	16	ns	2.0 4.5 6.0	Fig. 7 cots	
t _{su}	set-up time nD to nCP	60 12 10	8 3 2	8	75 15 13	2	90 18 15	81	ns data	2.0 4.5 6.0	Fig. 8	
th	hold time nD to nCP	5 5 5	0 0 0	17	5 5 5		5 5 5	12	ns	2.0 4.5 6.0	Fig. 8	
f _{max}	maximum clock pulse frequency	6.0 30 35	33 100 119	70	4.8 24 28	8	4.0 20 24	ie.	MHz	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle |_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle |_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	COEFFI	
nD 8	0.30	W 00
nMR	1.50	
nCP	1.50	

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

	2.0	285			Tamb	°C)				Т	EST CONDITION	IS
SYMBOL PARAMET		53	€8 74HCT 6€ 61 €8 €1						UNIT	Vac	WAVEFORMS	
	2.0	011	011 +25		-40 to +85		-40 to +125			V _{CC}		
	13 4.5 Fig. 5 6.0	min.	typ.	max.	min.	max.	min.	max.	90	13 110131		HJT [‡]
t _{PHL} /	propagation delay nCP to nQn		21	35	00	44	7	53	ns	4.5	Fig. 6	Wi
^t PHL	propagation delay nMR to nΩ _n		18	35	- 00	44	1	53	ns	4.5	Fig. 7	
t _{THL} /	output transition time		7	15		19		22	ns	4.5	Fig. 6	
t _W	clock pulse width HIGH or LOW	16	7	T T	20		24	12 16	ns	4.5	Fig. 6	rem
tw	master reset pulse width	16	5	9 .	20	(C)	24	60 12	ns	4.5	Fig. 7, see	Lie ¹
t _{rem}	removal time nMR to nCP	20	10	2	25	8	30	3 3	ns	4.5	Fig. 7	
t _{su}	set-up time nD to nCP	12	4	ā	15	ä	18	9 8	ns	4.5	Fig. 8	n'
t _h	hold time nD to nCP	5	-2	2	5	4 01 4	5 00	30	ns	4.5	Fig. 8	:XEITI
f _{max}	maximum clock pulse frequency	30	67		24		20		MHz	4.5	Fig. 6	

AC WAVEFORMS

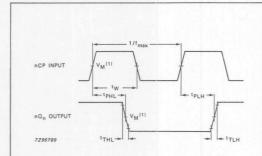


Fig. 6 Waveforms showing the clock (nCP) to output (nQ_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

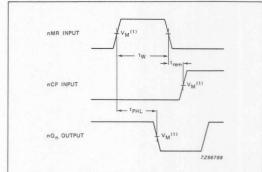


Fig. 7 Waveforms showing the master reset (nMR) pulse width, the master reset to output (nQ $_{n}$) propagation delay and the master reset to clock (nCP) removal time.

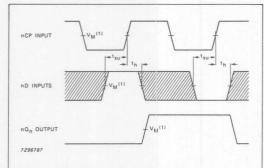


Fig. 8 Waveforms showing the data set-up and hold times for nD inputs.

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORW

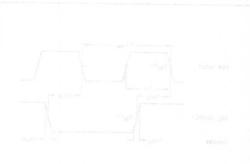


Fig. 6. Waveforms showing the clock. (now) to purport $(n\Omega_m)$ propagation delays, the clock pulse width, the purport transition times and the maximum clock frequency.





QUAD BILATERAL SWITCHES

FEATURES

- Low "ON" resistance: 160 Ω (typ.) at $V_{CC} = 4.5 \text{ V}$ 120 Ω (typ.) at V_{CC} = 6.0 V 80 Ω (typ.) at V_{CC} = 9.0 V
- Individual switch controls
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT4016 are high-speed Si-gate CMOS devices and are pin compatible with the "4016" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4016 have four independent analog switches (transmission gates).

Each switch has two input/output each switch has two inpurpotiput terminals (Y_n, Z_n) and an active HIGH enable input (E_n) . When E_n is connected to V_{CC} , a low bidirectional path between Y_n and Z_n is established (ON condition). When En is connected to ground (GND), the switch is disabled and a high impedance between Y_n and Z_n is established (OFF condition).

Current through a switch will not cause additional V_{CC} current provided the voltage at the terminals of the switch is maintained within the supply voltage range; $V_{CC} \gg (V_Y, V_Z) \gg GND$. Inputs Y_n and Z_n are electrically equivalent terminals.

APPLICA		CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	ONT	
t _{PZH} /	turn "ON" time E _n to V _{os}	C _L = 15 pF	16	17	ns	
t _{PHZ} / t _{PLZ}	turn "OFF" time E _n to V _{os}	$\begin{array}{c} C_L = 15 \text{ pF} \\ R_L = 1 \text{ k}\Omega \\ V_{CC} = 5 \text{ V} \end{array}$	14	20	ns	
CI	input capacitance	4 Functional diagram	3.5	3.5	pF	
C _{PD} power dissipation capacitance per switch		notes 1 and 2	12	12	pF	
CS	max. switch capacitance	THE	5	5	pF	

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$$
 where:

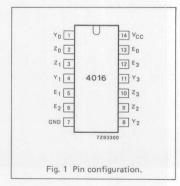
- f; = input frequency in MHz
- C_L = output load capacitance in pF C_S = max. switch capacitance in pF fo = output frequency in MHz $\Sigma \{(C_L + C_S) \times V_{CC}^2 \times f_0\} = \text{sum of outputs} \quad V_{CC} = \text{supply voltage in V}$
- 2. For HC the condition is VI = GND to VCC For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 V$

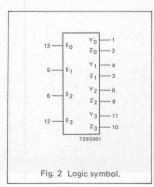
PACKAGE OUTLINES

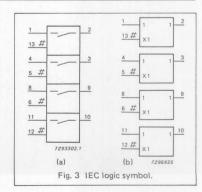
- 14-lead DIL; plastic (SOT27).
- 14-lead mini-pack; plastic (SO14; SOT108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11 7	Y ₀ to Y ₃ GND	independent inputs/outputs ground (0 V)
2, 3, 9, 10	Z ₀ to Z ₃	independent inputs/outputs
13, 5, 6, 12 14	E ₀ to E ₃	enable inputs (active HIGH) positive supply voltage







MUAD BILATERAL SWITCHES

• Chopper

APPLICATIONS

Signal gating
Modulation
Demodulation

PEATURES

- Low "ON" resistance: 160 Ω (typ) at V_{C1} = 4.5
- / 0.0 = 35V to Legyt) Ω 051
- V 0.0 = 50 V 16 (.473) 12 US
- a Individual switch controls
- Typical "break before make" buil
 - 122 permentan and at

SEMERAL DESCRIPTION

he 741C/HC74016 are high speed ligate CMOS devices and are his compatible with the "4616" of the 46008" saries. They are specified in combinate with LEDEC translated to 74

independent analog switches (transmi

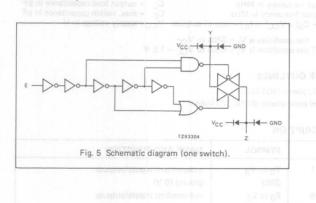
Each switch has two input/output termods (Y_D, Z_n) and an active HIGH sendous input $(E_0, W_{\rm HIGH})$ is connected to $V_{\rm CC}$, a low bidirectrional path between $V_{\rm CC}$ and $Z_{\rm CC}$ is subhished (ON conditional Waten E_0 is connected to ground (SND), the switch is disabled and a high subhished (SND). Impedence between $V_{\rm CC}$ and $Z_{\rm CC}$ is small dend (OFF) and $Z_{\rm CC}$ is exhibited (OFF).

Current through a switch will not coute additional Vpc current provided the voltage at the terminals of the switch is maintained within the supply voltage range; $Vpc \ge (VV, Vz) \ge GND$, heputs Y_n and Z_n are electrically

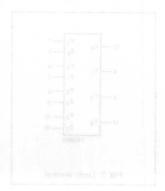
FUNCTION TABLE

INPUT	CHANNEL
En	IMPEDANCE
L	high
Н	low

H = HIGH voltage level L = LOW voltage level









RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
Vcc	DC supply voltage	-0.5	+11.0	V	SOLOW BELLEVIEW
±11K	DC digital input diode current	(1+678)	20	mA	for $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$
±1sK	DC switch diode current	ini ini	20	mA	for V_S < -0.5 V or V_S > V_{CC} + 0.5 V
±IS	DC switch current	-	25	mA	for -0.5 V < V _S < V _{CC} + 0.5 V
±ICC; ±IGND	DC V _{CC} or GND current	36	50	mA	ON ON resistance (prek) 120 240 250 240 250 240 250 240 250 250 250 250 250 250 250 250 250 25
T _{stg}	storage temperature range	-65	+150	°C	- 08r
P _{tot}	power dissipation per package	12 31	178		for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL	-	750	mW	above +70 °C: derate linearly with 12 mW/K
10 O	plastic mini-pack (SO)	24	500	mW	above +70 °C: derate linearly with 8 mW/K
PS	power dissipation per switch		100	mW	

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74HC			74HC1		LIMIT	CONDITIONS
STIVIBUL	paralleler Therefore It is reco	min.	typ.	max.	min.	typ.	max.	UNIT	CONDITIONS
Vcc	DC supply voltage	2.0	5.0	10.0	4.5	5.0	5.5	VFI ppi	For test circuit massu
VI	DC input voltage range	GND		Vcc	GND		Vcc	V	
٧s	DC switch voltage range	GND		Vcc	GND		Vcc	V	
T _{amb}	operating ambient temperature range	-40		+85	-40	262	+85	°C	see DC and AC
T _{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	CHARACTERISTICS
t _r , t _f	input rise and fall times one		6.0	1000 500 400 250	995 - 35 ¹	6.0	500	ns	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V V _{CC} = 10.0 V

DC CHARACTERISTICS FOR 74HC/HCT

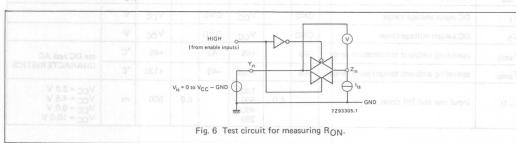
For 74HC: V_{CC} = 2.0, 4.5, 6.0 and 9.0 V For 74HCT: V_{CC} = 4.5 V

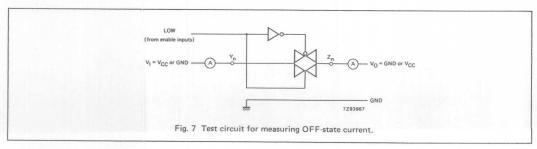
				inoa	Γ _{amb} (°C)	M JA	IM		g J	EST CO	NDITIO	NS
SYMBOL	PARAMETER			7	4HC/F	ICT	+ 8.	0-	UNIT	voltage	Is	Q.	vio
STINBUL	V 8.0 + 20 V < IV	6 V a	+25	V oot	-40 t	o +85	-40 to	+125	erro sb	VCC	μA	Vis	NI.
	Vs>Vcc+0.5 V	min.	typ.	max.	min.	max.	min.	max.	Thorn	diode cu	rfotriwa 2	00	held
R _{ON}	ON resistance (peak)	aV.	160 120 85	320 240 170	Am	- 400 300 213	3	- 480 360 255	Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	V _{CC} to GND	V _{IH} or V _{IL}
RON	ON resistance (rail)	81 8100	160 80 70 60	- 160 140 120	D)	200 175 150	+ 3	240 210 180	ΩΩΩ	2.0 4.5 6.0 9.0	100 1000 1000 1000	GND	V _{IH} or V _{IL}
RON	ON resistance (rail)		170 90 80 65	180 160 135	Wes	225 200 170	3	270 240 205	Ω Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	Vcc	V _{IH} or V _{IL}
ΔRON	maximum ΔΟΝ resistance between any two channels		16 12 9		Wervi	100		RIONS	Ω Ω Ω	2.0 4.5 6.0 9.0	1390 (VCC to GND	VIH or VIL

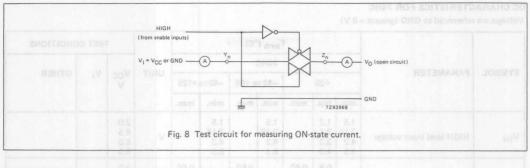
Notes to DC characteristics

1. At supply voltages approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

2. For test circuit measuring RON see Fig. 6.







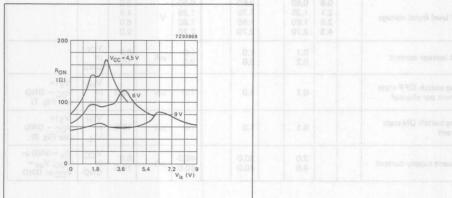


Fig. 9 Typical $R_{\mbox{ON}}$ as a function of input voltage $V_{\mbox{is}}$ for $V_{\mbox{is}}$ = 0 to $V_{\mbox{CC}}.$

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

				N.	Tamb (°C)		Lesione			TEST C	ONDITIONS
SYMBOL	PARAMETER	-(3)-	-6	1	74H0	;	6—E) ani	10 53V = V	.,	.,	OTHER
SAMBOL	PARAMETER		+25		-40 to +85 -40 to +125			+125 UNIT		V _{CC}	VI	OTHER
	CMD	min.	typ.	max.	min.	max.	min.	max.				
V _{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.3	e-VIO gr	1.5 3.15 4.2 6.3	n for n	1.5 3.15 4.2 6.3	T 8 pi	V	2.0 4.5 6.0 9.0		
VIL	LOW level input voltage		0.8 2.1 2.8 4.3	0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70	V	2.0 4.5 6.0 9.0		
±II	input leakage current			0.1 0.2		1.0		1.0 2.0	μΑ	6.0 10.0	V _{CC} or GND	
±IS	analog switch OFF-state current per channel			0.1		1.0		1.0	μА	10.0	V _{IH} or V _{IL}	IV _S I = V _{CC} - GND (see Fig. 7)
±IS	analog switch ON-state current			0.1		1.0		1.0	μА	10.0	V _{IH} or V _{IL}	IV _S I = V _{CC} - GND (see Fig. 8)
^I cc	quiescent supply current			2.0 4.0		20.0 40.0		40.0 80.0	μΑ	6.0 10.0	V _{CC} or GND	V _{is} = GND o V _{CC} ; V _{os} = V _{CC} or GNE

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V; } t_r = t_f = 6 \text{ ns; } C_L = 50 \text{ pF}$

					T _{amb} (°C)					TEST CONDITIONS
CVMADOL	DADAMETER				74H				LINUT		OTHER
SYMBOL	PARAMETER		+ 25		-40	to +85	-40 t	o + 125	UNIT	V _{CC}	OTHER
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} /	propagation delay V _{is} to V _{os}		17 6 5 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 9.0	R _L = ∞; C _L = 50 pF (see Fig. 16)
t _{PZH} / t _{PZL}	turn "ON" time E _n to V _{os}		52 19 15 11	190 38 32 28		240 48 41 35		235 57 48 42	ns	2.0 4.5 6.0 9.0	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 17 and 18)
t _{PHZ} /	turn "OFF" time E _n to V _{OS}		47 17 14 13	145 29 25 22		180 36 31 28		220 44 38 33	ns	2.0 4.5 6.0 9.0	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 17 and 18)

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

	rest conpr				Tamb (°C)					TEST CO	ONDITIONS	S
					74HC	т			LIAUT		V	OTHER	
SYMBOL	PARAMETER	126	+25	LIne	-40 t	to +85	-40 to	+125	UNIT	VCC	VI _{MA}	OTHER	
		min.	typ.	max.	min.	max.	min.	max.					
V _{IH} ³ q 08 a	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5	noitapa 10 V ₀₅		PTH ₁
VIL	LOW level input voltage	152	1.2	0.8	44	0.8	E 6	0.8	٧	4.5 to 5.5	ao V oz		HZ4 ₁
(87 5m) 1 = 80 pt± 18)	input leakage current	88		0.1	i a	1.0	E E	1.0	μΑ	5.5	V _{CC} or GND	1,2	724
±1 _S	analog switch OFF-state current per channel			0.1		1.0		1.0	μА	5.5	V _{IH} or V _{IL}	V _S = V _{CC} - GN (see Fig. 7	ND
±IS	analog switch ON-state current			0.1		1.0		1.0	μΑ	5.5	V _{IH} or V _{IL}	V _S I = V _{CC} - GN (see Fig. 8	ND
¹ cc	quiescent supply current	q-q)a	V	2.0		20.0	-qy	40.0	μА	4.5 to 5.5	V _{CC} or GND	V _{is} = GNE V _{CC} ; V _{os} V _{CC} or GI	=
ΔICC	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)	0	100	360		450	80	490	μА	4.5 to 5.5	V _{CC} -2.1 V	other inpu at VCC or GND	

Note

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
 To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT			
	1.00			

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	TEST CONDIT				T _{amb} (°C)					TEST CONDITIONS
93	HTO W. OOV T	MU			74HC	т				V 8	OTUED TORM
SYMBOL	PARAMETER	1251	+25	- 88	-40 1	o +85	-40 to	+125	UNIT	V _{CC}	OTHER
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} /	propagation delay V _{is} to V _{os}	v	6	12	0	15	8.	18	ns sest	4.5	R _L = ∞; C _L = 50 pF (see Fig. 16)
^t PZH	turn "ON" time E _n to V _{os}	y ac	19	35	0	44	0 5	53	ns	4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Figs 17 and 18)
^t PZL	turn "ON" time E _n to V _{os}		20	35		44		53	ns	4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 17 and 18)
t _{PHZ} / t _{PLZ}	turn "OFF" time En to Vos	Ац 0,1	23	35	I	44	0	53	ns	4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 17 and 18)

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

 $GND = 0 V; t_r = t_f = 6 ns$

SYMBOL	PARAMETER	typ.	UNIT	V _{CC}	V _{is(p-p)} V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.80 0.40	% %	4.5 9.0	4.0 8.0	$R_L = 10 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig. 14)
	sine-wave distortion f = 10 kHz	2.40 1.20	% %	4.5 9.0	4.0 8.0	$R_L = 10 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	4.5 9.0	note 1	$R_L = 600 \Omega$; $C_L = 50 pF$; f = 1 MHz (see Figs 10 and 15)
	crosstalk between any two switches	-60 -60	dB dB	4.5 9.0	note 1	$R_L = 600 \Omega$; $C_L = 50 pF$; f = 1 MHz (see Fig. 12)
V _(p-p)	crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 220	mV mV	4.5 9.0		$R_L = 600 \Omega$; $C_L = 50 pF$; $f = 1 MHz (E_n, square wave between V_{CC} and GND,t_r = t_f = 6 ns) (see Fig. 13)$
f _{max}	minimum frequency response (–3dB)	150 160	MHz MHz	4.5 9.0	note 2	$R_L = 50 \Omega$; $C_L = 10 pF$ (see Figs 11 and 14)
CS	maximum switch capacitance	5	pF			

Notes to AC characteristics

General note

 V_{is} is the input voltage at a Y_n or Z_n terminal, whichever is assigned as an input. V_{os} is the output voltage at a Y_n or Z_n terminal, whichever is assigned as an output.

- 1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω). 2. Adjust input voltage V_{is} to 0 dBm level at V_{OS} for 1 MHz $\,$ (0 dBm = 1 mW into 50 Ω).

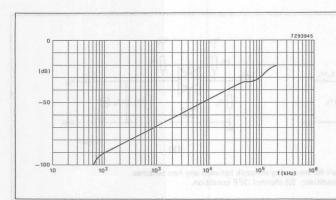
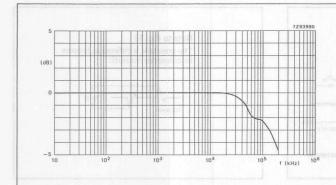
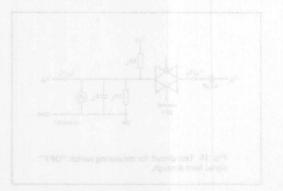


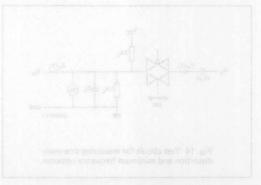
Fig. 10 Typical switch "OFF" signal feed-through as a function of frequency.

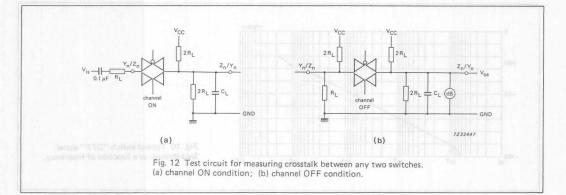


Note to Figs 10 and 11 Test conditions: $V_{CC} = 4.5 \text{ V; GND} = 0 \text{ V;} \\ R_L = 50 \Omega; R_{source} = 1 \text{ k}\Omega.$

Fig. 11 Typical frequency response.







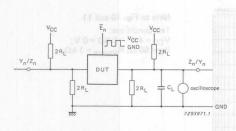
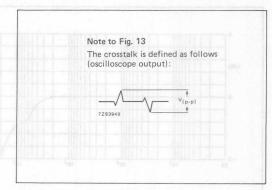


Fig. 13 Test circuit for measuring crosstalk between control and any switch.



$$V_{is} \xrightarrow{Y_n/Z_n} V_{is} \xrightarrow{V_n/Z_n} V_{os}$$

$$V_{is} \xrightarrow{10 \, \mu \text{F}} V_{n}/Z_{n} V_{os}$$

$$V_{is} \xrightarrow{I_{o}} V_{os}$$

Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

AC WAVEFORMS

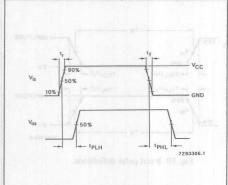
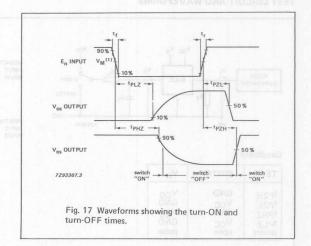


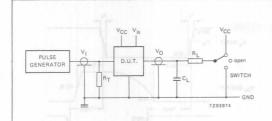
Fig. 16 Waveforms showing the input (V_{is}) to output (Vos) propagation delays.



Note to AC waveforms (1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} .

HCT: V_M = 1.3 V; V_I = GND to 3 V. Data 201

TEST CIRCUIT AND WAVEFORMS



Conditions

TEST	SWITCH	Vis
tPZH	GND	VCC
tPZL	VCC	GND
tPHZ	GND	VCC
tPLZ	VCC	GND
others	open	pulse

NEGATIVE 90% VM AMPLITUDE INPUT PULSE 10% VM TTHL(t_f) THL(t_f) AMPLITUDE OV AMPLITUDE INPUT PULSE 10% VM OV 7287476.3

Fig. 19 Input pulse definitions.

Fig. 18 Test circuit for measuring AC performance.

Definitions for Figs 18 and 19:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

pulse generator. $t_r = t_f = 6 \text{ ns; when measuring } f_{max}$, there is no constraint on t_r , t_f with 50% duty factor.

			t _r ; t _f		
FAMILY	AMPLITUDE	VM	f _{max} ; PULSE WIDTH	OTHER	
74HC	Vcc	50%	< 2 ns	6 ns	
74HCT	3.0 V	1.3 V	< 2 ns	6 ns	

JOHNSON DECADE COUNTER WITH 10 DECODED OUTPUTS

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4017 are high-speed Si-gate CMOS devices and are pin compatible with the "4017" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4017 are 5-stage Johnson decade counters with 10 decoded active HIGH outputs (Ω_0 to Ω_9), an active LOW output from the most significant flip-flop ($\overline{\Omega}_{5-9}$), active HIGH and active LOW clock inputs (CP $_0$ and \overline{CP}_1) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP_0 while \overline{CP}_1 is LOW or a HIGH-to-LOW transition at \overline{CP}_1 while CP_0 is HIGH (see also function table).

When cascading counters, the $\overline{\Omega}_{5.9}$ output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP₀ input of the next counter.

A HIGH on MR resets the counter to zero $(\Omega_0 = \overline{\Omega}_{5-9} = \text{HIGH}; \Omega_1 \text{ to } \Omega_9 = \text{LOW})$ independent of the clock inputs (CP₀ and $\overline{\Omega}_{7-1}^{\text{P}}$)

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

0)/44001	DADAMETED	CONDITIONS	TYF	UNIT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
t _{PHL} / propagation delay t _{PLH} CP ₀ , CP ₁ to Q _n		C _L = 15 pF	20	21	ns
f _{max}	maximum clock frequency	- V _{CC} = 5 V	77	67	MHz
CI	input capacitance	6.6.6.6	3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	35	36	pF

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

- f; = input frequency in MHz f_O = output frequency in MHz
- CL = output load capacitance in pF
- VCC = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is VI = GND to VCC
- For HCT the condition is VI = GND to VCC 1.5 V

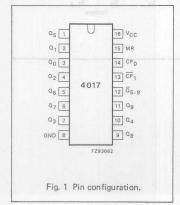
PACKAGE OUTLINES

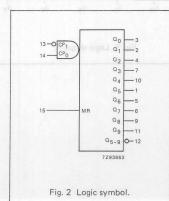
16-lead DIL; plastic (SOT38Z).

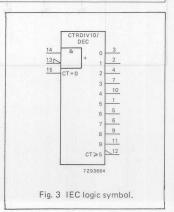
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

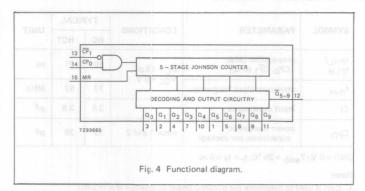
PIN NO.	SYMBOL	NAME AND FUNCTION						
3, 2, 4, 7, 10, 1, 5, 6, 9, 11	Q ₀ to Q ₉	decoded outputs						
8	GND	ground (0 V)						
12	Q ₅₋₉	carry output (active LOW)						
13	CP ₁	clock input (HIGH-to-LOW, edge-triggered)						
14	CP ₀	clock input (LOW-to-HIGH, edge-triggered)						
15	MR	master reset input (active HIGH)						
16	Vcc	positive supply voltage						







JOHNSON DECADE COUNTER WITH 10 DECODED OUTPUTS



FUNCTION TABLE 339UTA33

MR	CP ₀	CP ₁	OPERATION
Н	X	X	$Q_0 = Q_{5-9} = H;$ $Q_1 \text{ to } Q_9 = L$
L	H	1	counter advances
L	of control	Long	counter advances
L	Ligg	X	no change
L	X	Hope	no change
L	His	atoms v	no change
Lyn	ntasbr	sL030	no change

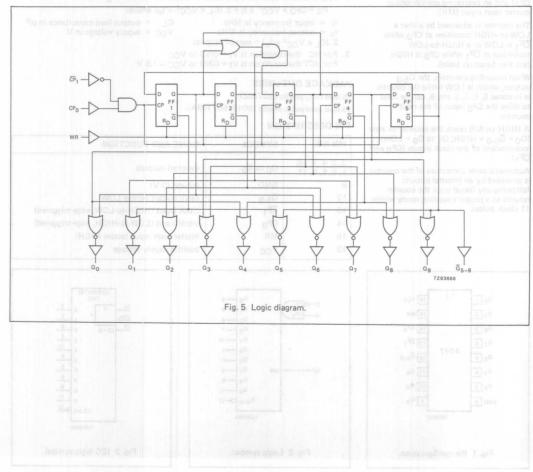
H = HIGH voltage level

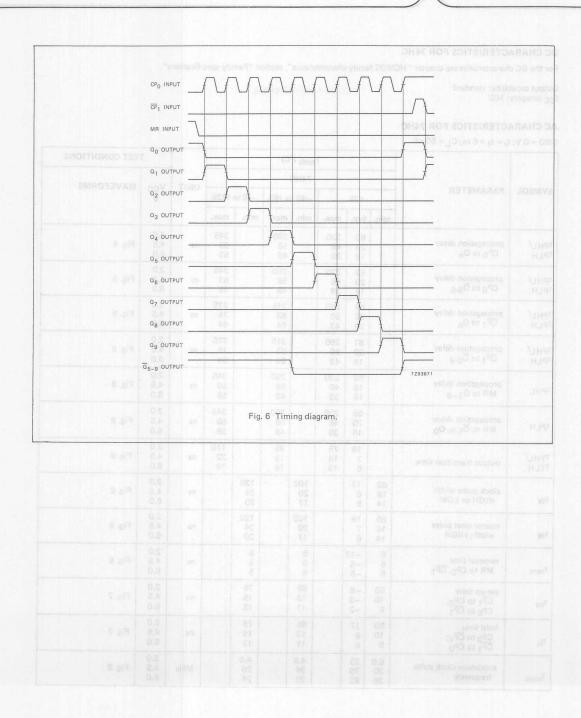
L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH clock transition

↓ = HIGH-to-LOW clock transition





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

					r _{amb} (°C)					TEST CONDITIONS
01/4501	DADAMETED.	74HC				_/	UNIT	W	WAVEFORMS		
SYMBOL	PARAMETER		+25		-40 to +85 -		-40 to +125		UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.	TUS	uo ga	
t _{PHL} /	propagation delay CP ₀ to Q _n		63 23 18	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 9
t _{PHL} /	propagation delay CP ₀ to $\overline{\Omega}_{5.9}$		63 23 18	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 9
t _{PHL} /	propagation delay CP ₁ to Ω _n		61 22 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 9
t _{PHL} /	propagation delay CP ₁ to $\overline{\Omega}_{5-9}$		61 22 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 9
^t PHL	propagation delay MR to Q ₁ _9		52 19 15	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 8
^t PLH	propagation delay MR to $\overline{\Omega}_{5.9}$, Ω_{0}		55 20 16	230 46 39	sib gai	290 58 49	613	345 69 59	ns	2.0 4.5 6.0	Fig. 8
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 9
tw	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
tw	master reset pulse width; HIGH	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
^t rem	removal time MR to CP ₀ , CP ₁	5 5 5	-17 -6 -5		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
t _{su}	set-up time CP ₁ to CP ₀ ; CP ₀ to CP ₁	50 10 9	-8 -3 -2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7
^t h	hold time CP ₀ to CP ₁ ; CP ₁ to CP ₀	50 10 9	17 6 5		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7
f _{max}	maximum clock pulse frequency	6.0 30 25	23 70 83		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
CP ₁	0.40
CPO	0.25
MR	0.50

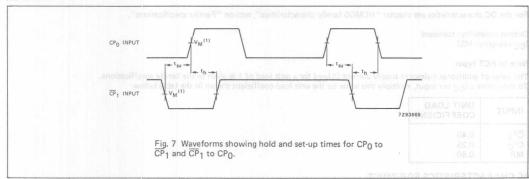
AC CHARACTERISTICS FOR 74HCT

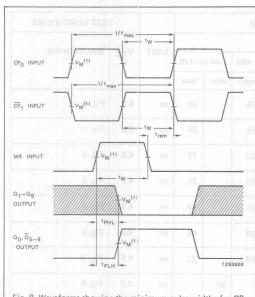
 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_1 = 50 \ pF$

		W.			r _{amb} (°C)					TEST CONDITIONS
		74HCT							LINUT	1/	WAVEFORMS
SYMBOL	PARAMETER	01,00	+25	TURNI OS	-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		-4.	113
tPHL/	propagation delay CP ₀ to Q _n	III _W V	25	46		58		69	ns	4.5	Fig. 9
t _{PHL} /	propagation delay CP ₀ to $\overline{\Omega}_{5-9}$		25	46		58		69	ns	4.5	Fig. 9
t _{PHL} /	propagation delay CP ₁ to Q _n		25	50		63		75	ns	4.5	Fig. 9
t _{PHL} /	propagation delay CP ₁ to Q ₅₋₉		25	50		63		75	ns	4.5	Fig. 9
^t PHL	propagation delay MR to Q ₁ _9		22	46		58		69	ns	4.5	Fig. 8
tPLH	propagation delay MR to $\overline{\Omega}_{5-9}$, Ω_0		20	46		58		69	ns	4.5	Fig. 8
t _{THL} / t _{TLH}	output transition time		7	15		19	19t	22	ns	4.5	Fig. 9
tw	clock pulse width HIGH or LOW	16	7	D -10	20	0.00	24	Name and	ns	4.5	Fig. 8
tw	master reset pulse width; HIGH	16	4	or [4]	20		24	ons Rivi	ns	4.5	Fig. 8
^t rem	removal time MR to CP ₀ , CP ₁	5	-5		5		5		ns	4.5	Fig. 8
t _{su}	set-up time CP ₁ to CP ₀ ; CP ₀ to CP ₁	10	-3	A or er	13		15	DIH-or	ns	4.5	Fig. 7
th	hold time CP ₀ to CP ₁ ; CP ₁ to CP ₀	10	6		13		15	pered on	ns	4.5	Fig. 7
f _{max}	maximum clock pulse frequency	30	61		24		20		MHz	4.5	Fig. 8

AC WAVEFORMS







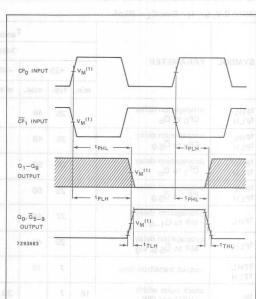


Fig. 8 Waveforms showing the minimum pulse widths for CP0, $\overline{\text{CP}}_1$ and MR inputs; the recovery time for MR and the propagation delays for MR to Q_n and \overline{Q}_5 .9 outputs.

Fig. 9 Waveforms showing the propagation delays for CP0, $\overline{\text{CP}}_1$ to Ω_n , $\overline{\Omega}_{5\text{-}9}$ outputs and the output transition times.

Note to Figs 8 and 9

Conditions:

 \overline{CP}_1 = LOW while CP_0 is triggered on a LOW-to-HIGH transition and CP_0 = HIGH, while \overline{CP}_1 is triggered on a HIGH-to-LOW transition.

Note to AC waveforms

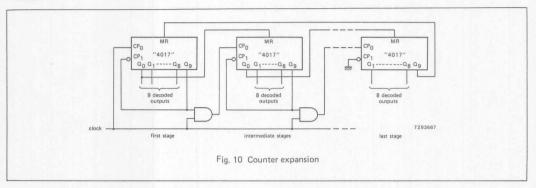
(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

APPLICATION INFORMATION

Some applications for the "4017" are:

- · Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer

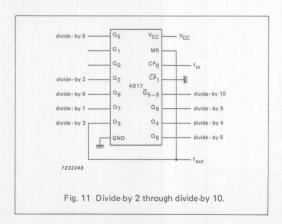
Figure 10 shows a technique for extending the number of decoded output states for the "4017". Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).



Note to Fig. 10

It is essential not to enable the counter on \overline{CP}_1 when CP_0 is HIGH, or on CP_0 when \overline{CP}_1 is LOW, as this would cause an extra count.

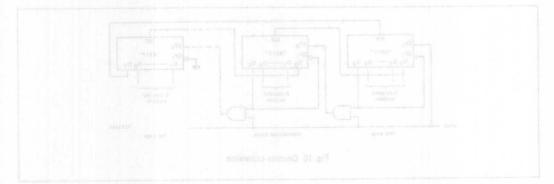
Figure 11 shows an example of a divide-by 2 through divide-by 10 circuit using one "4017". Since "4017" has an asynchronous reset, the output pulse widths are narrow (minimum expected pulse width is 6 ns). The output pulse widths can be enlarged by inserting a RC network at the MR input.



APPLICATION INFORMATION

Some applications for the PATCLY age.

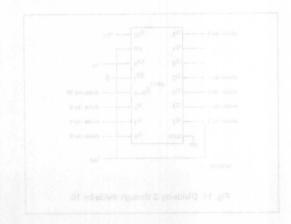
- Decede counter with decimal deceding
- Thebuses owing settems outposes a to too I &
 - Sequential controlle
 - Time



Note to Fig. 1

It is essential not to enable the counter on CP₁ when CP₀ is LOW as this would exuse an extractions.

Figure 11 shows an example of a divide by 2 through divide by 10 circuit using one "A017", Since "A017" has an asynchronous raws, the comput pulse widths are general immiliation expected pulse width is 8 ms). The output pulse width does be enlarged by inserting a RC network at the MB input.



14-STAGE BINARY RIPPLE COUNTER

FEATURES

- Output capability: standard
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4020 are high-speed Si-gate CMOS devices and are pin compatible with the "4020" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4020 are 14-stage binary ripple counters with a clock input ($\overline{\text{CP}}$), an overriding asynchronous master reset input (MR) and twelve fully buffered parallel outputs (Ω_0 , Ω_3 to Ω_{13}).

The counter is advanced on the HIGH-to-LOW transition of $\overline{\text{CP}}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of \overline{CP} .

Each counter stage is a static toggle flip-flop.

OVANDOL	DADAMETED	CONDITIONS	TYF	LIBILT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
t _{PHL} /	propagation delay CP to Q0 Qn to Qn+1 MR to Qn	C _L = 15 pF	11 6 17	15 6 19	ns ns ns
f _{max}	maximum clock frequency	1 1 1 2 1	101	52	MHz
CI	input capacitance sits is not	Fig. 4 Fund	3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	19	20	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

- 1. CPD is used to determine the dynamic power dissipation (PD in μ W):
 - PD = CPD × VCC^2 × f_i + Σ (CL × VCC^2 × f_o) where:
 - fi = input frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V
- f_0 = output frequency in MHz VCC = supply voltage Σ (C_L x V_{CC}² x f_0) = sum of outputs
- 2. For HC the condition is V_I = GND to V_{CC}

 For HCT the condition is V_I = GND to V_{CC} 1.5 V

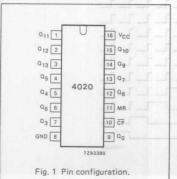
PACKAGE OUTLINES

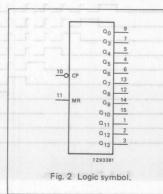
16-lead DIL; plastic (SOT38Z).

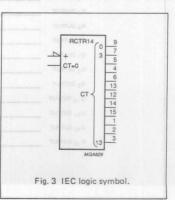
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

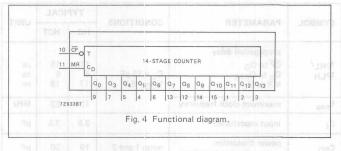
PIN NO.	SYMBOL	NAME AND FUNCTION
9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	Q ₀ , Q ₃ to Q ₁₃	parallel outputs
8	GND	ground (0 V)
10	CP	clock input (HIGH-to-LOW, edge-triggered)
11,	MR	master reset input (active HIGH)
16	Vcc	positive supply voltage

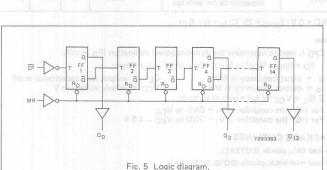






14-STAGE BRIVARY RIPPLE COUNTER





FUNCTION TABLE

INF	PUTS	OUTPUTS
CP	MR	Q ₀ , Q ₃ to Q ₁₃
† bee	ge de m	no change count
X	to Husea	art ritiw skitean

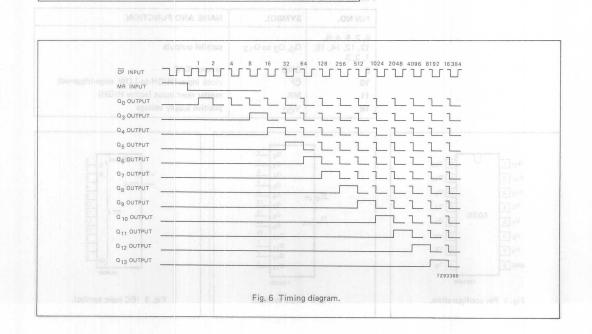
H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH clock transition

↓ = HIGH-to-LOW clock transition



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", see continuous and College to College t

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pf}$

		T _{amb} (°C)								TEST CONDITIONS		
OVER DOL		74HC							UNIT	LOAD	WAVEFORMS TURN	
SYMBOL	PARAMETER		+25		-40	-40 to +85		-40 to +125		V _{CC}	as o	15
		min.	typ.	max.	min.	max.	min.	max.			01.1	
t _{PHL} /	propagation delay CP to Q ₀		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7	
t _{PHL} /	propagation delay Q _n to Q _{n+1}		22 8 6	75 15 13	(°C) TOH	95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7	
[†] PHL	propagation delay MR to Q _n	125 max.	55 20 16	170 34 29	of Old	215 43 37	+25 yp. n	225 51 43	ns	2.0 4.5 6.0	Fig. 8	JOBWY
t _{THL} /	output transition time	1 50	19 7 6	75 15 13	14	95 19 16	E 3	110 22 19	ns	2.0 4.5 6.0	Fig. 7	PLH PLH
tW	clock pulse width HIGH or LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	HT4 ATH
tW	master reset pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns _{Bri}	2.0 4.5 6.0	Fig. 8	J.HT-
^t rem	removal time MR to CP	50 10 9	6 2 2	3	65 13 11	Ġ .	75 15 13	os	ns	2.0 4.5 6.0	Fig. 8	w
f _{max}	maximum clock pulse frequency	6.0 30 35	30 92 109		4.8 24 28		4.0 20 24	0.8	MHz	2.0 4.5 6.0	Fig. 7	W

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications",

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
CP	0.85
MR	1.10

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

SYMBOL	PARAMETER 0.5	T _{amb} (°C)						TEST CONDITIONS			
		974HCT 81 8					10	PLH Unio Qu			
		899 +25 B		-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
	ns 4.5 Fig. 8 6.0	min.	typ.	max.	min.	max.	min.	max.			Dos AM
t _{PHL} / t _{PLH}	propagation delay <u>CP</u> to Ω ₀	110	18	36	0	45	19 7	54	ns	4.5	Fig. 7
t _{PHL} /	propagation delay Q _n to Q _{n+1}		8	15	90	19	T1	22	ns	4.5	Fig. 7
tPHL	propagation delay MR to Q _n		22	45		56	8	68	ns	4.5	Fig. 8
t _{THL} / t _{TLH}	output transition time		7	15	00	19	1000	22	ns dtbi	4.5	Fig. 7
t _W	clock pulse width HIGH or LOW	20	7		25	34	30	50 10	ns	4.5	Fig. 7 _{orner}
t _W	master reset pulse width HIGH	20	8		25		30	0,a	ns	4.5	Fig. 8
t _{rem}	removal time 0.8 MR to CP	10	2		13		15	35	ns	4.5	Fig. 8
f _{max}	maximum clock pulse frequency	25	47		20		17		MHz	4.5	Fig. 7

AC WAVEFORMS

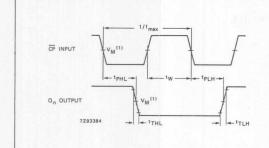


Fig. 7 Waveforms showing the clock (\overline{CP}) to output (O_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

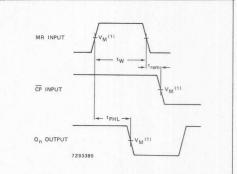


Fig. 8 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (\overline{CP}) removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

AC WAVEFORMS

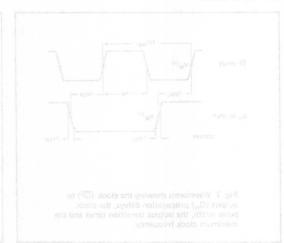




Fig. 8 Waveforms showing the master reset (MR) pulse width, the master reset to output $(O_{\rm pl})$ propagation delays and the master reset to clock (CP) removal time.

Note to AC waveforms

(1) HC: $V_M = 50\%$; $V_1 = 6MD$ to V_{CC} . HCT: $V_M = 1.3 V$; $V_1 = 6MD$ to 3 V.

7-STAGE BINARY RIPPLE COUNTER

FEATURES

- Output capability: standard
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4024 are high-speed Si-gate CMOS devices and are pin compatible with the "4024" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4024 are 7-stage binary ripple counters with a clock input (\overline{CP}) , an overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs $(Q_0$ to Q_6).

The counter advances on the HIGH-to-LOW transition of $\overline{\text{CP}}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of \overline{CP} .

Each counter stage is a static toggle flip-flop.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

APPLICATIONS

- · Frequency dividing circuits
- · Time delay circuits

230/41/0		001101710110	TYF	PICAL	LIBILT
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
t _{PHL} /	propagation delay <u>CP</u> to Ω ₀	C _L = 15 pF V _{CC} = 5 V	14	14	ns
f _{max}	maximum clock frequency	_ vCC = 2 v	90	70	MHz
CL speriov	input capacitance		3.5	3.5	pF
C _{PD} power dissipation capacitance per package		notes 1 and 2	25	27	pF

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

fi = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

fo = output frequency in MHz VCC =

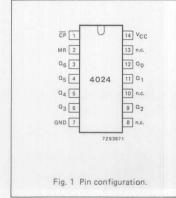
 Σ (C_L x V_{CC}² x f₀) = sum of outputs 2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} - 1.5 V

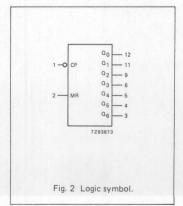
PACKAGE OUTLINES

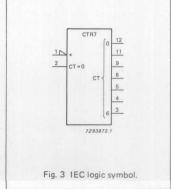
14-lead DIL; plastic (SOT27). 14-lead mini-pack; plastic (SO14; SOT108A).

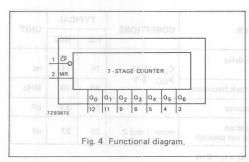
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1 mergeib	CP CP	clock input (HIGH-to-LOW, edge-triggered)
2	MR	master reset input (active HIGH)
12, 11, 9, 6, 5, 4, 3	Q ₀ to Q ₆	parallel outputs
7	GND	ground (0 V)
8, 10, 13	n.c.	not connected
14	Vcc	positive supply voltage









INP	UTS	OUTPUTS		
CP	MR	Qn		
1	LH.Jat	no change		
X ↓	L Hosen	count		

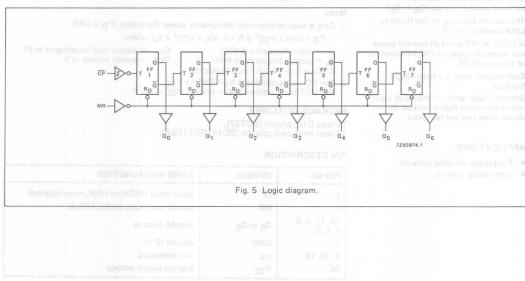
H = HIGH voltage level

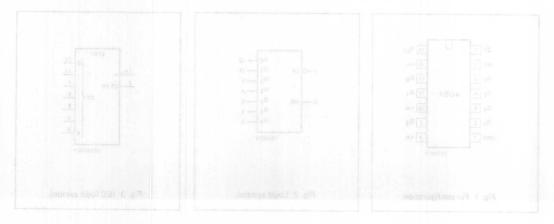
L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH clock transition

↓ = HIGH-to-LOW clock transition





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section. "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

					T _{amb} (°C)					TEST CONDITIONS	
SYMBOL	PARAMETER		74HC								MANEGORMS	
STWBUL		+25			-40	to +85	-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
^t PHL [/] ^t PLH	p <u>rop</u> agation delay <u>CP</u> to Q ₀		47 17 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6	
^t PHL	propagation delay MR to Ω ₀	ALL I	63 23 18	200 40 34	TO	250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6	
^t PHL [/] ^t PLH	propagation delay Ω_n to Ω_{n+1}	35	25 9 7	80 16 14	99 ET (100 20 17	am a	120 24 20	ns	2.0 4.5 6.0	Fig. 6	
t _{THL} /	output transition time	2/1	19 7 6	75 15 13	胁	95 19 16	35	110 22 19	ns	2.0 4.5 6.0	Fig. 6	
t _W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20	8	ns	2.0 4.5 6.0	Fig. 6	
tw	master reset pulse width HIGH	80 16 14	22 8 6		100 20 17		120 24 20	Υ	ns	2.0 4.5 6.0	Fig. 6	
^t rem	removal time MR to CP	50 10 9	6 2 2	24	65 13 11	20	75 15 13	8 8	ns	2.0 4.5 6.0	Fig. 6	
f _{max}	maximum clock pulse frequency	6.0 30 35	27 82 98	31	4.8 24 28	205	4.0 20 24	0 0	MHz	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

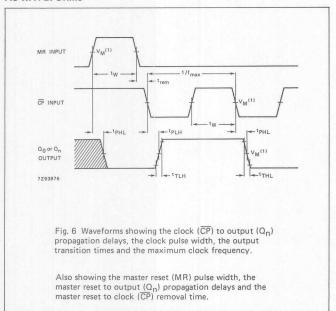
INPUT	UNIT LOAD COEFFICIENT
CP	0.75
MR	0.85

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	2.0	0			T _{amb} (°C)					TEST CONDITION	IS
CVMPOL	s 4.5 Fig. 6		51		74HC	Т	46	23	UNIT	Van	WAVEFORMS	JH
SYMBOL	PARAMETER	10	+25		-40	to +85	-40 t	o +125	UNIT	VCC	n noiteusuoro	
	4.5 Eig. 8 6.0	min.	typ.	max.	min.	max.	min.	max.		100	On to Quet	FLIS
t _{PHL} /	propagation delay CP to Ω0	0	17	35	98	44	75	53	ns	4.5	Fig. 6	JH
[†] PHL	propagation delay MR to Q ₀		21	40	UI I	50		60	ns	4.5	Fig. 6	
t _{PHL} /	propagation delay Q _n to Q _{n+1}		9	16		20		24	ns	4.5	Fig. 6	V
t _{THL} / t _{TLH}	output transition time	2	7	15		19		22	ns	4.5	Fig. 6	Ų
t _W	clock pulse width HIGH or LOW	16	9	75	20	65	24	8 8	ns	4.5	Fig. 6	.000
t _W	master reset pulse wiclth HIGH	16	6	4.0	20	4.8	24	0 27	ns	4.5	Fig. 6	
t _{rem}	removal time MR to CP	10	0	20	13	24 28	15	88 88	ns	4.5	Fig. 6	0000
f _{max}	maximum clock pulse frequency	30	64		24		20		MHz	4.5	Fig. 6	

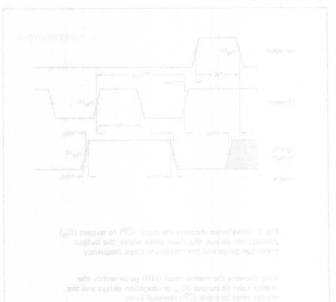
AC WAVEFORMS



Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

AC VAVEFORINS



Note to AC valuationss (1) HC : V_M = 50%; V_I = GND to V_{GC}

12-STAGE BINARY RIPPLE COUNTER

FEATURES

- Output capability: standard
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4040 are high-speed Si-gate CMOS devices and are pin compatible with the "4040" of the "4000" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4040 are 12-stage binary ripple counters with a clock input ($\overline{\text{CP}}$), an overriding asynchronous master reset input (MR) and twelve parallel outputs (Ω_0 to Ω_1 1).

The counter advances on the HIGH-to-LOW transition of $\overline{\text{CP}}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{\text{CP}}.$

Each counter stage is a static toggle flip-flop.

APPLICATIONS

- Frequency dividing circuits
- Time delay circuits
- Control counters

			TYF	UNIT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
^t PHL [/] ^t PLH	$\begin{array}{c} \text{propagation delay} \\ \hline \text{CP to } \Omega_0 \\ \Omega_n \text{ to } \Omega_{n+1} \end{array}$	C _L = 15 pF V _{CC} = 5 V	14	16 8	ns ns
f _{max}	maximum clock frequency	G; 02 02 04 0	90	79	MHz
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	20	20	pF

$$GND = 0 \text{ V}; T_{amb} = 25 \, ^{\circ}\text{C}; t_r = t_f = 6 \text{ ns}$$

Note:

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD × VCC^2 × f_i + Σ (CL × VCC^2 × f_o) where:

f; = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

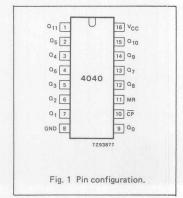
PACKAGE OUTLINES

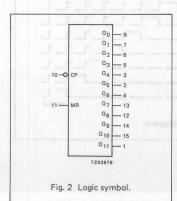
16-lead DIL; plastic (SOT38Z).

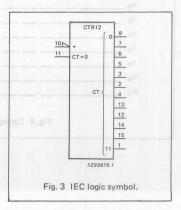
16-lead mini-pack; plastic (SO16; SOT109A).

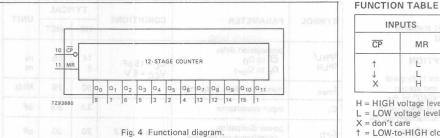
PIN DESCRIPTION

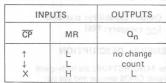
PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	Q ₀ to Q ₁₁	parallel outputs
10	CP CP	clock input (HIGH-to-LOW, edge-triggered
11	MR	master reset input (active HIGH)
16	Vcc	positive supply voltage











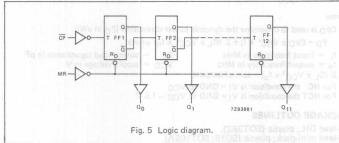
H = HIGH voltage level

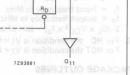
L = LOW voltage level

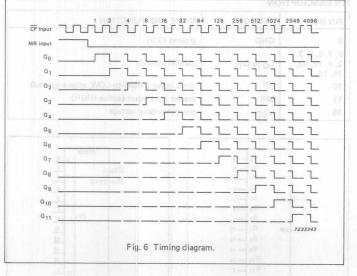
X = don't care

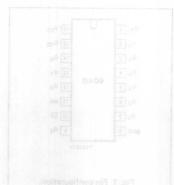
↑ = LOW-to-HIGH clock transition

↓ = HIGH-to-LOW clock transition









DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", see a supply specifications and supply specifications of the DC characteristics are characteristics.

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC met sett number of the beat time a not tool All memory request receiving functions to subsect the

GND = 0 V; tr = tf = 6 ns; C1 = 50 pF latter air nu recommend seed from air videolav aid; yigitlem, sugni see colle

					T _{amb} (°C)				70	TEST CONDIT	IONS
					74H	2						
SYMBOL	PARAMETER	ĮN.	+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORM	S
		min.	typ.	max.	min.	max.	min.	max.	TOM.	500	POLITZISIZTO	
t _{PHL} /	propagation delay		47 17 14	150 30 26	(3°)	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	.V 0 = 0!
t _{PHL} /	propagation delay Q _n to Q _{n+1}		28 10 8	100 20 17	19.1	125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 7	JOSIAY
^t PHL	propagation delay MR to Q _n	-XS	61 22 18	185 37 31	0899 ,1	230 46 39	6 (2)	280 56 48	ns	2.0 4.5 6.0	Fig. 7	
t _{THL} /	output transition time		19 7 6	75 15 13	50	95 19 16	40	110 22 19	ns	2.0 4.5 6.0	Fig. 7	HT2 TH2
tw	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20	22	ns	2.0 4.5 6.0	Fig. 7	HJ!
tw	master reset pulse width; HIGH	80 16 14	22 8 6		100 20 17		120 24 20	7	ns	2.0 4.5 6.0	Fig. 7	HTI JAHJ
^t rem	removal time MR to CP	50 10 9	8 3 2	24	65 13 11	20	75 15 13	6 8	ns	2.0 4.5 6.0	Fig. 7	V
f _{max}	maximum clock pulse frequency	6.0 30 35	27 82 98	er	4.8 24 28	81	4.0 20 24	\$ 0	MHz	2.0 4.5 6.0	Fig. 7	лна

THEFT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

DC CHARACTERISTICS FOR 74HCT

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

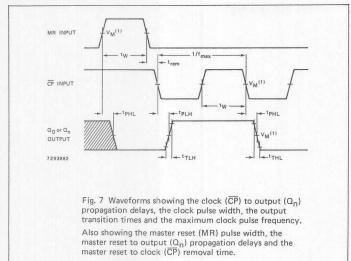
INPUT	UNIT LOAD COEFFICIENT
CP MR	0.85

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

	0.8				T _{amb} (°C)				-	TEST CONDITIONS	S
SYMBOL	PARAMETER		38		74HC	Т	0.0	0.1	UNIT	elay	o noitspagota	
STIVIBUL	PARAMETER 0.8		+25		-40	to +85	-40 t	o +125	UNIT	VCC	WAVEFORMS	
	s 4.5 Fig. 7	min.	typ.	max.	min.	max.	min.	max.		\/sis	α naitegegang ωΩ of RM	JH
t _{PHL} /	propagation delay CP to Q ₀	0	19	40	61	50	75	60	ns	4.5	Fig. 7	
t _{PHL} /	propagation delay Q _n to Q _{n+1}		10	20	81	25	13	30	ns	4.5	Fig. 7	HJ
^t PHL	propagation delay MR to Q _n		23	45		56		68	ns	4.5	Fig. 7	1
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 7	1
t _W	clock pulse width HIGH or LOW	16	7	25	20	80	24	8 0	ns	4.5	Fig. 7	
t _W	master reset pulse width; HIGH	16	6	13	20		24	2 0	ns	4.5	Fig. 7	FITTE
t _{rem}	removal time MR to CP	10	2	24	13	28 28	15	28 d 18 8	ns	4.5	Fig. 7	3687
f _{max}	maximum clock pulse frequency	30	72		24		20		MHz	4.5	Fig. 7	

AC WAVEFORMS



Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

AC WAVEFORMS



Note to AC waveforms
(1) HC : VM = 50%; V) = GND to Vcc.

PHASE-LOCKED-LOOP WITH VCO

FEATURES

- Low power consumption
- · Centre frequency of up to 17 MHz (typ.) at $V_{CC} = 4.5 \text{ V}$
- Choice of three phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop; edge-triggered RS flip-flop
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operating power supply voltage range: VCO section 3.0 to 6.0 V
- digital section 2.0 to 6.0 V Zero voltage offset due to op-amp buffering
- Output capability: standard
- Icc category: MSI

			TYP	DEBG	
SYMBOL	PARAMETER MONTOMA	CONDITIONS	нс	нст	UNIT
fo	VCO centre frequency	C1 = 40 pF R1 = 3 kΩ V _{CC} = 5 V	1909 1909	19	MHz
CI	input capacitance (pin 5)	T VCO	3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	24	24	pF

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

$$PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

fo = output frequency in MHz

f; = input frequency in MHz = Output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. Applies to the phase comparator section only (VCO disabled). For power dissipation of the VCO and demodulator sections see Figs 22, 23 and 24.

PACKAGE OUTLINES

16-lead DIL: plastic (SOT38Z). 16-lead mini-pack; plastic (SO16; SOT109A).

GENERAL DESCRIPTION

The 74HC/HCT4046A are high-speed Si-gate CMOS devices and are pin compatible with the "4046" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

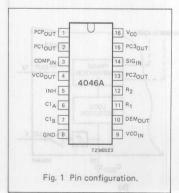
The 74HC/HCT4046A are phase-lockedloop circuits that comprise a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3) with a common signal input amplifier and a common comparator input.

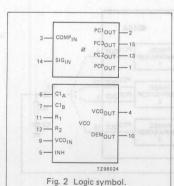
The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "4046A" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

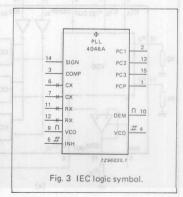
(continued on next page)

APPLICATIONS

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control







PIN DESCRIPTION

PIN NO	ТЭН	SYMBOL	NAME AND FUNCTION	
1 2 3HM 3	81	PCPOUT PC1OUT COMPIN	phase comparator 1 output 000	u ^k
4 Aq		VCO _{OUT}	VCO output and sonstbagge rugni inhibit input	
6 30		C1 _A 2 bm	capacitor C1 connection A	
8		GND VCOIN	ground (0 V) VCO input	
10 11		DEMOUT	demodulator output	
12		R ₁ of Q ⁹) noise R ₂		
13 Rg a		PC2OUT	phase comparator 2 output respect to signal input	
15 16		PC3 _{OUT}	phase comparator 3 output positive supply voltage	

GENERAL DESCRIPTION (Cont'd) VCO

The VCO requires one external capacitor C1 (between C1_A and C1_B) and one external resistor R1 (between R₁ and GND) or two external resistors R1 and R2 (between R₁ and GND, and R₂ and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of

resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{OUT}). In contrast to conventional techniques where the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, here the DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from DEM_{OUT} to GND; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input (COMP_{IN}), or connected via a frequency-divider. The

PHASE-LOCKED-LOOP WITH VCO

VCO output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while

a HIGH level turns both off to minimize standby power consumption.

The only difference between the HC and HCT versions is the input level specification of the INH input. This input disables the VCO section. The sections of the comparator are identical, so that there is no difference in the $\rm SIG_{IN}$ (pin 14) or $\rm COMP_{IN}$ (pin 3) inputs between the HC and HCT versions.

Phase comparators willidays sugtuo

The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

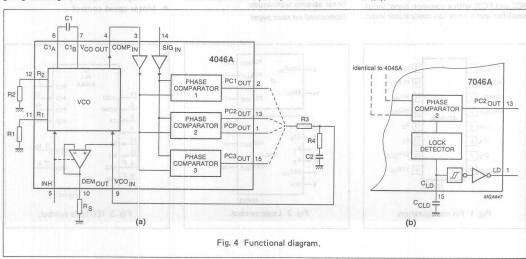
Phase comparator 1 (PC1)

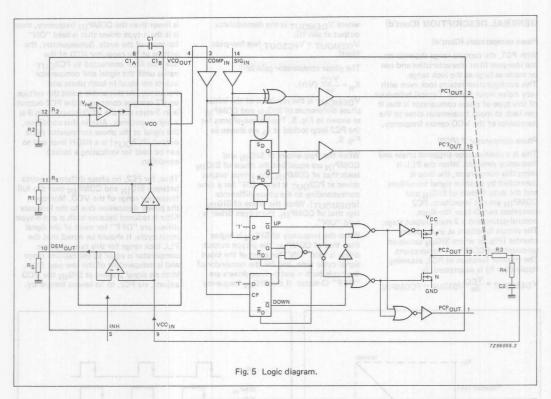
This is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f_1) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_1$) is suppressed, is:

VDEMOUT =
$$\frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;

VDEMOUT = VPC1OUT (via low-pass





The phase comparator gain is: $K_p = \frac{V_{CC}}{\pi} (V/r)$.

$$K_p = \frac{V_{CC}}{\pi} (V/r).$$

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input (COMPIN) as shown in Fig. 6. The average of V_{DEMOUT} is equal to $1/2\ V_{CC}$ when there is no signal or noise at SIGIN and with this input the VCO oscillates at the centre frequency (fo). Typical waveforms for the PC1 loop locked at fo are shown in Fig. 7.

The frequency capture range (2f_c) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range (2f_L) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

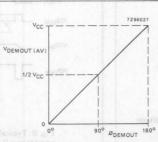


Fig. 6 Phase comparator 1: average output voltage versus input phase difference:

VDEMOUT = VPC10UT =

 $\frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

 ϕ DEMOUT = (ϕ SIGIN - ϕ COMPIN).

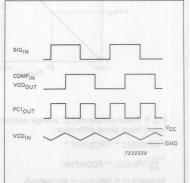


Fig. 7 Typical waveforms for PLL using phase comparator 1, loop locked at fo.

GENERAL DESCRIPTION (Cont'd)

Phase comparators (Cont'd)

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration retains lock even with very noisy input signals. Typical behaviour of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

Phase comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig. 5) where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count. The transfer function of PC2, assuming ripple ($f_{\Gamma} = f_{I}$) is suppressed, is:

 $V_{DEMOUT} = \frac{V_{CC}}{4\pi} (\phi_{SIGIN} - \phi_{COMPIN})$

where V_{DEMOUT} is the demodulator output at pin 10;

V_{DEMOUT} = V_{PC2OUT} (via low-pass filter).

$$K_p = \frac{V_{CC}}{4\pi} (V/r).$$

VDEMOUT is the resultant of the initial phase differences of SIGIN and COMPIN as shown in Fig. 8. Typical waveforms for the PC2 loop locked at fo are shown in Fig. 9.

When the frequencies of SIG $_{IN}$ and COMP $_{IN}$ are equal but the phase of SIG $_{IN}$ leads that of COMP $_{IN}$, the p-type output driver at PC2 $_{OUT}$ is held "ON" for a time corresponding to the phase difference (ϕ DEMOUT). When the phase of SIG $_{IN}$ lags that of COMP $_{IN}$, the n-type driver is held "ON".

When the frequency of SIGIN is higher than that of COMPIN, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n and p-type drivers are "OFF" (3-state). If the SIGIN frequency

is lower than the COMP_{IN} frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to PC2_{OUT} varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level and so can be used for indicating a locked condition.

Thus, for PC2, no phase difference exists between SIG_{IN} and COMP_{IN} over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_{IN} the VCO adjusts, via PC2, to its lowest frequency.

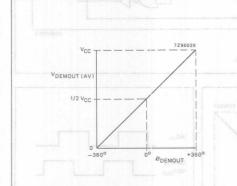


Fig. 8 Phase comparator 2: average output voltage versus input phase difference:

VDEMOUT = VPC2OUT =

 $\frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

 ϕ DEMOUT = $(\phi$ SIGIN $- \phi$ COMPIN).

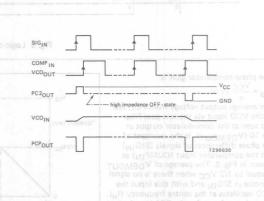


Fig. 9 Typical waveforms for PLL using phase comparator 2, loop locked at fo.

Phase comparator 3 (PC3)

This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIGIN and COMPIN are not important. The transfer characteristic of PC3, assuming ripple $(f_r = f_i)$ is suppressed, is:

 $V_{DEMOUT} = \frac{V_{CC}}{2\pi} (\phi_{SIGIN} - \phi_{COMPIN})$

where VDEMOUT is the demodulator output at pin 10;

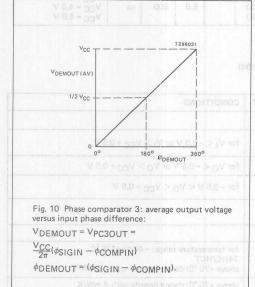
VDEMOUT = VPC3OUT (via low-pass filter). RETOARAND

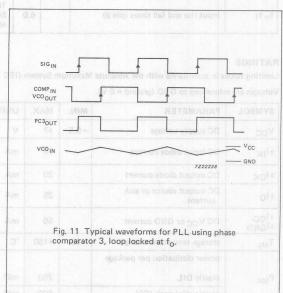
<u>Vcc</u> (V/r). 2π

The average output from PC3, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 (VDEMOUT), is the resultant of the phase differences of SIG_{IN} and COMP_{IN} as shown in Fig. 10. Typical waveforms for the PC3 loop locked at fo are shown in Fig. 11.

The phase-to-output response characteristic of PC3 (Fig. 10) differs from that of PC2 in that the phase angle between SIGIN and COMPIN varies between 0° and 360° and is 180° at the

The phase comparator gain is: god and centre frequency. Also PC3 gives a greater voltage swing than PC2 for input phase differences but as a consequence the ripple content of the VCO input signal is higher. The PLL lock range for this type of phase comparator and the capture range are dependent on the low-pass filter. With no signal present at SIGIN the VCO adjusts, via PC3, to its lowest frequency.





RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER 19 1911 1902		74HC		28	74HC	Lack-ail	UNIT	CONDITIONS TO A COOL AND	
	PARAMETER 10 June 100 Verb	min.	typ.	max.	min.	typ.	max.	positive		
Vcc	DC supply voltage	3.0	5.0	6.0	4.5	5.0	5.5	Varion	transitions and the duty and COMPIN era not into	
VCC	DC supply voltage if VCO section is not used	2.0	5.0	6.0	4.5	5.0	5.5	V	ransfer characteristic or haple $(f_n = f_i)$ is suppres	
VI	DC input voltage range	0	eno dem	Vcc	0	eriT	VCC	V	V DEMOUT = Zir (VSIC	
Vo	DC output voltage range	0	11 1914)	Vcc	0	ciran	Vcc	V	where V DEMOUT is the	
T _{amb}	operating ambient temperature range	- 40	PIVICE	+85	-40	vist	+85	°C	see DC and AC	
T _{amb}	operating ambient temperature range	-40	St Dill	+125	-40	N/ZSCI	+125	°C	CHARACTERISTICS	
t _r , t _f	input rise and fall times (pin 5)		6.0	1000 500 400		6.0	500	ns	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V _{CC}	DC supply voltage	-0.5	+7	V	
±1IK	DC input diode current		20	mA	for $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$
±IOK	DC output diode current		20	mA	for $V_0 < -0.5 \text{ V}$ or $V_0 > V_{CC} + 0.5 \text{ V}$
±10	DC output source or sink current		25	mA	for -0.5 V < V _O < V _{CC} + 0.5 V
±ICC; ±IGND	DC V _{CC} or GND current	er er e	50	mA	Fig. 10 Phase comparator 3: average output voltage versus input phase difference:
T _{stg}	storage temperature range	- 65	+150	°C	VERMOUT " VPCSOUT "
P _{tot}	power dissipation per package plastic DIL		750	mW	for temperature range: – 40 to +125 °C 74HC/HCT above +70 °C: derate linearly with 12 mW/K 10M30°C
	plastic mini-pack (SC)		500	mW	above +70 °C: derate linearly with 8 mW/K

DC CHARACTERISTICS FOR 74HC

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

snot	TEST CONDIT		T _{amb} (°C)								TEST CONDITIONS
OVMDOL	DADAMETED				74H	C			UNIT	V	OTHER
SYMBOL	PARAMETER	25	+25	a- as	-40	to +85	-40 t	o +125	ONT	T V _{CC} OTHER	OTHER JOS
		min.	typ.	max.	min.	max.	min.	max.			
Icc	quiescent supply current (VCO disabled)	V	1	8.0	8	80.0		160.0	μА	6.0	pins 3, 5, and 14 at v pin 9 at GND; I _I at p 3 and 14 to be exclude

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

= 20 µA				4,4	r _{amb} (°C)				8	TEST C	ONDITIONS
= 20 µA				0.0	74H	0					Total	DESILES T
SYMBOL	PARAMETER 8.4		+25	3,7	-40	to +85	-40 to	o +125	UNIT	VCC	VI	OTHER
Au CS	= 01 HIV 0.8	min.	typ.	max.	min.	max.	min.	max.			lay	LOW
V _{IH} Au 00	DC coupled HIGH level input voltage SIGIN, COMPIN	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2	0	V	2.0 4.5 6.0	TUC TUC	TOM I
S.2 mA VIL	DC coupled LOW level input voltage SIG _{IN} , COMP _{IN}	A.	0.8 2.1 2.8	0.5 1.35 1.8	0.3	0.5 1.35 1.8	E.O 18	0.5 1.35 1.8	V	2.0 4.5 6.0	TUK	00V
V _{OH}	HIGH level output voltage PCPOUT, PCnOUT	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V _{IH} or V _{IL}	$-1_0 = 20 \mu A$ $-1_0 = 20 \mu A$ $-1_0 = 20 \mu A$
V _{OH}	HIGH level output voltage PCPOUT, PCnOUT	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2	0	V	4.5 6.0	V _{IH} or V _{IL}	-1 _O = 4.0 mA -1 _O = 5.2 mA
V _{OL}	LOW level output voltage PCPOUT, PCnOUT		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1	300	0.1 0.1 0.1	V	2.0 4.5 6.0	VIH or VIL	I _O = 20 μA I _O = 20 μA I _O = 20 μA
V _{OL}	LOW level output voltage PCPOUT, PCnOUT		0.15 0.16			0.33 0.33	300	0.4 0.4	V	4.5 6.0	VIH or VIL	I _O = 4.0 mA I _O = 5.2 mA
ıl± he range led far B1:	input leakage current SIG _{IN} , COMP _{IN}			3.0 7.0 18.0 30.0		4.0 9.0 23.0 38.0	2.1	5.0 11.0 27.0 45.0	μА	2.0 3.0 4.5 6.0	V _{CC} or GND	landea
±I _{OZ}	3-state OFF-state current PC2 _{OUT}			0.5		5.0	3.4	10.0	μΑ	6.0	V _{IH} or V _{IL}	V _O = V _{CC} or GND
RI	input resistance SIG _{IN} , COMP _{IN}		800 250 150						kΩ	3.0 4.5 6.0	point;	self-bias operating $\Delta V_{\parallel} = 0.5 V_{\uparrow}$ gs 12, 13 and 14

DC CHARACTERISTICS FOR 74HC (Cont'd) VCO section

Voltages are referenced to GND (ground = 0 V)

					T _{amb} (°C)		-			TEST CO	ONDITIONS
		(4)			74H	C				1	NETENA	SYMBOL DAN
SYMBOL	PARAMETER 30	25	+25	3- B	-40	to +85	-40 to	+125	UNIT	VCC	VI	OTHER ONLY &
		min.	typ.	max.	min.	max.	min.	max.				
VIH	HIGH level input voltage INH	2.1 3.15 4.2	1.7 2.4 3.2	. 0	2.1 3.15 4.2		2.1 3.15 4.2		V	3.0 4.5 6.0	que Insc désib O	
VIL	LOW level input voltage INH		1.3 2.1 2.8	0.9 1.35 1.8		0.9 1.35 1.8		0.9 1.35 1.8	V 0 ≈ hous	3.0 4.5 6.0	section	
V _{OH} 2MC	HIGH level output voltage VCOOUT	2.9 4.4 5.9	3.0 4.5 6.0		2.9 4.4 5.9	tmoT	2.9 4.4 5.9		V	3.0 4.5 6.0	V _{IH} or V _{IL}	- I _O = 20 μA - I _O = 20 μA - I _O = 20 μA
V _{OH}	HIGH level output voltage VCOOUT	3.98 5.48	4.32 5.81	b B	3.84 5.34	6	3.7 5.2	+	V	4.5 6.0	V _{IH} or V _{IL}	-I _O = 4.0 mA -I _O = 5.2 mA
V _{OL}	LOW level output voltage VCOOUT	-83	0 0 0	0.1 0.1 0.1	1000	0.1 0.1 0.1	0.0 pm	0.1 0.1 0.1	V	3.0 4.5 6.0	V _{IH} or V _{IL}	I _O = 20 μA I _O = 20 μA I _O = 20 μA
V _{OL}	LOW level output voltage VCOOUT	\$ 8 B	0.15 0.16	0.26 0.26	a.0	0.33 0.33	8,0 8	0.4 0.4	V	4.5 6.0	V _{IH} or V _{IL}	I _O = 4.0 mA I _O = 5.2 mA
VOL	LOW level output voltage C1 _A , C1 _B			0.40 0.40	1,8	0.47 0.47	5,1 8	0.54 0.54	V	4.5 6.0	V _{IH} or V _{IL}	I _O = 4.0 mA I _O = 5.2 mA
Ац 05 ±1 ₁ Ат 0,3	input leakage current INH, VCO _{IN}			0.1		1.0	100	1.0	μА	6.0	V _{CC} or GND	HDIH MADA
R1 Au	resistor range	3.0 3.0 3.0	0	300 300 300	1.0	81,69	1.0	0	kΩ	3.0 4.5 6.0	PH TUO	note 1
R2 Am 0	resistor range	3.0 3.0 3.0	0	300 300 300	2.0		5.0 8	0	kΩ	3.0 4.5 6.0	luo level	note 1
C1	capacitor range	40 40 40	La l	no limit	4.0		3.0		pF	3.0 4.5 6.0	e a uu	andui .
Vvcoin	operating voltage range at VCOIN	1.1 1.1 1.1	27	1.9 3.4 5.9	28.1		.05 .05		V	3.0 4.5 6.0	4, CON	over the range specified for R1; for linearity see Figs 20 and 21.

Note

^{1.} The parallel value of R1 and R2 should be more than 2.7 k Ω . Optimum performance is achieved when R1 and/or R2 are/is > 10 k Ω .

Demodulator section

Voltages are referenced to GND (ground = 0 V)

						T _{amb} (°C)				Hg 08 -	TEST CONDITIONS	SV 0 = QV
	TEST CONDITE					74H	C dres						1111
SYMBOL	PARAMETER		MU	+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	OTHER	
		V.	min.	typ.	max.	min.	max.	min.	max.			PARAMETER	TOBMY
Rs	resistor range		50 50 50	808 308	300 300 300	1mgx. 250	nia:	mas. 200	typ.	kΩ	3.0 4.5 6.0	at R _S > 300 kΩ the leakage current influence V _{DEMO}	
V _{OFF}	offset voltage VCO _{IN} to V _I	DEMOUT	(41) (41)	±30 ±20 ±10		90 42 1425		340	18	mV	3.0 4.5 6.0	V _I = V _V COIN = 1/2 V _O values taken over R _S ra see Fig. 15	
R _D	dynamic outpuresistance at	ıt 0.8	en .	25 25 25		88 72 1340		950	35 28 77	Ω	3.0 4.5 6.0	V _{DEMOUT} = 1/2	VCC
	61 .g.1	4.5 0.8	an	69		88 58		84 46	28		И	SIGIN, COMPL to PC3OUT	HJE

AC CHARACTERISTICS FOR 74HC

Phase comparator section

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	Vec OTHER				T _{amb} (°C)					TEST CONDITIONS
0.410.01	V	THOU	38746	703	74H	C		425		.,	OTHER
SYMBOL	PARAMETER		+25	-nim	-40	to +85	-40 t	o +125	UNIT	V _{CC}	OTHER
	3,0 at Hg > 300 kG	min.	typ.	max.	min.	max.	min.	max.	18.		
t _{PHL} /	propagation delay SIG _{IN} , COMP _{IN} to PC1 _{OUT}	Į.	63 23 18	200 40 34		250 50 43	300	300 60 51	ns	2.0 4.5 6.0	Fig. 16
tPHL/	propagation delay SIG _{IN} , COMP _{IN} to PCP _{OUT}	Ω.	96 35 28	340 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig. 16
t _{PHL} /	propagation delay SIG _{IN} , COMP _{IN} to PC3 _{OUT}		77 28 22	270 54 46		340 68 58		405 81 69	ns	2.0 4.5 6.0	Fig. 16
t _{PZH} /	3-state output enable time SIG _{IN} , COMP _{IN} to PC2 _{OUT}		83 30 24	280 56 48		350 70 60		420 84 71	ns	2.0 4.5 6.0	Fig. 17
t _{PHZ} /	3-state output disable time SIG _{IN} , COMP _{IN} to PC2 _{OUT}		99 36 29	325 65 55		405 81 69		490 98 83	ns	2.0 4.5 6.0	Fig. 17
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 16
V _{I(p-p)}	AC coupled input sensitiv (peak-to-peak value) at SIG _{IN} or COMP _{IN}	rity	9 11 15 33						mV	2.0 3.0 4.5 6.0	f _i = 1 MHz

VCO section

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

					T _{amb} (°C)					TEST CONDITIONS
CVMPOL	DADAMETER				74H	2			LINUT		OTHER
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	0 +125	UNIT	V _{CC}	OTHER
		min.	typ.	max.	typ.	max.	min.	max.			
∆f/T	frequency stability with temperature change				0.20 0.15 0.14				%/K	3.0 4.5 6.0	$V_1 = V_{VCOIN} = 1/2 V_{CC};$ $R1 = 100 \text{ k}\Omega; R2 = \infty;$ C1 = 100 pF; see Fig. 18
fo	VCO centre frequency (duty factor = 50%)	3.0 11.0 13.0							MHz	3.0 4.5 6.0	$V_{VCOIN} = 1/2 V_{CC};$ $R1 = 3 k\Omega; R2 = \infty;$ C1 = 40 pF; see Fig. 19
Δfvco	VCO frequency linearity		1.0 0.4 0.3						%	3.0 4.5 6.0	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 20 and 21
δνςο	duty factor at VCO _{OUT}		50 50 50						%	3.0 4.5 6.0	

DC CHARACTERISTICS FOR 74HCT

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

	TEST CONDIT				T _{amb} (°C)					TEST CONDITIONS
0)/440.01	DADAMETED				74H	CT			LIAUT		OTHER
SYMBOL	PARAMETER	35	+25	s	-40	to +85	-40 t	o +125	UNIT	VCC	OTHER TO HORNY
		min.	typ.	max.	min.	max.	min.	max.			
¹ cc	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μА	6.0	pins 3, 5 and 14 at V _{CC} ; pin 9 at GND; I _I at pins 3 and 14 to be excluded
ΔICC	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) V _I = V _{CC} - 2.1 V		100	360		450		490	μА	4.5 to 5.5	pins 3 and 14 at V _{CC} ; pin 9 at GND; I ₁ at pins 3 and 14 to be excluded

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given above. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

	,	nV	.,			TUONDIA PENDUT	
INPUT		LOAD	IT a				
INH	1.00						
Act D	10 = 4	HIV 10	8,5				

DC CHARACTERISTICS FOR 74HCT

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SMC	TEST CONDITI				T _{amb} (°C)	400 000			1	TEST C	ONDITIONS
	THE TAX NOV THE				74HC	т			UNIT	V	Vi	OTHER OBMY
SYMBOL	PARAMETER 00	25	+25	B- B	-40	to +85	-40 t	o +125	UNIT	V _{CC}	V	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
V _{IH} ⁷⁸ I	DC coupled HIGH level input voltage SIGIN, COMPIN	3.15	2.4		.08		8,8		v ins	4.5	ent supp disebs	(VC)
VILOSVIA	DC coupled LOW level input voltage SIG _{IN} , COMP _{IN}	a Di	2.1	1.35	084		uas t	iar	V tot V tot f at	4.5	up lend in per in load cos	tien 201a Linno Linno
VoH	HIGH level output voltage PCPOUT, PCnOUT	4.4	4.5		4.4		4.4		V	4.5	VIH or VIL	-1 _O = 20 μA
V _{OH}	HIGH level output voltage PCPOUT, PCnOUT	3.98				nu a no Init loa		l) trignic s yalup a	yiqque Vyiqiri	4.5	V _{IH} or V _{IL}	-1 ₀ = 4.0 mA
V _{OL}	LOW level output voltage PCPOUT, PCnOUT		0	0.1		0.1		0.1	V	4.5	V _{IH} or V _{IL}	1 _O = 20 μΑ
V _{OL}	LOW level output voltage PCP _{OUT} , PC _{nOUT}		0.15	0.26		0.33		0.4	٧	4.5	V _{IH} or V _{IL}	I _O = 4.0 mA
±II	input leakage current SIG _{IN} , COMP _{IN}			30		38		45	μА	5.5	V _{CC} or GND	
±IOZ	3-state OFF-state current PC2 _{OUT}			0.5		5.0		10.0	μΑ	5.5	VIH or VIL	V _O = V _{CC} or GND
R _I	input resistance SIG _{IN} , COMP _{IN}		250						kΩ	4.5	point	self-bias operating $\triangle V_1 = 0.5 V$; gs 12, 13 and 14

DC CHARACTERISTICS FOR 74HCT VCO section

Voltages are referenced to GND (ground = 0 V)

	HEST CONDITION					T _{amb} (°C)					TEST C	ONDITION	S
						74H0	CTURY	Y Y						
SYMBOL	PARAMETER			+25	os 63	-40	to +85	-40 to	0 +125	UNIT	V _{CC}	VI	OTHER	
			min.	typ.	max.	min.	max.	min.	max.	raim.				
V _{IH} assistance	HIGH level input voltage INH	4,5	2.0	1.6		2.0		2.0		V	4.5 to 5.5	sga	n vorsiser	
VIE Vect	LOW level input voltage INH	4.6	Vm	1.2	0.8		0.8		0.8	V	4.5 to 5.5		ov recitio UEODV	190
V _{OH}	HIGH level output voltage VCOOUT	4.5	4.4	4.5		4.4		4.4	25	V	4.5	V _{IH} or V _{IL}	-I _O = 20	μΑ
V _{OH}	HIGH level output voltage VCOOUT		3.98	4.32		3.84		3.7		V	4.5	VIH or VIL	-I _O = 4.0	mA
VoL	LOW level output voltage VCOOUT			0	0.1		0.1		0.1	· v	4.5	VIH or VIL	ΙΟ = 20 μ.	A
VOL	LOW level output voltage VCOOUT			0.15	0.26		0.33		0.4	V	4.5	V _{IH} or V _{IL}	I _O = 4.0 n	nA
VOL	LOW level outpu voltage C1 _A , C1 (test purposes o	B			0.40		0.47		0.54	V	4.5	V _{IH} or V _{IL}	I _O = 4.0 n	nA
±II	input leakage cur INH, VCO _{IN}	rent			0.1		1.0		1.0	μА	5.5	V _{CC} or GND		
R1	resistor range		3.0		300					kΩ	4.5		note 1	
R2	resistor range		3.0		300					kΩ	4.5		note 1	
C1	capacitor range		40		no limit					pF	4.5			n# E
Vvcoin	operating voltage range at VCO _{IN}		1.1		3.4					V	4.5		over the ra specified to for lineari Figs 20 an	or R1; ty see

Note

^{1.} The parallel value of R1 and R2 should be more than 2.7 k Ω . Optimum performance is achieved when R1 and/or R2 are/is > 10 k Ω .

DC CHARACTERISTICS FOR 74HCT

Demodulator section

Voltages are referenced to GND (ground = 0 V)

DC CHARACTERISTICS FOR 74HCT

VCO section

Voltages are referenced to GND (ground = 0 V)

	TEST CONDITIONS						r _{amb} ('	,C)	T		TEST CONDITIONS			
SYMBOL						74HC	THAT		LIMIT		OTHER			
	PARAMETER			+25			-40 to +85		-40 to +125		UNIT	V _{CC}	OTHER	TOSMAS
				min.	typ.	max.	min.	max.	min.	max.	ann			
R _S	resistor r	ange	4,5 10 5.5	50		300		2.0		1,6	kΩ	4.5	at R _S > 300 kΩ the leakage curre influence V _{DEM}	nt can HIV
V _{OFF}	offset vo VCO _{IN}		моит	V	±20		8.0		8.0	1.2	mV	4.5	V _I = V _V COIN = values taken over see Fig. 15	1/2 V _{CC} ; R _S range;
R _D	dynamic resistan		MOUT	V	25	4,4		6,6			Ω	4.5	V _{DEMOUT} = 1/3	2 V _{CC}
		-17											LDD 004	

AC CHARACTERISTICS FOR 74HCT

Phase comparator section

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

					T _{amb} (°C)	No.	TEST CONDITIONS				
01/44001	Vectorial III	X	(00)		74H	СТ			OTUED.			
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC	OTHER	
		min.	typ. max.		min. max.		min. max.					
tPHL/	propagation delay SIG _{IN} , COMP _{IN} to PC1 _{OUT}	4	23	40		50		60	ns	4.5	Fig. 16	
t _{PHL} /	propagation delay SIG _{IN} , COMP _{IN} to PCP _{OUT}	80046	35	68		85		102	ns	4.5	Fig. 16	
t _{PHL} / t _{PLH}	propagation delay SIG _{IN} , COMP _{IN} to PC3 _{OUT}	i fegni	28	54		68	un Di	81	ns	4.5	Fig. 16	
t _{PZH} /	3-state output enable time SIG _{IN} , COMP _{IN} to PC2 _{OUT}	sa V d	30	56		70		84	ns	4.5	Fig. 17	
t _{PHZ} /	3-state output disable time SIG _{IN} , COMP _{IN} to PC2 _{OUT}		36	65		81		98	ns	4.5	Fig. 17	
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 16	
V _{I (p-p)}	AC coupled input sensitivity (peak-to-peak value) at SIGIN or COMPIN		15						mV	4.5	f _i = 1 MHz	

VCO section

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

SYMBOL		T _{amb} (°C)								TEST CONDITIONS		
	1 to VSV	- 50V5	9		74H0	т	ANIA SE	1.57	W2 V _{CC} -8.25			
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC	OTHER	
		min.	typ.	max.	typ.	max.	min.	max.				
Δf/T	frequency stability with temperature change	2000 = 2000 25000 25000	Rg -	T.	0.15		riyis	MIAMO	%/K	4.5	$V_I = V_{VCOIN}$ within recommended range; R1 = 100 k Ω ; R2 = ∞ ; C1 = 100 pF; see Fig. 18t	
fo	VCO centre frequency (duty factor = 50%)	11.0	17.0						MHz	4.5	$V_{VCOIN} = 1/2 V_{CC};$ $R1 = 3 k\Omega; R2 = \infty;$ C1 = 40 pF; see Fig. 19	
∆f∨co	VCO frequency linearity		0.4						%	4.5	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 20 and 21	
δνςο	duty factor at VCOOUT		50						%	4.5		

FIGURE REFERENCES FOR DC CHARACTERISTICS

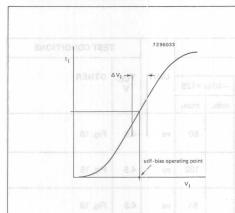


Fig. 12 Typical input resistance curve at SIG_{IN} , $COMP_{IN}$.

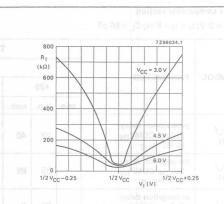


Fig. 13 Input resistance at SIGIN, COMPIN with ΔV_I = 0.5 V at self-bias point.

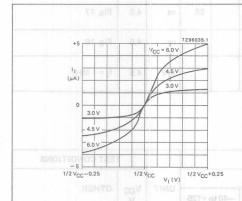
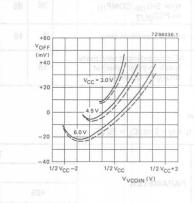


Fig. 14 Input current at SIG_{IN}, COMP_{IN} with $\Delta V_I = 0.5 \text{ V}$ at self-bias point.



 $-R_S = 50 k\Omega$ --- R_S = 300 kΩ

Fig. 15 Offset voltage at demodulator output as a function of VCO $_{\mbox{\scriptsize IN}}$ and $\mbox{\scriptsize R}_{\mbox{\scriptsize S}}.$

AC WAVEFORMS

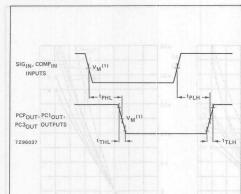
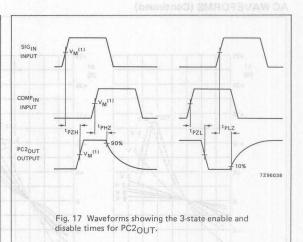


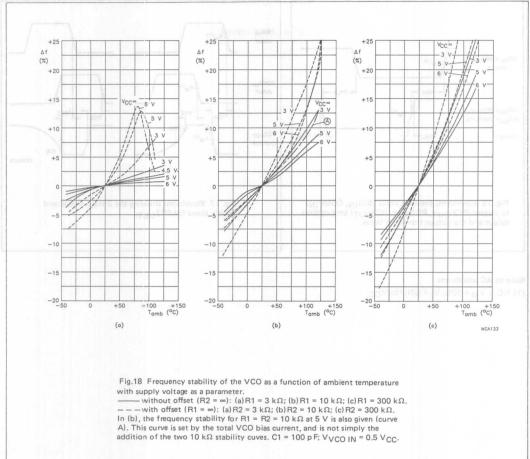
Fig. 16 Waveforms showing input (SIGIN, COMPIN) to output (PCP_{OUT}, PC1_{OUT}, PC3_{OUT}) propagation delays and the output transition times.

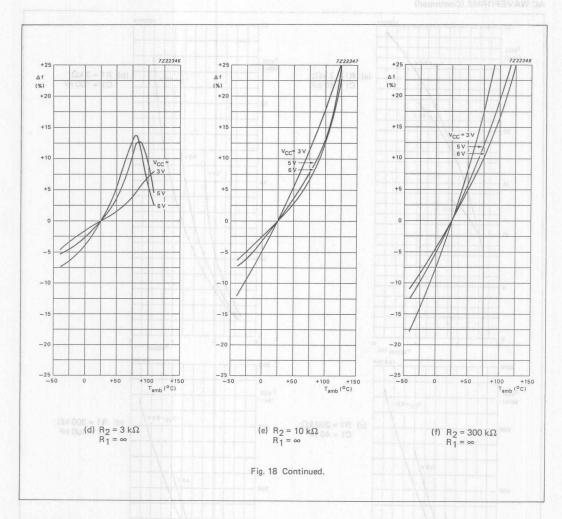


Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} .



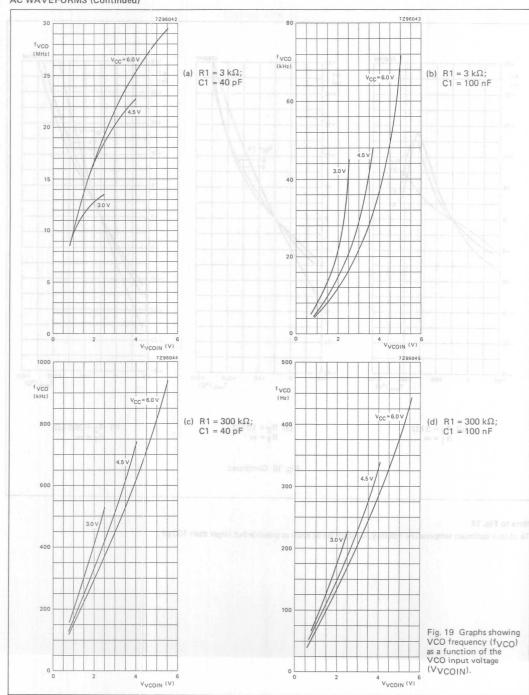




Note to Fig. 18

To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

AC WAVEFORMS (Continued)



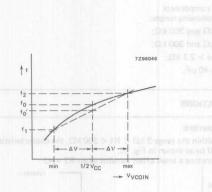


Fig. 20 Definition of VCO frequency linearity: $\Delta V = 0.5 \ V$ over the $V_{\hbox{\scriptsize CC}}$ range:

for VCO linearity

$$f'_0 = \frac{f_1 + f_2}{2}$$

linearity =
$$\frac{f'_0 - f_0}{f'_0} \times 100\%$$

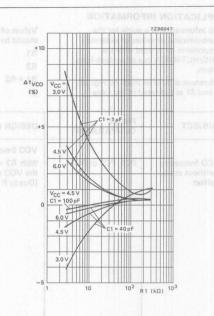
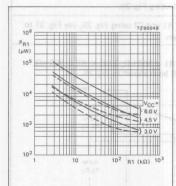
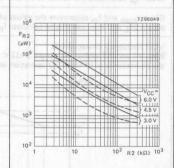


Fig. 21 Frequency linearity as a function of R1, C1 and V_{CC}: R2 = ∞ and Δ V = 0.5 V.



- C1 = 40 pF $\cdot \cdot \cdot C1 = 1 \mu \text{F}$

Fig. 22 Power dissipation versus the value of R1: $C_L = 50$ pF; $R2 = \infty$; VVCOIN = 1/2 V_{CC} ; $T_{amb} = 25$ °C.



--- C1 = 40 pF --- C1 = 1 μF

Fig. 23 Power dissipation versus the value of R2: $C_L = 50$ pF; R1 = ∞ ; $V_{COIN} = GND = 0$ V; $T_{amb} = 25$ °C.

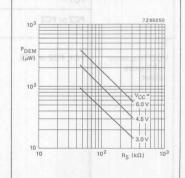


Fig. 24 Typical dc power dissipation of demodulator sections as a function of Rg: R1 = R2 = ∞; T_{amb} = 25 °C; V_{VCOIN} = 1/2 V_{CC}.

APPLICATION INFORMATION

This information is a guide for the approximation of values of external components to be used with the 74HC/HCT4046A in a phase-lock-lcop system.

References should be made to Figs 29, 30 and 31 as indicated in the table.

Values of the selected components should be within the following ranges:

R1 between 3 k Ω and 300 k Ω ;

2 between 3 k Ω and 300 k Ω ;

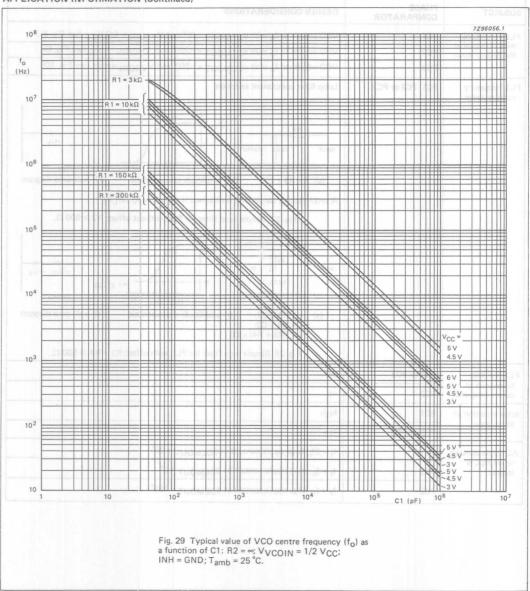
R1 + R2 parallel value > 2.7 k Ω ;

C1 greater than 40 pF.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS							
		VCO frequency characteristic							
VCO frequency without extra offset	PC1, PC2 or PC3	With R2 = ∞ and R1 within the range 3 k Ω < R1 < 300 k Ω , the characteristics of the VCO operation will be as shown in Fig. 25. (Due to R1, C1 time constant a small offset remains when R2 = ∞ .)							
	100 a 100 A 100 A	¹vco							
	For or	for the state of t							
	mearity as a 1								
		Selection of R1 and C1							
	PC1	Given f _O , determine the values of R1 and C1 using Fig. 29.							
	PC2 or PC3	Given f_{max} and f_{o} , determine the values of R1 and C1 using Fig. 29, use Fig. 31 to obtain $2f_L$ and then use this to calculate f_{min} .							
VCO frequency with extra	PC1, PC2 or PC3	VCO frequency characteristic With R1 and R2 within the ranges 3 k Ω < R1 < 300 k Ω , 3 k Ω < R2 < 300 k Ω , the characteristics of the VCO operation will be as shown in Fig. 26.							
offset	Addition to	fvco 7296052.1							
		1 _{max} + + +							
		fo 21 due to R ₁ ,C ₁							
		†min 1 1 1 1 1 1 1 1 1							
		THE COURT OF THE C							
		due to R ₂ ,C ₁							
		0.9 V 1/2 V _{CC} V _{CC} -0.9 V V _{CC}							
	Fig. 24 Typical des	Fig. 26 Frequency characteristic of VCO operating with offset: f_0 = centre frequency; $2f_L$ = frequency lock range.							
	democulation section	Selection of R1, R2 and C1							
	PC1, PC2 or PC3	Given f_0 and f_L , determine the value of product R1C1 by using Fig. 31. Calculate f_0 ff from the equation f_0 ff = f_0 — 1.6 f_L . Obtain the values of C1 and R2 by using Fig. 30.							

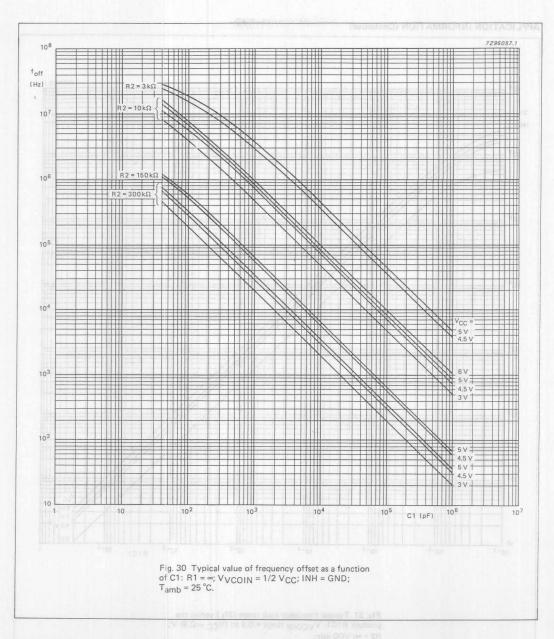
SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS							
PLL conditions	PC1	VCO adjusts to f_0 with $\phi_{DEMOUT} = 90^{\circ}$ and $V_{VCOIN} = 1/2 V_{CC}$ (see Fig. 6).							
with no signal at the SIG _{IN} input	PC2	VCO adjusts to f_0 with $\phi_{DEMOUT} = -360^{\circ}$ and $V_{VCOIN} = min$. (see Fig. 8).							
	PC3	VCO adjusts to f_0 with $\phi_{DEMOUT} = -360^{\circ}$ and $V_{VCOIN} = min$. (see Fig. 10).							
PLL frequency capture range	PC1, PC2 or PC3	Loop filter component selection							
		$\begin{array}{c c} & & & & \\ \hline & & & & \\ \hline & & & & \\ \hline & & & &$							
		(a) $\tau = R3 \times C2$ (b) amplitude characteristic (c) pole-zero diagram							
		A small capture range (2f _C) is obtained if $2f_{\rm C}\approx 1/\pi~(\sqrt{2\pi f_{\rm L}/\tau})$							
		Fig. 27 Simple loop filter for PLL without offset; R3 \geqslant 500 Ω .							
		INPUT C2 F($_{3}\omega$) OUTPUT $_{1}^{R4}$ OUTPUT $_{2}^{C}$ $_{1}^{C}$ $_{1}^{C}$							
		Fig. 28 Simple loop filter for PLL with offset; R3 + R4 \geqslant 500 Ω .							
PLL locks on	PC1 or PC3	yes							
harmonics at centre frequency	PC2	no							
noise rejection at	PC1	high							
signal input	PC2 or PC3	low 100							
AC ripple content when PLL is	PC1	$f_r = 2f_i$, large ripple content at $\phi_{DEMOUT} = 90^\circ$							
locked	PC2	$f_r = f_i$, small ripple content at $\phi_{DEMOUT} = 0^\circ$							
	PC3	$f_r = f_i$, large ripple content at $\phi_{DEMOUT} = 180^\circ$							





Notes to Fig. 29

- 1. To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
- Interpolation for various values of R1 can be easily calculated because, a constant R1C1 product will produce almost the same VCO output frequency.

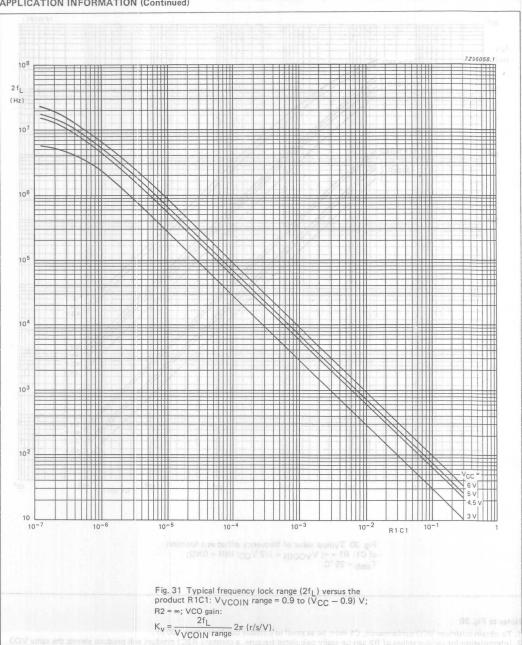


Notes to Fig. 30

1. To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.

2. Interpolation for various values of R2 can be easily calculated because, a constant R2C1 product will produce almost the same VCO output frequency.

APPLICATION INFORMATION (Continued)



PLL design example

The frequency synthesizer, used in the design example shown in Fig. 32, has the following parameters:

Output frequency: 2 MHz to 3 MHz frequency steps : 100 kHz settling time : 1 ms : < 20% overshoot

The open-loop gain is H (s) \times G (s) = $K_{p} \times K_{f} \times K_{o} \times K_{n}$.

Where:

K_p = phase comparator gain Kf = low-pass filter transfer gain $K_0 = K_v/s$ VCO gain $K_n = 1/n$ divider ratio

The programmable counter ratio Kn can be found as follows:

$$N_{min.} = \frac{f_{OUt}}{f_{step}} = \frac{2 \text{ MHz}}{100 \text{ kHz}} = 20$$

$$N_{\text{max.}} = \frac{f_{\text{out}}}{f_{\text{step}}} = \frac{3 \text{ MHz}}{100 \text{ kHz}} = 30$$

The VCO is set by the values of R1, R2 and C1, R2 = $10 \text{ k}\Omega$ (adjustable). The values can be determined using the information in the section "DESIGN CONSIDERATIONS" With f_0 = 2.5 MHz and f_L = 500 kHz this gives the following values (V_{CC} = 5.0 V): $R1 = 10 k\Omega$

 $R2 = 10 k\Omega$ C1 = 500 pF The VCO gain is:

$$K_V = \frac{2f_L \times 2 \times \pi}{0.9 - (V_{CC} - 0.9)} =$$

$$= \frac{1 \text{ MHz}}{3.2} \times 2\pi \approx 2 \times 10^6 \text{ r/s/V}$$

The gain of the phase comparator is:

$$K_p = \frac{V_{CC}}{4 \times \pi} = 0.4 \text{ V/r}.$$

The transfer gain of the filter is given by:

$$K_f = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2) s}$$

Where:

$$\tau_1$$
 = R3C2 and τ_2 = R4C2.

The characteristics equation is: $1 + H(s) \times G(s) = 0$.

This results in:

$$\begin{split} \mathbf{s}^2 + \frac{1 + \mathsf{K}_\mathsf{p} \times \mathsf{K}_\mathsf{v} \times \mathsf{K}_\mathsf{n} \times \tau_2}{(\tau_1 + \tau_2)} \, \mathbf{s} + \\ \frac{\mathsf{K}_\mathsf{p} \times \mathsf{K}_\mathsf{v} \times \mathsf{K}_\mathsf{n}}{(\tau_1 + \tau_2)} &= 0. \end{split}$$

The natural frequency ω_n is defined as

$$\omega_{\rm n} = \sqrt{\frac{K_{\rm p} \times K_{\rm v} \times K_{\rm n}}{(\tau_1 + \tau_2)}}$$

and the damping value ξ is defined as

$$\zeta = \frac{1}{2\omega_n} \times \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)}.$$

In Fig. 33 the output frequency response to a step of input frequency is shown.

The overshoot and settling time percentages are now used to determine $\omega_{\rm n}$. From Fig. 33 it can be seen that the damping ratio \$ = 0.45 will produce an overshoot of less than 20% and settle to within 5% at $\omega_n t = 5$. The required settling time is 1 ms. This results in:

$$\omega_{\rm n} = \frac{5}{\rm t} = \frac{5}{0.001} = 5 \times 10^3 \text{ r/s}.$$

Rewriting the equation for natural frequency results in:

$$(\tau_1 + \tau_2) = \frac{\mathsf{K}_\mathsf{p} \times \mathsf{K}_\mathsf{v} \times \mathsf{K}_\mathsf{n}}{\omega_\mathsf{n}^2}.$$

The maximum overshoot occurs at N_{max}.:

$$(\tau_1 + \tau_2) = \frac{0.4 \times 2 \times 10^6}{5000^2 \times 30} = 0.0011 \text{ s.}$$

When C2 = 470 nF, then

$$R4 = \frac{(\tau_1 + \tau_2) \times 2 \times \omega_{\Pi} \times \zeta - 1}{K_{D} \times K_{V} \times K_{D} \times C2} = 315 \Omega$$

now R3 can be calculated:

$$R3 = \frac{\tau_1}{C2} - R4 = 2 k\Omega.$$

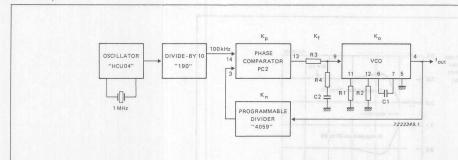
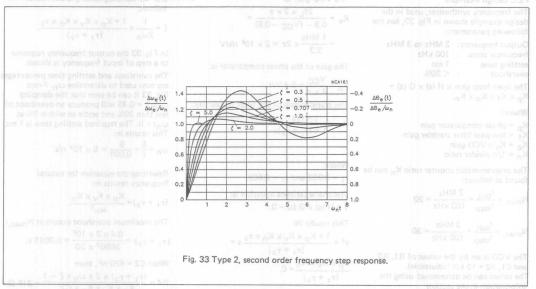


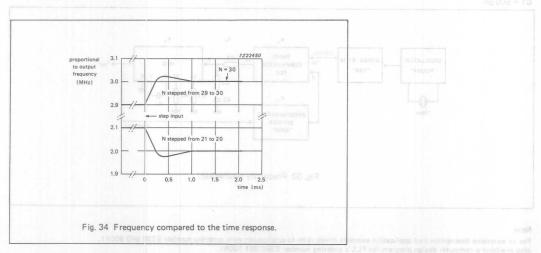
Fig. 32 Frequency synthesizer.

For an extensive description and application example please refer to application note ordering number 9398 649 90011. Also available a computer design program for PLL's ordering number 9398 961 10061.





Since the output frequency is proportional to the VCO control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 9 of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin 9 with a simple RC filter, whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time.



HEX INVERTING HIGH-TO-LOW LEVEL SHIFTER

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC4049 is a high-speed Si-gate CMOS device and is pin compatible with the "4049" of the "40008" series. It is specified in compliance with JEDEC standard no. 7A.

The 74HC4049 provides six inverting buffers with a modified input protection structure, which has no diode connected to VCC. Input voltages of up to 15 V may therefore be used.

This feature enables the inverting buffers to be used as logic level translators, which will convert high level logic to low level logic, while operating from a low voltage power supply. For example 15 V logic ("4000B series") can be converted down to 2 V logic.

The actual input switch level remains related to the V_{CC} and is the same as mentioned in the family characteristics. At the same time each part can be used as a simple inverter without level translation.

APPLICATIONS

 Converting 15 V logic ("4000B" series) down to 2 V logic.

OVMOOL	PARAMETER	CONDITIONS	TYPICAL	UNIT	
SYMBOL	PARAMETER	CONDITIONS	нс		
t _{PHL} / propagation delay t _{PLH} nA to nY		C _L = 15 pF V _{CC} = 5 V	8	ns	
CI	input capacitance	76	3.5	pF	
CPD	power dissipation capacitance per buffer	note 1	14	pF	

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6ns$$

Note

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

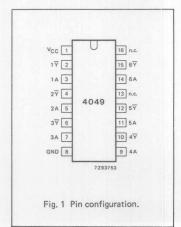
- f; = input frequency in MHz f_O = output frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V
- ut frequency in MHz VCC = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

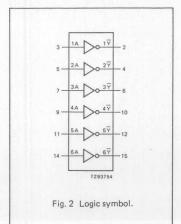
PACKAGE OUTLINES

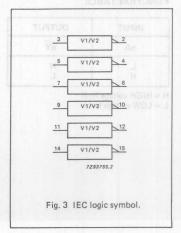
16-lead DIL; plastic (SOT38Z). 16-lead mini-pack; plastic (SO16; SOT109A).

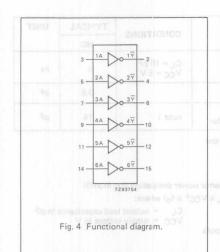
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	Vcc	positive supply voltage
2, 4, 6, 10, 12, 15	1 √ to 6 √	data outputs
3, 5, 7, 9, 11, 14	1A to 6A	data inputs a level and margally sign. I 8 and
8	GND	ground (0 V)
13, 16	n.c.	not connected









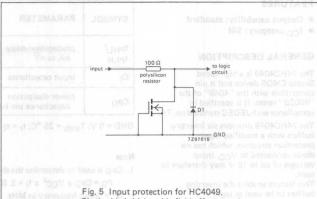
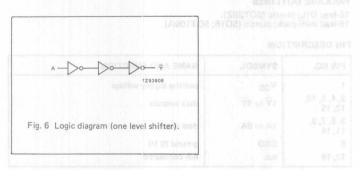


Fig. 5 Input protection for HC4049. Single sided thick oxide field effect metal gate transistor as input protection.



 Conversing 15 V logic ("4000B" series) down to 7 V logic.

FUNCTION TABLE

INPUT	OUTPUT
nA	nΨ
L 3- 8	Н
Н	L

H = HIGH voltage level L = LOW voltage level







RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134) Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
Vcc	DC supply voltage	-0.5	+7	V	YMBOL PARAMETER +25
VIK	DC input voltage range	-0.5	+16	V	min typ, mex.
-IIK	DC input diode current		20	mA	for V _I < -0.5 V
±IOK	DC output diode current		20	mA	for $V_0 < -0.5 \text{V}$ or $V_0 > V_{CC} + 0.5 \text{V}$
±ΙΟ	DC output source or sink current - standard outputs	1 0.6 1.35 1.8	25	mA	for =0.5 V < V ₀ < V _{CC} + 0.5 V
±ICC; ±IGND	DC V _{CC} or GND current for types with: - standard outputs		50	9.1 A.A mA	HIGH level output voltage 4,4 4,5 4,5 4,5 4,5 4,5 4,6 4,5 4,6 4,5 4,6 4,6 4,6 4,6 4,6 4,6 4,6 4,6 4,6 4,6
T _{stg}	storage temperature range	-65	+150	°C	HOH level output voluge 13.88
Ptot Au O	power dissipation per package	1.0 1.0 1.0 1.0	750	mW	for temperature range: -40 to +125 °C 74HC above +70 °C: derate linearly with 12 mW/K
Am 0.	plastic mini-pack (SO)	4.0	400	mW	above +70 °C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER			74HC		UNIT	CONDITIONS	
	PARAMETER	min.	typ.	max.	ONT	CONDITIONS		
Vcc	DC supply voltage		2.0	5.0	6.0	V		
VI	DC input voltage range		GND	- 0	15	V	umo Aiddns tuenearch	
T _{amb}	operating ambient temperature range		-40		+85	°C	see DC and AC	
T _{amb}	operating ambient temperature range		-40		+125	°C	characteristics	
	поиор таат		(34)	dna ^T	1000 500		V _{CC} = 2.0 V; V _{IN} = 2.0 V V _{CC} = 4.5 V; V _{IN} = 4.5 V	
t _r , t _f input rise and fall tim	input rise and fall times		9	6.0	400 650	ns	VCC = 4.5 V, VIN = 4.5 V VCC = 6.0 V; VIN = 6.0 V VCC = 6.0 V; VIN = 10.0 V VCC = 6.0 V; VIN = 15.0 V	
	UNIT VOC WAVEFOR	40 to +125	281 6	05	1000			

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V) [AET 3EII] mercy/8 mumixaM analogs/A and draw sponsible are or souleview grid

		-			Tamb	(°C)			0 0000	pathy med	TEST C	ONDITIONS	
		74HC								METER	RYMBOL PARAM		
SYMBOL	PARAMETER		+25		-40 to +85 -		-40 1	-40 to +125		V _C C V	VI	OTHER	
		min.	typ.	max.	min.	max.	min.	max.		ge rang	striov ro	FIK DC init	
VIH	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1	V tol	1.5 3.15 4.2	en.	1.5 3.15 4.2		V	2.0 4.5 6.0		-lik DC ind	
VIL	LOW level input voltage	≥¦oV.	0.7 1.8 2.3	0.5 1.35 1.8	A	0.5 1.35 1.8	ag	0.5 1.35 1.8	V	2.0 4.5 6.0	por non	tuo Oid Oili Insta-	
Vон	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9	m	1.9 4.4 5.9		v ine	2.0 4.5 6.0	VIH or VIL	$-1_0 = 20 \mu A$ $-1_0 = 20 \mu A$ $-1_0 = 20 \mu A$	
V _{OH}	HIGH level output voltage standard outputs	3.98 5.48			3.84 5.34	a a	3.7 5.2	88-	V agni	4.5 6.0	VIH or VIL	-I _O = 4.0 mA -I _O = 5.2 mA	
VOL	LOW level output voltage all outputs	arido ::	POR	0.1 0.1 0.1	199	0.1 0.1 0.1	bev	0.1 0.1 0.1	V	2.0 4.5 6.0	VIH or VIL	I _O = 20 μA I _O = 20 μA I _O = 20 μA	
VOL	LOW level output voltage standard outputs	enso d)° 07+	0.26 0.26	100	0.33 0.33	400	0.4 0.4	V	4.5 6.0	VIH or VIL	10 = 4.0 mA 10 = 5.2 mA	
				0.1		1.0		21.0	μΑοο	6.0	VCC or GND	ECOMMENDED	
± 1 ₁	input leakage current		.008011	0.5) d	5.0		5.0	μА	2.0 to 6.0	15 V	SYMBOL PA	
¹ CC	quiescent supply current	1	0.0 at	2.0	8	20.0		40.0	μΑ	6.0	15 V or GND		

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	VGC = 2.0 V; VM = 2.0 V VGC = 3.5 V; VM = 4.5 V		T _{amb} (°C)							TEST CONDITIONS	
SYMBOL PARAMETER	The state of the s	904 974HC								t fielt b	to to input rise and
		+25		-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/ tPLH	propagation delay nA to $n\overline{Y}$		28 10 8	85 17 14		105 21 18		130 26 22	ns	2.0 4.5 6.0	Fig. 7
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

AC WAVEFORMS

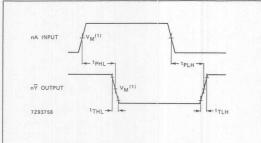
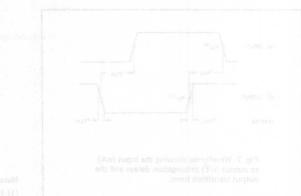


Fig. 7 Waveforms showing the input (nA) to output (n \overline{Y}) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

AC WAYERSRIMS



Note to AC wavelorms 1) BC: V_M ~ 60%; V_I = GMD to V_{CC}.

HEX HIGH-TO-LOW LEVEL SHIFTER

FEATURES

• Output capability: standard

· ICC category: SSI

GENERAL DESCRIPTION

The 74HC4050 is a high-speed Si-gate CMOS device and is pin compatible with the "4050" of the "4000B" series. It is specified in compliance with JEDEC standard no. 7A.

The 74HC4050 provides six non-inverting buffers with a modified input protection structure, which has no diode connected to V_{CC}. Input voltages of up to 15 V may therefore be used. This feature enables the non-inverting buffers to be used as logic level translators, which will convert high level logic to low level logic, while operating from a low voltage power supply. For example 15 V logic ("4000B series") can be converted down to 2 V logic.

The actual input switch level remains related to the V_{CC} and is the same as mentioned in the family characteristics.

APPLICATIONS

 Converting 15 V logic ("4000B" series) down to 2 V logic.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
	PARAMETER	CONDITIONS	нс	
t _{PHL} /	propagation delay nA to nY	C _L = 15 pF V _{CC} = 5 V	7	ns
CI	input capacitance	y y	3,5	pF
CPD power dissipation capacitance per buffer		note 1	14	pF

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Note

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_0)$ where:

f_i = input frequency in MHz f_O = output frequency in MHz CL = output load capacitance in pF

VCC = supply voltage in V

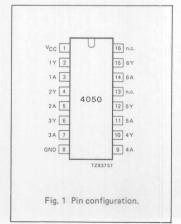
 $\Sigma (C_L \times V_{CC})^2 \times f_0 = \text{sum of outputs}$

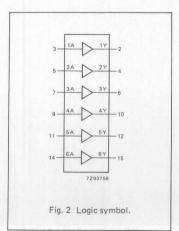
PACKAGE OUTLINES

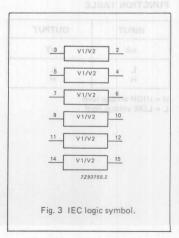
16-lead DIL; plastic (SOT38Z). 16-lead mini-pack; plastic (SO16; SOT109A).

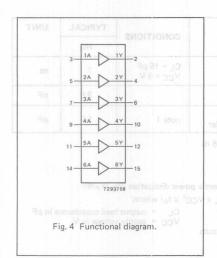
PIN DESCRIPTION

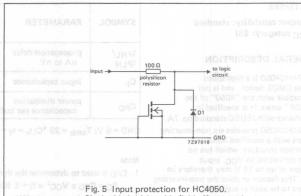
PIN NO.	SYMBOL	NAME AND FUNCTION						
1	Vcc	positive supply voltage						
2, 4, 6, 10, 12, 15	1Y to 6Y	data outputs						
3, 5, 7, 9, 11, 14	1A to 6A	data inputs feed and compalls aged 3, st-7						
8	GND	ground (0 V)						
13, 16	n.c.	not connected						











SHM of your super Single sided thick oxide field effect metal at Many shaupad a gate transistor as input protection.

Fig. 6 Logic diagram (one level shifter).

FUNCTION TABLE

INPUT	OUTPUT
nA_	nY
L	L
Н	Н

H = HIGH voltage level

L = LOW voltage level





RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
Vcc	DC supply voltage	-0.5	+7	V	YERRARITER
VIK	DC input voltage range	-0.5	+16	V	min. typ. max.
-I _{IK}	DC input diode current	1 2	20	mA	for V _I < -0.5 V
±IOK	DC output diode current	1 3	20	mA	for $V_0 < -0.5 \text{ V}$ or $V_0 > V_{CC} + 0.5 \text{ V}$
±ΙΟ	DC output source or sink current - standard outputs	8.0 8.1	25	mA	for -0.5 V < V _O < V _{CC} + 0.5 V
±ICC; ±IGND	DC VCC or GND current for types with: - standard outputs		50	mA	MIGH level output voltage 4.8 2.0 e.s els outputs sil outputs
T _{stg}	storage temperature range	-65	+150	°C	HIGH level output voltage 3.03
P _{tot}	power dissipation per package	10	750	mW	for temperature range: —40 to +125 °C 74HC above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)	4.0	500	mW	above +70 °C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74HC		UNIT	CONDITIONS
STWIBOL	PARAMETER AA 0.3	min.	typ.	max.	UNIT	CONDITIONS
Vcc	DC supply voltage	2.0	5.0	6.0	V	
VI	DC input voltage range	GND	1-1	15	V	The Antidoo Montains 1
T _{amb}	operating ambient temperature range	-40		+85	°C	see DC and AC
T _{amb}	operating ambient temperature range	-40		+125	°C	characteristics
t _r , t _f	input rise and fall times	(91)	6.0	1000 500 400 650 1000	ns	V _{CC} = 2.0 V; V _{IN} = 2.0 V V _{CC} = 4.5 V; V _{IN} = 4.5 V V _{CC} = 6.0 V; V _{IN} = 6.0 V V _{CC} = 6.0 V; V _{IN} = 10.0 V V _{CC} = 6.0 V; V _{IN} = 15.0 V

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V) [883 DBI) analysis murnixal/studoed A art of the complete goldeni 1

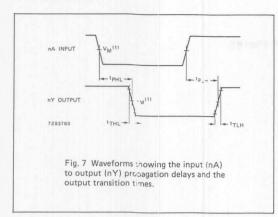
					Tamb (°C)			= punor	y una	TEST C	ONDITIONS
		N/S	OFFICE	100-	74HC	A.X.	M .V	184		9	AMETE	SYMBOL PAR
SYMBOL	PARAMETER	+25			-40	to +85	-40 t	o +125	UNIT	VCC	VI	OTHER
		min.	typ.	max.	min.	max.	min.	max.	991	ten soed	kw mge	V _{IK} DC.
VIH	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1	noi soi	1.5 3.15 4.2		1.5 3.15 4.2		v tne	2.0 4.5 6.0	olb augr	-tue 00.s
VIL	LOW level input voltage	oV >	0.7 1.8 2.3	0.5 1.35 1.8	Agg	0.5 1.35 1.8	35	0.5 1.35 1.8	v sinis	2.0 4.5 6.0	né manyo tné poeto	o 20 gla nuo de -
V _{OH}	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		v Imani	2.0 4.5 6.0	VIH or VIL	$-1_0 = 20 \mu A$ $-1_0 = 20 \mu A$ $-1_0 = 20 \mu A$
V _{OH}	HIGH level output voltage standard outputs	3.98 5.48			3.84 5.34	-08	3.7 5.2		V	4.5 6.0	VIH or VIL	-I _O = 4.0 mA -I _O = 5.2 mA
VoL	LOW level output voltage all outputs	C. del	2 2 e +70	0.1 0.1 0.1	Wite	0.1 0.1 0.1	35	0.1 0.1 0.1	V	2.0 4.5 6.0	VIH or VIL	I _O = 20 μA I _O = 20 μA I _O = 20 μA
VoL	LOW level output voltage standard outputs	C: de	e + 70	0.26 0.26	Vite	0.33	ne	0.4 0.4	v	4.5 6.0	VIH or VIL	1 _O = 4.0 mA 1 _O = 5.2 mA
				0.1		1.0		1.0	μΑ	6.0	VCC or GND	ECOMMENDES
±II	input leakage current	-	.xam	0.5	 	5.0		5.0	μΑ	2.0 to 6.0	15 V	SYMBOL PA
Icc	quiescent supply current	V	0.8	2.0	5 5	20.0		40.0	μΑ	6.0	15 V or GND	Vec De

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	VCC = 4.5 V; V;N = VCC = 6.0 V; V;N =		008		Tamb		TEST CONDITIONS					
	PARAMETER				74H							
			+2	5	-40	-40 to +85 -40			UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/ tPLH	propagation delay nA to nY		25 9 7	85 17 14		105 21 18		130 26 22	ns	2.0 4.5 6.0	Fig. 7	
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7	

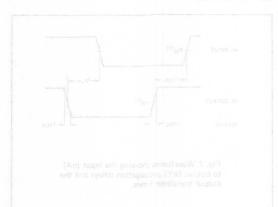
AC WAVEFORMS



Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.





Note to AC waveforms (1) NC : V_M = 50%; V, 4 GND to V_{CC} HCT: V_M = 1,3 V; V_I = 6ND to 3 V.

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- Wide analog input voltage range:
 ± 5 V.
- Low "ON" resistance: 80 Ω (typ.) at $V_{CC} V_{EE} = 4.5 \text{ V}$ 70 Ω (typ.) at $V_{CC} V_{EE} = 6.0 \text{ V}$ 60 Ω (typ.) at $V_{CC} V_{EE} = 9.0 \text{ V}$
- Logic level translation: to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4051 are high-speed Si-gate CMOS devices and are pin compatible with the "4051" of the "40008" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4051 are 8-channel analog multiplexers/demultiplexers with three digital select inputs (S_0 to S_2), an active LOW enable input (\overline{E}), eight independent inputs/outputs (Y_0 to Y_7) and a common input/output (Z).

With E LOW, one of the eight switches is selected (low impedance ON-state) by S₀ to S₂. With E HIGH, all switches are in the high impedance OFF-state, independent of S₀ to S₂.

 V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0 to S_2 , and Ξ). The V_{CC} to GND ranges are Ξ .0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (Y_0 to Y_7 , and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, VEE is connected to GND (typically ground).

CATIONS		CONDITIONS	TYF	PICAL	UNIT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	ONT	
t _{PZH} /	turn "ON" time E to V _{os} S _n to V _{os}	C _L = 15 pF R _L = 1 kΩ	22 20	22 24	ns ns	
t _{PHZ} /	turn "OFF" time E to V _{os} S _n to V _{os}	V _{CC} = 5 V	18 19	16 20		
C ₁ S ²	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per switch	notes 1 and 2	25	25	pF	
CS	max. switch capacitance independent (Y) common (Z)		5 25	5 25	pF pF	

 $V_{EE} = GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$ Notes

1. $\mathrm{C_{PD}}$ is used to determine the dynamic power dissipation ($\mathrm{P_D}$ in $\mu\mathrm{W}$):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L + C_S) \times V_{CC}^2 \times f_o)$ where:

2. For HC $\,$ the condition is V $_{I}$ = GND to V $_{CC}$ $\,$ For HCT the condition is V $_{I}$ = GND to V $_{CC}$ - 1.5 V $\,$

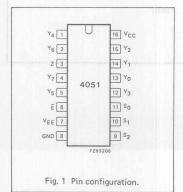
PACKAGE OUTLINES

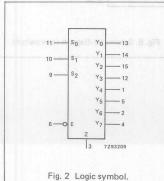
16-lead DIL; plastic (SOT38Z).

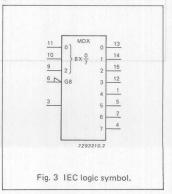
16-lead mini-pack; plastic (SO16; SOT109A).

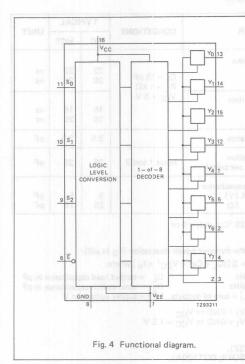
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3	Z E	common input/output enable input (active LOW)
7	VEE	negative supply voltage
8	GND	ground (0 V)
11, 10, 9	S ₀ to S ₂	select inputs
13, 14, 15, 12, 1, 5, 2, 4	Yo to Y7	independent inputs/outputs
16	Vcc	positive supply voltage









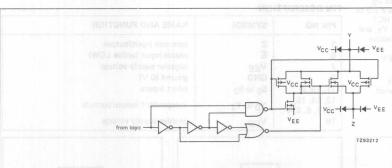
APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and 90 0 (typ.) at V_{CC} – V_{EE} = 4.5 V V 0 0 (typ.) at V_{CC} – V_{EE} = 6.0 V 0 0 0 (typ.) at V_{CC} – V_{EE} = 9.0 V Logic level unstations: demultiplexing
- Signal gating

FUNCTION TABLE

Sec	INF	PUTS	9753	channel
υςĒ	s ₂	S ₁	s ₀	ON
L L X	L L L	L H H	L H L H	$Y_0 - Z$ $Y_1 - Z$ $Y_2 - Z$ $Y_3 - Z$
L VL	H H OHO H	L L H	L H L H	Y ₄ - Z Y ₅ - Z Y ₆ - Z Y ₇ - Z
ob H	X	X	X	none

H = HIGH voltage level L = LOW voltage level X = don't care



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to VEE = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
Vcc	DC supply voltage	-0.5	+11.0	V	
±1IK	DC digital input diode current		20	mA	for $V_1 < -0.5 \text{ V}$ or $V_1 > V_{CC} + 0.5 \text{ V}$
±I _{SK}	DC switch diode current		20	mA	for V_S < -0.5 V or V_S > V_{CC} + 0.5 V
±1 _S	DC switch current		25	mA	for $-0.5 \text{ V} < \text{V}_{\text{S}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$
±1EE	DC V _{EE} current		20	mA	
±I _{CC} ; ±I _{GND}	DC V _{CC} or GND current		50	mA	101 0 1 2 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1
T _{stg}	storage temperature range	-65	+150	°C	
P _{tot}	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL	7 600	750	mW	above +70 °C: derate linearly with 12 mW/K and a pine
	plastic mini-pack (SO)	TIDV YIGG	500	mW	above +70 °C: derate linearly with 8 mW/K
Ps	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Y_{n} , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Y_{n} . In this case there is no limit for the voltage drop across the switch, but the voltages at Y_{n} and Z may not exceed V_{CC} or V_{EE} .

RECOMMENDED OPERATING CONDITIONS

SYMBOL	UNIT Vec Vee Is		74HC			74НСТ		SB	SYMBOL PARAMET
STWIBOL	PARAMETER V dS1+or	min.	typ.	max.	min.	typ.	max.	UNIT	CONDITIONS
Vcc	DC supply voltage V _{CC} -GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
V _{CC}	DC supply voltage V _{CC} -V _{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
V _I	DC input voltage range	GND	eei	Vcc	GND		Vcc	V	
Vs	DC switch voltage range	VEE	av1	Vcc	VEE		Vcc	V	
T _{amb}	operating ambient temperature range	-40	150	+85	-40		+85	°C	see DC and AC
T _{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	CHARACTERISTICS
t _r , t _f	input rise and fall times		6.0	1000 500 400 250	3 93 3 08 10 08	6.0	500	(fier) eor	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V V _{CC} = 10.0 V

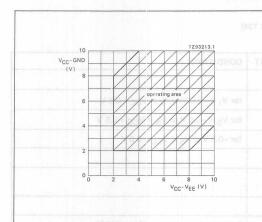


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4051.

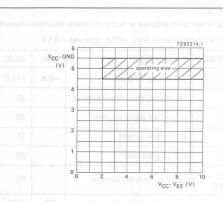


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4051.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} – GND or V_{CC} – V_{EE} = 2.0, 4.5, 6.0 and 9.0 V For 74HCT: V_{CC} – GND = 4.5 and 5.5 V; V_{CC} – V_{EE} = 2.0, 4.5, 6.0 and 9.0 V

						T _{amb} (°C)					TEST	COND	TION	S
0)/440.01	DADAMETED.			7	4HC/H	нст	sano3	CANADA	una n	- USG		Desi			
SYMBOL	PARAMETER		+25		-40 to +85		-40 to +125		UNIT	VCC	VEE	IS μA	Vis	VI	
			min.	typ.	max.	min.	max.	min.	max.						
RON	ON resistance (peak)	10.D	0.8	100 90 70	180 160 130	TE V	- 225 200 165	2.0	_ 270 240 195	ΩΩΩ	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	V _{CC} to V _{EE}	or
RON	ON resistance (rail)	-Vcc +85		150 80 70 60	140 120 105	av Ba	- 175 150 130	3V 94-	- 210 180 160	Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	VEE	VIH or VIL
RON	ON resistance (rail)	900	0.8	150 90 80 65	- 160 140 120	or l	- 200 175 150	4-	240 210 180	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	Vcc	V _{IH} or V _{IL}
ΔR _{ON}	maximum ∆ON resist between any two ch			9 8 6	1 0					Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5		V _{CC} to V _{EE}	VIH or VIL

Notes to DC characteristics

- At supply voltages (V_{CC} V_{EE}) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
 For test circuit measuring R_{ON} see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

	TEST CONDITIO			Т	amb (°C)					TEST	COND	ITIONS
	PARAMETER 30V TW				74H0	ΣŢ	UNIT	.,	.,	.,	OTHER		
SYMBOL		+25			-40 to +85		-40 to +125		UNIT	V _{CC}	VEE	VI	OTHER
		min.	typ.	max.	min.	max.	min.	max.					
V _{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3	1044	V	2.0 4.5 6.0 9.0		spaqone V _{is} to	भ 14 ₁ गिम्ब्
: 02 = 50 n V _{IL} s £ s: J V		0.00	0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7	43 88 73 44	0.5 1.35 1.8 2.7	66 1 63 1	0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0	N" tin	O" mun V or II	724s /HZ4s
±113=10:	input leakage current	CD (S)	92 10 92	0.1	43 86 73	1.0 2.0	34 36 36 36 36 36	1.0 2.0	μΑ	6.0	0	V _{CC} or GND	724; ;H24;
±IS	analog switch OFF-state current per channel		43	0.1	73	1.0	195 5 35 1	1.0	μΑ	10.0	0	V _{IH} or V _{IL}	V _S I = V _{CC} - V _E (see Fig. 10
±Is	analog switch OFF-state current all channels	8	42	0.4	58 26 73	4.0	2 42 1 29	4.0	μΑ	10.0	0	V _{IH} or V _{IL}	V _S I = V _{CC} - V _E (see Fig. 10
±IS	analog switch ON-state current		74	0.4	82	4.0	84 8 8 42 8	4.0	μΑ	10.0	0	V _{IH} or V _{IL}	V _S I = V _{CC} - V _E (see Fig. 11
Icc	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μΑ	6.0	0	V _{CC} or GND	V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	TEST CONDIT				T _{amb} ((°C)					TEST	CONDITIONS	
					74H	C					.,	OTUED	
SYMBOL	PARAMETER		351 +25			to +85	-40 to +125		UNIT	V _{CC}	VEE	OTHER	
		min.	typ.	max.	min.	max.	min.	max.	1				
t _{PHL} /	propagation delay V _{is} to V _{os}		14 5 4 4	60 12 10 8	ä	75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = \infty$; $C_L = 50 \text{ pF}$ (see Fig. 17)	
^t PZH [/] ^t PZL	turn "ON" time	35 8	72 29 21 18	345 69 59 51	1.6	430 86 73 64	8 0.5 1,2 1,8 1 1,8	520 104 88 77	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_{L} = 1 \text{ k}\Omega$; $C_{L} = 50 \text{ pF}$ (see Figs 18, 19 and 20	
t _{PZH} / t _{PZL}	turn "ON" time S _n to V _{os}	4 0	66 28 19 16	345 69 59 51	2.0	430 86 73 64	0.1	520 104 88 77	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 18, 19 and 20	
tPHZ/ tPLZ	turn "OFF" time Ē to V _{os}	0	58 31 17 18	290 58 49 42	0 1	365 73 62 53	0.0	435 87 74 72	ns	2.0 4.5 6.0 4.5		$R_{L} = 1 \text{ k}\Omega$; $C_{L} = 50 \text{ pF}$ (see Figs 18, 19 and 20	
t _{PHZ} / t _{PLZ}	turn "OFF" time S _n to V _{os}		61 25 18 18	290 58 49 42	E.A	365 73 62 53	9:0 9:0	435 87 74 72	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 18, 19 and 20	

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

81/1	теат сопритю			T	amb (°C)				TEST CONDITIONS				
0.44501					74HC	Tor			UNIT				OTHER	
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNII	V _{CC}	VEE	VITA	OTHER	
		min.	typ.	max.	min.	max.	min.	max.						
V _{IH} (HIGH level input voltage	2.0	1.6		2.0		2.0	3 4	V	4.5 to 5.5	ion del co	Vis to	Kld ₁	
VIL	LOW level input voltage	0	1.2	0.8	88 88	0.8	39	0.8	V	4.5 to 5.5	anit "L	E to V	/HZds	
±1100 = 10	input leakage current		68	0.1	58 L 04 L	1.0	64 1 SE 1	1.0	μΑ	5.5	0	V _C C or GND	Z Jas shds	
±IS	analog switch OFF-state current per channel	n	38) 54	0.1	01-	1.0	32	1.0	μΑ	10.0	0	V _{IH} or V _{IL}	IV _S I = V _{CC} - V _{EE} (see Fig. 10)	
±IS	analog switch OFF-state current all channels		101	0.4		4.0		4.0	μΑ	10.0	0	V _{IH} or V _{IL}	IV _S I = V _{CC} - V _{EE} (see Fig. 10)	
±IS	analog switch ON-state current		(12) (8)	0.4		4.0		4.0	μА	10.0	0	V _{IH} or V _{IL}	IV _S I = V _{CC} - V _{EE} (see Fig. 11)	
Icc	quiescent supply current		14	8.0 16.0		80.0 160.0		160.0 320.0	μΑ	5.5 5.0	0 -5.0	VCC or GND	V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}	
ΔICC	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450	erskys	490	μΑ	4.5 to 5.5	0	V _{CC} -2.1V	other inputs at V _{CC} or GND	

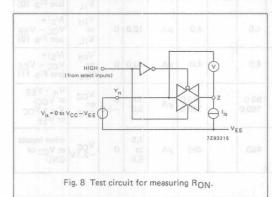
Note to HCT types

INPUT	UNIT LOAD COEFFICIENT
S _n E	0.50 0.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

SNO	TEST CONDITI			Т	amb	(°C)					TEST	CONDITIONS
	OLI - WILLIAM TO THE	00			74HC	TAT				.,	Vaar	OTHER 9 JOBMYS
SYMBOL	PARAMETER	125	+25	à- a	-40	to +85	-40 t	o +125	UNIT	VCC	V _{EE}	OTHER
		min.	typ.	max.	min.	max.	min.	max.	167			
t _{PHL} /	propagation delay Vis to Vos	V	5 4	12		15 10		18 12	ns	4.5 4.5	0 -4.5	R _L = ∞; C _L = 50 pF (see Fig. 17)
t _{PZH} /	turn "ON" time E to V _{os}		26 16	55 39		69 49		83 59	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Figs 18, 19 and 20)
t _{PZH} /	turn "ON" time S _n to V _{os}		28 16	55 39	3.01	69 49	6,0	83 59	ns	4.5 4.5	0 -4.5	$R_{L} = 1 \text{ k}\Omega$; $C_{L} = 50 \text{ pF}$ (see Figs 18, 19 and 20)
t _{PHZ} /	turn "OFF" time E to Vos	Au 0	19 16	45 32	2.1	56 40	1.0	68 48	ns	4.5 4.5	0 -4.5	$R_{L} = 1 \text{ k}\Omega$; $C_{L} = 50 \text{ pF}$ (see Figs 18, 19 and 20)
t _{PHZ} /	turn "OFF" time S _n to V _{os}	All o	23 16	45 32		56 40	1.0	68 48	ns	4.5 4.5	0 -4.5	$R_{L} = 1 \text{ k}\Omega$; $C_{L} = 50 \text{ pF}$ (see Figs 18, 19 and 20)



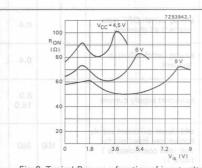
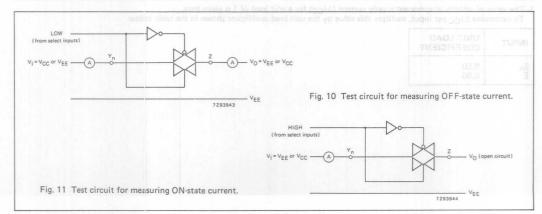


Fig. 9 Typical R $_{ON}$ as a function of input voltage V $_{is}$ for V $_{is}$ = 0 to V $_{CC}$ – V $_{EE}.$



ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

 $GND = 0 V; T_{amb} = 25 °C$

SYMBOL	PARAMETER DO STORE	typ.	UNIT	V _{CC}	VEE	V _{is(p-p)}	CONDITIONS
SV.	sine-wave distortion f = 1 kHz	0.04 0.02	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10 \text{ k}\Omega; C_L = 50 \text{ pF}$ (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600 \Omega$; $C_L = 50 pF$ (see Figs 12 and 15)
V _(p-p)	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5	DE 691	$R_L = 600 \Omega$; $C_L = 50 pF$; $f = 1 MHz$ ($E \text{ or } S_D$, square-wave between V_{CC} and GND , $t_r = t_f = 6 ns$) (see Fig. 16)
f _{max}	minimum frequency response (–3dB)	170 180	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	$R_L = 50 \Omega$; $C_L = 10 pF$ (see Figs 13 and 14)
CS	maximum switch capacitance independent (Y) common (Z)	5 25	pF pF			ALC:	Nay.

Notes to AC characteristics

 V_{is} is the input voltage at a Y_{η} or Z terminal. whichever is assigned as an input. V_{Os} is the output voltage at a Y_{η} or Z terminal, whichever is assigned as an output.

- 1. Adjust input voltage V_{js} to 0 dBm level (0 dBm = 1 mW into 600 Ω). 2. Adjust input voltage V_{is} to 0 dBm level at V_{OS} for 1 MHz (0 dBm = 1 mW into 50 Ω).

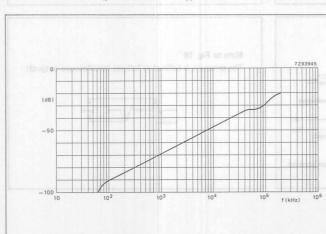
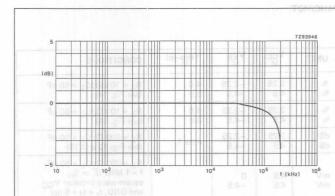


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13 TEMARAR JOBMY2

Test conditions: $\begin{array}{l} \text{V}_{\text{CC}} = 4.5 \text{ V; GND} = 0 \text{ V; V}_{\text{EE}} = -4.5 \text{ V;} \\ \text{R}_{\text{L}} = 50 \; \Omega; \; \text{R}_{\text{source}} = 1 \text{ k} \Omega \end{array}$

Fig. 13 Typical frequency response.

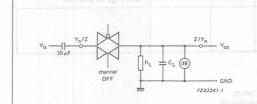


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

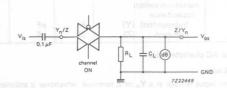


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

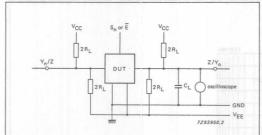
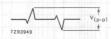


Fig. 16 Test circuit for measuring crosstalk between control and any switch,

Note to Fig. 16

The crosstalk is defined as follows (oscilloscope output):



AC WAVEFORMS

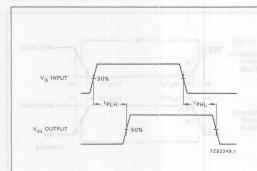


Fig. 17 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

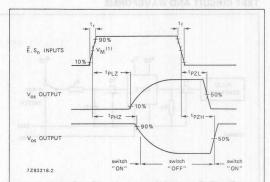


Fig. 18 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 18

(1) HC : $V_M = 50\%$; $V_I = GND \text{ to } V_{CC}$. HCT: $V_M = 1.3 \text{ V}$; $V_I = GND \text{ to } 3 \text{ V}$.

TEST CIRCUIT AND WAVEFORMS

AC WAVEFORMS

t_r; t_f

OTHER

6 ns

6 ns

f_{max}; PULSE WIDTH

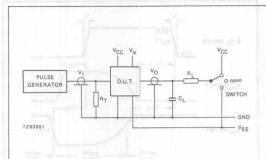


Fig. 19 Test circuit for measuring AC performance.

NEGATIVE 10% NEGATIVE 10% VM 10% 17HL(t_f) 17HL(t_f) 17HL(t_f) AMPLITUDE AMPLITUDE 10% THL(t_f) 17HL(t_f) 17HL(t_f)

Fig. 20 Input pulse definitions.

Conditions

TEST	SWITCH	Vis
tPZH	VEE	VCC
tPZL	VCC	VEE
tPHZ	VEE	VCC
tPLZ	VCC	VEE
others	open	pulse

74HC V_{CC} 50% < 2 ns 74HCT 3.0 V 1.3 V < 2 ns

FAMILY AMPLITUDE VM

Definitions for Figs 19 and 20:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

 $R_T=$ termination resistance should be equal to the output impedance Z_O of the pulse generator.

 $t_r = t_f = 6$ ns; when measuring f_{max} , there is no constraint to t_r , t_f with 50% duty factor.

888

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- Wide analog input voltage range: xelogists ± 5 V.
- Low "ON" resistance: 80 Ω (typ.) at V_{CC} V_{EE} = 4.5 V move 70 Ω (typ.) at V_{CC} V_{EE} = 6.0 V 60 Ω (typ.) at V_{CC} V_{EE} = 9.0 V
- Logic level translation: to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4052 are high-speed Si-gate CMOS devices and are pin compatible with the "4052" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A,

The 74HC/HCT4052 are dual 4-channel analog multiplexers/demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs (nY₀ to nY₃) and a common input/output (nZ). The common channel select logics include two digital select inputs (S₀ and S₁) and an active LOW enable input (E).

With \overline{E} LOW, one of the four switches is selected (low impedance ON-state) by S_0 and S_1 . With \overline{E} HIGH, all switches are in the high impedance OFF-state, independent of S_0 and S_1 .

 V_{CC} and GND are the supply voltage pins for the digital control inputs (S0 and S1, and E). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY0 to nY3, and nZ) con swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC}-V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, VEE is connected to GND (typically ground).

MPPLICATI		CONDITIONS	TYF	PICAL	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
tPZH/	turn "ON" time E or S _n to V _{os}	C _L = 15 pF 	28	18	ns
t _{PHZ} /	turn "OFF" time E or S _n to V _{os}	V _{CC} = 5 V	21	13	ns
CI	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per switch	notes 1 and 2	57	57	pF
CS	max. switch capacitance independent (Y) common (Z)	1-of-4 DECODER	5 12	5 12	pF pF

$$V_{EE} = GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

1. CpD is used to determine the dynamic power dissipation (PD in μ W):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:

2. For HC the condition is V_1 = GND to V_{CC} For HCT the condition is V_1 = GND to V_{CC} – 1.5 V

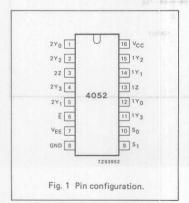
PACKAGE OUTLINES

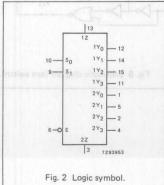
16-lead DIL; plastic (SOT38Z).

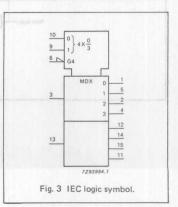
16-lead mini-pack; plastic (SO16; SOT109A).

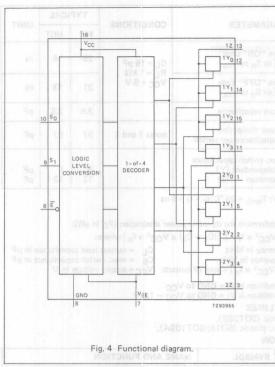
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5, 2, 4	2Y ₀ to 2Y ₃	independent inputs/outputs
6	Ē	enable input (active LOW)
7	VEE	negative supply voltage
8	GND	ground (0 V)
10, 9	S ₀ , S ₁	select inputs
12, 14, 15, 11	1Y ₀ to 1Y ₃	independent inputs/outputs
13, 3	1Z, 2Z	common inputs/outputs
16	Vcc	positive supply voltage









APPLICATIONS

- Analog multiplexing and spation angle golsten about a demultiplexing
- Digital multiplexing and people relies "MO" wo.1
- demultiplexing and say 30 h law 10 a Signal gating

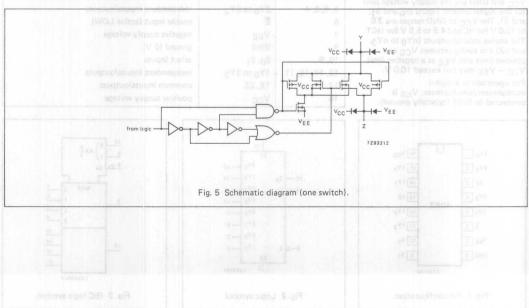
FUNCTION TABLE

	INPUTS	3	CHANNEL
Ē	S ₁	s ₀	ON
L L L	L L 2H H	L H L	$ \begin{array}{r} nY_0 - nZ \\ nY_1 - nZ \\ nY_2 - nZ \\ nY_3 - nZ \end{array} $
Н	X	X	none

H = HIGH voltage level

L = LOW voltage level

X = don't care



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to VEE = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
Vcc	DC supply voltage	-0.5	+11.0	V	
±11K	DC digital input diode current		20	mA	for $V_1 < -0.5 \text{ V}$ or $V_1 > V_{CC} + 0.5 \text{ V}$
± ISK	DC switch diode current		20	mA	for V_S < -0.5 V or V_S > V_{CC} + 0.5 V
±I _S	DC switch current		25	mA	for -0.5 V < V _S < V _{CC} + 0.5 V
±1EE	DC V _{EE} current		20	mA	
±ICC; ±IGND	DC V _{CC} or GND current		50	mA	71 3 a a 2 2 a
T _{stg}	storage temperature range	-65	+150	°C	
P _{tot}	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL a milanago beamon	g 7 Gua	750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)	iqv ylqq	500	mW	above +70 °C: derate linearly with 8 mW/K
Ps	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminals nZ, when switch current flows in terminals nY_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ, no V_{CC} current will flow out of terminals nY_n. In this case there is no limit for the voltage drop across the switch, but the voltages at nY_n and nZ may not exceed V_{CC} or V_{EE} .

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74HC		97.	74HCT			
STIVIBUL	PARAMETER	min.	typ.	max.	min.	typ.	max.	UNIT	CONDITIONS
Vcc oo	DC supply voltage V _{CC} —GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
V _{CC}	DC supply voltage V _{CC} -V _{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
VI	DC input voltage range	GND		Vcc	GND		VCC	V	
V _S	DC switch voltage range	VEE	175	Vcc	VEE	3	Vcc	V	NOTERED NO DESERTE
T _{amb}	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC
T _{amb}	operating ambient temperature range	-40	- 000	+125	-40		+125	°C	CHARACTERISTICS
t _r , t _f	input rise and fall times 42 084		6.0	1000 500 400	0 14 5 12	6.0	500	ns	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V
HIV 33V				250	10				V _{CC} = 10.0 V

V_{CC}-GND

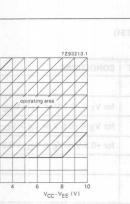


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4052.

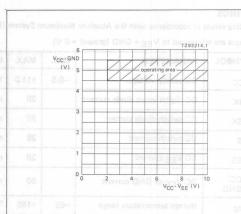


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4052.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: $V_{CC} - \text{GND}$ or $V_{CC} - V_{EE}$ =2.0, 4.5, 6.0 and 9.0 V For 74HCT: $V_{CC} - \text{GND}$ =4.5 and 5.5 V; $V_{CC} - V_{EE}$ =2.0, 4.5, 6.0 and 9.0 V

	100 Aew Zu pus UAu		53 (Q V - 9			T _{amb} (°C)			t timit o	a si sa	TEST	COND	ITION	S
SYMBOL	PARAMETER		74HC/HCT								Vcc	VEE	Is	Vis	VI
STWIBOL	PANAMETER		ТЭН	+25		-40 to +85		-40 t	o +125	UNIT	V	VEE	μA	Vis	VI
814	MITCONDITIO	gem	min.	typ.	max.	min.	max.	min.	max.			ASTE	MARA	10	âMY3
RON	ON resistance (peak)		0.6	100 90 70	180 160 130	or at	225 200 165		- 270 240 195	ΩΩΩ	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	V _{CC} to V _{EE}	V _{IN} or V _{IL}
RON	ON resistance (rail)	170 V 120 V		150 80 70 60	- 140 120 105	oV aV	- 175 150 130	VEI VEI	210 180 160	ΩΩΩ	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	VEE	VIH or VIL
RON	ON resistance (rail)		0.4	150 90 80 65	160 140 120	101	_ 200 175 150		240 210 180	ΩΩΩ	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	Vcc	V _{IH} or V _{IL}
ΔRON	maximum △ON resist: between any two ch			9 8 6		25				ΩΩΩ	2.0 4.5 6.0 4.5	0 0 0 -4.5		V _{CC} to V _{EE}	V _{IH} or V _{IL}

Notes to DC characteristics

- 1. At supply voltages ($V_{CC} V_{EE}$) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- 2. For test circuit measuring RON see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SNOT	TEST CONDIT			Т	amb (°C)				TEST CONDITIONS					
rud-ii	PARAMETER DOV TIMO				74H	3	LIBILT	.,	.,		OTHER				
SYMBOL		257+ +25			-40 to +85		-40 to +125		UNIT	V _{CC}	V _{EE}	VI	OTHER		
		min.	typ.	max.	min.	max.	min.	max.							
V _{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7	2	1.5 3.15 4.2 6.3	2	1.5 3.15 4.2 6.3	0.50	V	2.0 4.5 6.0 9.0	nt lev	il Həli	Hin		
VIL	LOW level input voltage	8.1	0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7	0	0.5 1.35 1.8 2.7	.2 0	0.5 1.35 1.8 2.7	V 301	2.0 4.5 6.0 9.0	gni la	el WQ.	JIV		
±I _I	input leakage current	0.		0.1 0.2		1.0		1.0 2.0	μΑ	6.0	0	VCC or GND			
±IS	analog switch OFF-state current per channel			0.1		1.0		1.0	μА		0	V _{IH} or V _{IL}	IV _S I = V _{CC} - V _{EE} (see Fig. 10)		
±IS	analog switch OFF-state current all channels			0.2		2.0		2.0	μΑ	10.0	0	V _{IH} or V _{IL}	V _S I = V _{CC} - V _{EE} (see Fig. 10)		
±IS	analog switch ON-state current	2.1		0.2		2.0		2.0	μА	10.0	0	V _{IH} or V _{IL}	IV _S I = V _{CC} - V _{EE} (see Fig. 11)		
Icc	quiescent supply current	20.0		8.0 16.0		80.0 160.0	i i	160.0 320.0	μΑ	6.0	0	V _{CC} or GND	V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}		

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

	.woled side	Forth r	T _{amb} (°C)								TEST CONDITIONS				
0.44001					74H				LINUT	V	v_ 0	OTHER			
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	VEE	OTHER			
		min.	typ.	max.	min.	max.	min.	max.				0.45 E			
tpHL/ tpLH	propagation delay V _{is} to V _{os}		14 5 4 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = ∞; C _L = 50 pF (see Fig. 18)			
tPZH/ tPZL	turn "ON" time E to V _{os} S _n to V _{os}		105 38 30 26	325 65 55 46		405 81 69 58		490 98 83 69	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = ∞; C _L = 50 pF (see Figs 19, 20 and 21)			
tPHZ/ tPLZ	turn "OFF" time E to Vos S _n to Vos		74 27 22 22	250 50 43 38		315 63 54 48		375 75 64 57	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 19, 20 and 21)			

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

	TEST CONDIT	T _{amb} (°C)								TEST CONDITIONS				
SYMBOL	PARAMETER	74НСТ									пота	S S CI A C	OTHER	
		+25			-40 to +85		-40 to +125		UNIT	V _{CC}	V _{EE}	VI	OTHER	
		min.	typ.	max.	min.	max.	min.	max.						
V _{IH}	HIGH level input voltage	2.0	1.6	0.4	2.0	- 848	2.0	1.5 3.15 4.2	V	4.5 to 5.5	păl la e	el HarH	HIV	
VIL	LOW level input voltage	36	1.2	0.8	0.1	0.8	8 0	0.8	V	4.5 to 5.5	qni im	el WOJ	ll V	
±II	input leakage current	0.1		0.1	2.	1.0	2.0	1.0	μΑ	5.5	0	V _{CC} or GND		
±IS = 2V	analog switch OFF-state current per channel	B.3		0.1	2.	1.0	10	1.0	μΑ	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} - V _{EE} (see Fig. 10)	
±IS	analog switch OFF-state current all channels	1		0.2		2.0		2.0	μА	10.0	0	V _{IH} or V _{IL}	V _S I = V _{CC} - V _{EE} (see Fig. 10)	
see Fig. 10) Vgl= 2l±	analog switch ON-state current			0.2		2.0		2.0	μΑ	10.0	0	VIH or VIL	V _S I = V _{CC} - V _{EE} (see Fig. 11)	
Icc V = alv	quiescent supply current	0.031		8.0 16.0	38	80.0 160.0	2	160.0 320.0	μΑ	5.5 5.0	0 -5.0	V _{CC} or GND	V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}	
ΔICC	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)	U.S.	100	360		450		490	μА	4.5 to 5.5	0	V _{CC} -2.1V	other inputs at V _{CC} or GND	

Note to HCT types

The value of additional quiescent supply current (\(\Delta\Lambda\CC\)) for a unit load of 1 is given here.
 To determine \(\Delta\Lambda\CC\) per input, multiply this value by the unit load coefficient shown in the table below.

	UNIT LOA	D]					
INPUT	COEFFICIENT		99\ V					
S _n E	0.45 0.45							
30 pF	R[= m; C] = (see Fig. 18)							

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	PARAMETER	T _{amb} (°C)								TEST CONDITIONS		
SYMBOL										V	V	OTHER
		+25			-40 to +85		-40 to +125		UNIT	VCC	V	OTHER
		min.	typ.	max.	min.	max.	min.	max.			3	HAT = 1
t _{PHL} /	propagation delay V _{is} to V _{os}	4.0 8.0	5 4	12 8	25	15 10	8	18 12	ns	4.5 4.5		R _L = ∞; C _L = 50 pF (see Fig. 18)
t _{PZH} /	turn "ON" time E to V _{os} S _n to V _{os}	Ron	41 28	70 48	25 2.	88 60	8b 8b	105 72	ns	4.5 4.5	0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 19, 20 and 21)
t _{PHZ} /	turn "OFF" time E to V _{os} S _n to V _{os}	note	26 21	50 38	8s. 8.	63 48	8h 8h	75 57	ns	4.5 4.5	0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 19, 20 and 21)

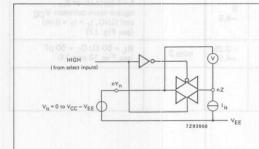


Fig. 8 Test circuit for measuring RON.

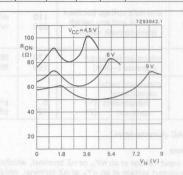
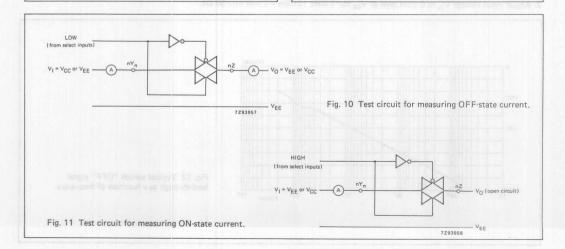


Fig. 9 Typical RON as a function of input voltage $V_{\dot{I}\dot{S}}$ for $V_{\dot{I}\dot{S}}$ = 0 to VCC $^-$ VEE.



ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

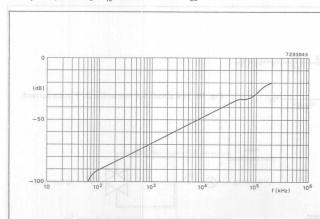
SYMBOL	PARAMETER	typ.	UNIT	VCC	V _{EE}	Vis(p-p)	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10 \text{ k}\Omega; C_L = 50 \text{ pF}$ (see Fig. 14)
7g 03 =	sine-wave distortion f = 10 kHz	0.12	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10 \text{ k}\Omega; C_L = 50 \text{ pF}$ (see Fig. 14)
Ot = 50 pl 1, 20 and 21	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600 \Omega$; $C_L = 50 pF$; f = 1 MHz (see Figs 12 and 15)
	crosstalk between any two switches/ multiplexers	-60 -60	dB dB	2.25 4.5	-2.25 -4.5	note 1	R _L = 600 Ω; C _L = 50 pF; f = 1 MHz (see Fig. 16)
V _(p-p)	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5		R _L = 600Ω ; C _L = 50 pF ; f = 1 MHz (E or S _D , square-wave between V _{CC} and GND, t _r = t_f = 6 ns) (see Fig. 17)
f _{max}	minimum frequency response (–3dB)	170 180	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	$R_L = 50 \Omega$; $C_L = 50 pF$ (see Figs 13 and 14)
CS	maximum switch capacitance independent (Y) common (Z)	5 12	pF pF				eva

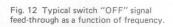
Notes to AC characteristics

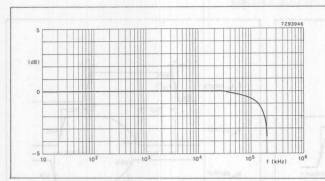
General note

 V_{is} is the input voltage at an nY_n or nZ terminal, whichever is assigned as an input. V_{os} is the output voltage at an nY_n or nZ terminal, whichever is assigned as an output.

- 1. Adjust input voltage V_{is} to 0 dEm level (0 dBm = 1 mW into 600 Ω).
 2. Adjust input voltage V_{is} to 0 dEm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).







Note to Figs 12 and 13

Test conditions: V_{CC} = 4.5 V; GND = 0 V; V_{EE} = -4.5 V; R_L = 50 Ω ; R_{source} = 1 k Ω .

Fig. 13 Typical frequency response.

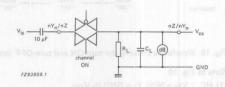


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

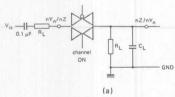
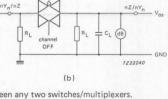


Fig. 16 Test circuits for measuring crosstalk between any two switches/multiplexers. (a) channel ON condition; (b) channel OFF condition.



 $\begin{array}{c|c} V_{CC} & S_n \text{ or } \overline{\mathbb{E}} \\ \hline \\ 2R_L & DUT \\ \hline \\ 2R_L & C_L \\ \hline \\ 2R_L & C_L \\ \hline \\ 7293962.2 \\ \end{array}$

Fig. 17 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 17

The crosstalk is defined as follows (oscilloscope output):

AC WAVEFORMS

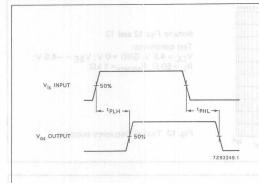


Fig. 18 Waveforms showing the input (V $_{is})$ to output (V $_{os})$ propagation delays.

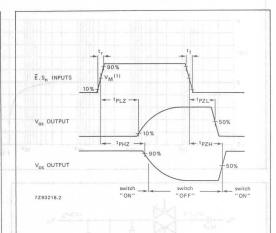
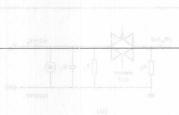


Fig. 19 Waveforms showing the turn-ON and turn-OFF times.

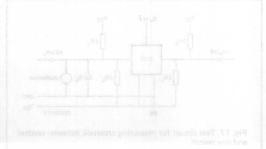
Note to Fig. 19

(1) HC :
$$V_M = 50\%$$
; $V_I = GND$ to V_{CC} .
HCT: $V_M = 1.3$ V; $V_I = GND$ to 3 V.



ie. 16 Test circuits for measuring crossfelk between any two switches/additionars.
 channel ON condition; (b) channel OFF condition.





TEST CIRCUIT AND WAVEFORMS

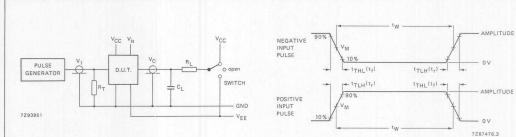


Fig. 20 Test circuit for measuring AC performance.

Fig. 21 Input pulse definitions.

Conditions

TEST	SWITCH	Vis
tPZH	VEE	VCC
tPZL	VCC	VEE
tPHZ	VEE	VCC
tPLZ	VCC	VEE
others	open	pulse

Definitions	for	Figs	20	and	21:	

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

 R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

 $t_r = t_f = 6$ ns; when measuring f_{max} , there is no constraint to t_r , t_f with 50% duty factor.

FAMILY AME			t _r ; t _f					
	AMPLITUDE	V _M	f _{max} ; PULSE WIDTH	OTHER				
74HC	Vcc	50%	< 2 ns	6 ns				
74HCT	3.0 V	1.3 V	< 2 ns	6 ns				

TEST CIRCUIT AND WAVEFORMS

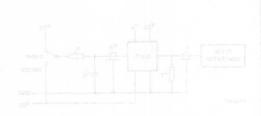
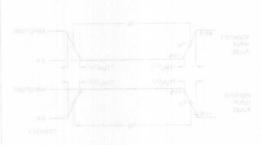


Fig. 20 Test curcuit for measuring AC performance



iq. 2) I traver surse definitions.

Conditions



Definitions for Pins 20 and 21.

- Or = load capacitance including jig and probe depectance (see AC CHARACTERISTICS for
- Fig. 4: reimination resistance should be equal to the output impedance Z_O of the pulse generator.
- f_f = t_f = 6 ns; when measuring f_{max}, there is no constraint to t_f, t_f with 90% duty factor.

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- Low "ON" resistance: 80 Ω (typ.) at V_{CC} V_{EE} = 4.5 V 70 Ω (typ.) at V_{CC} V_{EE} = 6.0 V 60 Ω (typ.) at V_{CC} V_{EE} = 9.0 V
- Logic level translation: to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4053 are high-speed Si-gate CMOS devices and are pin compatible with the "4053" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4053 are triple 2-channel analog multiplexers/demultiplexers with a common enable input (\overline{E}). Each multiplexer/demultiplexer has two independent inputs/outputs (nY₀ and nY₁), a common input/output (nZ) and three digital select inputs (S₁ to S₃).

With \overline{E} LOW, one of the two switches is selected (low impedance ON-state) by S₁ to S₃. With \overline{E} HIGH, all switches are in the high impedance OFF-state, independent of S₁ to S₃.

 V_{CC} and GND are the supply voltage pins for the digital control inputs (S1 to S3, and E). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY0 and nY1, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC}-V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

CVMPOL	DADAMETED	CONDITIONS	TYF	N DES	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
^t PZH [/]	turn "ON" time E to V _{os} S _n to V _{os}	CL = 15 pF	17 21	23 21	ns a s
tpHZ/ tPLZ turn "OFF" time E to Vos S _n to Vos		$\begin{array}{c} R_L = 1 \text{ k}\Omega \\ V_{CC} = 5 \text{ V} \end{array}$	18 17	20 19	ns ns
CI	input capacitance	aqubni y Y	3.5	3.5	pF S1
C _{PD}	power dissipation capacitance per switch	notes 1 and 2	36	36	pF
CS	max. switch capacitance independent (Y) common (Z)		5 8	5 8	pF pF

$$V_{EE} = GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$$
 where:

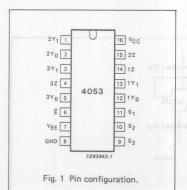
$$f_i$$
 = input frequency in MHz C_L = output load capacitance in pF

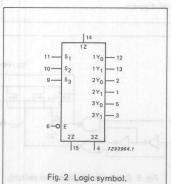
$$f_0$$
 = output frequency in MHz C_S^c = max. switch capacitance in pF $\Sigma \{(C_L + C_S) \times V_{CC}^2 \times f_0\}$ = sum of outputs V_{CC} = supply voltage in V

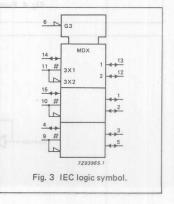
2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} - 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z). 16-lead mini-pack; plastic (SO16; SOT109A).

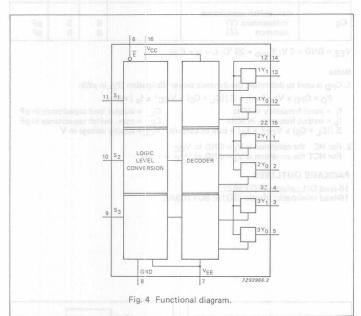






PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	7 GRIMAS
2, 1 5, 3 88 68 6	0.0,0	independent inputs/outputs independent inputs/outputs enable input (active LOW)	
7 8 11, 10, 9	VEE GND S ₁ to S ₃	negative supply voltage ground (0 V) select inputs	
12, 13	1Y ₀ , 1Y ₁	independent inputs/outputs	
14, 15, 4 16	1Z to 3Z VCC	common inputs/outputs positive supply voltage	



- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating Shot V d sides of the sid

FUNCTION TABLE

INF	PUTS	CHANNEL
E alla	S _n	ON
L ow Lne o	Bar Laxais	$ \begin{array}{r} \text{nY}_0 - \text{nZ} \\ \text{nY}_1 - \text{nZ} \end{array} $
H S	×	none

H = HIGH voltage level L = LOW voltage level

X = don't care

V_{CC} → V_{EE}

from logic

Fig. 5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to VEE = GND (ground = 0 V)

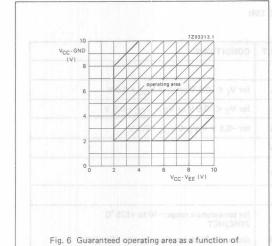
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
Vcc	DC supply voltage	-0.5	+11.0	V	
±IIK	DC digital input diode current		20	mA	for $V_1 < -0.5 \text{ V}$ or $V_1 > V_{CC} + 0.5 \text{ V}$
±1SK	DC switch diode current		20	mA	for V_S < -0.5 V or V_S > V_{CC} + 0.5 V
±IS	DC switch current		25	mA	for -0.5 V < V _S < V _{CC} + 0.5 V
±1EE	DC V _{EE} current		20	mA	
±I _{CC} ; ±I _{GND}	DC V _{CC} or GND current		50	mA	at 8 8 9 2 00
T _{stg}	storage temperature range	-65	+150	°C	
P _{tot}	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL priterago bestosta	ig. T G	750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)	ades a	500	mW	above +70 °C: derate linearly with 8 mW/K
PS	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminals nZ, when switch current flows in terminals nY_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ, no V_{CC} current will flow out of verminals nY_n. In this case there is no limit for the voltage drop across the switch, but the voltages at nY_n and nZ may not exceed V_{CC} or V_{EE} .

RECOMMENDED OPERATING CONDITIONS

OVIMBOL	125 V V 1pA	40 to +1		74HC			74HC1		LIMIT	CONDITIONS	
SYMBOL	PARAMETER	mi	in. typ.		max.	min.	typ.	max.	UNIT	CONDITIONS	
Vcc so	DC supply voltage V _{CC} -GND	2.0		5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7	
VCC	DC supply voltage V _{CC} -V _{EE}	2.0)	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7	
V _I	DC input voltage range	GN	ID		Vcc	GND	9	Vcc	V		
V _S	DC switch voltage range	VE	E	175	VCC	VEE	8	Vcc	V(list) e	onstelan VO Mesistani	
T _{amb}	operating ambient temperature rang	ge -4	0		+85	-40	18	+85	°C	see DC and AC	
T _{amb}	operating ambient temperature rang	ge -4	0	200	+125	-40	18	+125	°C	CHARACTERISTICS	
t _r , t _f	input rise and fall times			6.0	1000 500 400 250	120	6.0	500	ns	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V V _{CC} = 10.0 V	



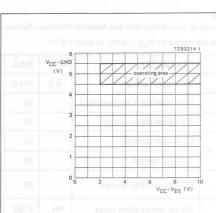


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4053.

DC CHARACTERISTICS FOR 74HC/HCT

the supply voltages for 74HC4053.

For 74HC: V_{CC} – GND or V_{CC} – V_{EE} = 2.0, 4.5, 6.0 and 9.0 V For 74HCT: V_{CC} – GND = 4.5 and 5.5 V; V_{CC} – V_{EE} = 2.0, 4.5, 6.0 and 9.0 V

						T _{amb} (°C)		TEST CONDITIONS						
0.445.01					7	4HC/F	ICT	UNIT	awn	V _{EE}	I _S μA	Vis	10005		
SYMBOL	PARAMETER		TON	+25		-40 to +85		-40 to +125					UNIT	V _{CC}	VI
-	torranos TINU		min.	typ.	max.	min.	max.	min.	max.			RETER	MARAS	100	BWAS
	ns 8 api R sea V	die	0	100	180	0.01	- 225	2.0	_ 270	Ω	2.0	0	100	Vcc	VIH
RON ON resistance (pe	ON resistance (peak)	0.01	0	90	160 130	0.07	200 165	2.0	240 195	Ω	6.0	0 -4.5	1000 1000	VEE	or V _{IL}
		001		150	10	DOV I	_	GND	_	Ω	2.0	0	100		VIH
RON	ON resistance (rail)			80 70	140 120	NOV	175 150	asV .	210 180	Ω	4.5 6.0	0	1000	VEE	or
	3"	384		60	105	201	130	Oliv.	160	Ω	4.5	-4.5	1000		VIL
	ON resistance (rail)	a\$1-		150 90	160	12	200	04-	_ 240	Ω	2.0 4.5	0	100 1000	Vcc	VIH
RON	/ OA = goV			80 65	140 120	1001	175 150		210 180	Ω	6.0 4.5	0 -4.5	1000	• ((VIL
	maximum ∆ON resista	ance		9		40D 230				Ω	2.0 4.5	0		Vcc	VIH
	between any two cha	annels		8						Ω	6.0 4.5	0 -4.5		VEE	or V _{IL}

Notes to DC characteristics

- At supply voltages (V_{CC} V_{EE}) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
 For test circuit measuring R_{ON} see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

	TIGUED TREET				T _{amb} (°C)					TEST	COND	ITIONS
OVIMBOL	BARAMETER				74H	at .		UNIT	V		V	OTHER	
SYMBOL	PARAMETER	+25			-40 t	-40 to +85		-40 to +125		VCC	VEE	VI	OTHER
		min.	typ.	max.	min.	max.	min.	max.					
V _{IH} 3000	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3	81 8	V	2.0 4.5 6.0 9.0	1	repkqo:	e /1Hd ₂
t kΩ; 50 pF JIV igs 19,	LOW level input voltage	30	0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7	27 35 42	0.5 1.35 1.8 2.7	228 44 37	0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0	mir "l	A ear g	7.2dg
±I ₁ (Ωx) t 50 pF II±	input leakage current	Ø8 8	8	0.1 0.2	278	1.0	221	1.0	μА	6.0 10.0	0	V _{CC} or GND	o \u00e4
±IS	analog switch OFF-state current per channel	a	A C	0.1	38	1.0	210	1.0	μΑ	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} - V _{EE} (see Fig. 10)
±Is RI SI	analog switch OFF-state current all channels	100 100	8	0.1	45	1.0	36 29	1.0	μА	10.0	0	V _{IH} or V _{IL}	IV _S I = V _{CC} - V _{EE} (see Fig. 10)
±I _S (15 b	analog switch ON-state current	0.00	6 6 8	0.1	83	1.0	42 26 26 29	1.0	μΑ	10.0	0	V _{IH} or V _{IL}	IV _S I = V _{CC} - V _{EE} (see Fig. 11)
^I CC	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μА	6.0 10.0	0	V _{CC} or GND	V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	TOUNOU TRAT				T _{amb} (°C)					TEST C	ONDITIONS
CVMDOL	DADAMETED ON THE	u L			74H0	:	LINUT	.,	G, 344	OTHER OSMYS		
SYMBOL PAR	PARAMETER	6	+25	Q8- 1	-40 t	o +85	-40 to +125		UNIT	V _{CC}	VEE	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay V _{is} to V _{os}	Į.	15 5 4 4	60 12 10 8	To the second	75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = ∞; C _L = 50 pF (see Fig. 18)
t _{PZH} / t _{PZL}	turn "ON" time of E to Vos	Į ši	60 20 16 15	220 44 37 31	1.2	275 55 47 39	1.2	330 66 56 47	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 \text{ k}\Omega;$ $C_L = 50 \text{ pF}$ (see Figs 19, 20 and 21)
tPZH/	turn "ON" time S _n to V _{os}		75 25 20 15	220 44 37 31	2.0	275 55 47 39	5.0	330 66 56 47	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 \text{ k}\Omega;$ $C_L = 50 \text{ pF}$ (see Figs 19, 20 and 21)
^t PHZ [/] ^t PLZ	turn "OFF" time E to V _{OS}		63 21 17 15	210 42 36 29	o.r	265 53 45 36	1.0	315 63 54 44	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Figs 19, 20 and 21)
t _{PHZ} /	turn "OFF" time S _n to V _{os}	4 1	60 20 16 15	210 42 36 29	0.1	265 53 45 36	1,0	315 63 54 44	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 19, 20 and 21)

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

	TEST CONDIT				T _{amb} (°C)				TEST CONDITIONS			
		74HCT							.,	.,	.,	OTHER	
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	VEE	VI	OTHER
		min.	typ.	max.	min.	max.	min.	max.		4.5 to 5.5			
V _{IH} 3,205	HIGH level input voltage		1.6		2.0		2.0		V		lab no	DEQECO	e UHE
VIL TO BE	LOW level input voltage		1.2	0.8	60	0.8	42	0.8	V	4.5 to 5.5	mit ")	sor m	0 VH29
1 (21) 1 (42) ± 10 (6)	input leakage current			0.1	ea	1.0	ijik	1.0	μΑ	5.5	0	V _C C or GND	
±1s (12.1)	analog switch OFF-state current per channel		18	0.1	43	1.0	34.	1.0	μΑ	10.0	0	VIH or VIL	V _S = V _{CC} - V _{EE} (see Fig. 10)
±IS	analog switch OFF-state current all channels		10	0.1	39	1.0	16	1.0	μΑ	10.0	0	VIH or VIL	V _S I= V _{CC} - V _{EE} (see Fig. 10)
±Is CI and	analog switch ON-state current		13 TA	0.1	55	1.0	44	1.0	μΑ	10.0	0 1	V _I H or V _I L	VS = VCC - VEE (see Fig. 11)
lcc	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μΑ	5.5 5.0	0 -5.0	V _{CC} or GND	V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}
ΔICC	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μΑ	4.5 to 5.5	0	V _{CC} -2.1 V	other inputs at VCC or GND

Note to HCT types

1. The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given here. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
S _n	0.50 0.50

AC CHARACTERISTICS FOR 74HCT GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

DC CHARACTERISTICS FOR 74HCT

	TEST CONDITI					T _{amb} (°C)					TEST C	ONDITIONS
0.44501	Chanadaran		74HCT					UNIT		V	OTHER		
SYMBOL	PARAMETER 30		a	+25	-40 t		0 to +85 -40		-40 to +125		VCC	VEE	OTHER OBMYS
			min.	typ.	max.	min.	max.	min.	max.	2			
t _{PHL} /	propagation delay V _{is} to V _{os}		V	5 4	12		15 10		18 12	ns	4.5 4.5	0 -4.5	$R_L = \infty$; $C_L = 50 \text{ pF}$ (see Fig. 18)
t _{PZH} / t _{PZL}	turn "ON" time E to Vos		V	27 16	48 34	9,0	60 43	8.0	72 51	ns ^{SQ}	4.5 4.5	0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Figs 19, 20 and 21)
t _{PZH} /	turn "ON" time S _n to V _{OS}			25 16	48 34	1.0	60 43	1.0	72 51	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Figs 19, 20 and 21)
t _{PHZ} /	turn "OFF" time E to V _{os}		u 1	24 15	44 31	0.1	55 39	1.0	66 47	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Figs 19, 20 and 21)
tPHZ/	turn "OFF" time	A	4 3	22 15	44 31	0.1	55 39	1,0	66 47	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Figs 19, 20 and 21)
= e0 1:30		A	0,0	16		160		8,0		ins	pty curr	gus fre) dames

Note to HCT types

The value of additional quiescent supply current (ALCQ) for suriff load of T is given here.
 To determine of one input, multiply this value by the unit load coefficient shown in the table bylow.

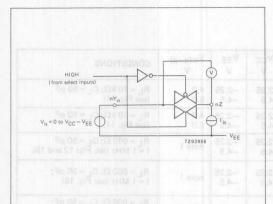


Fig. 8 Test circuit for measuring $R_{\mbox{\scriptsize ON}}$.

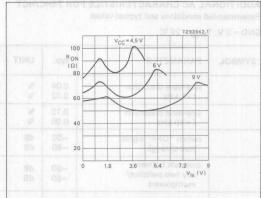
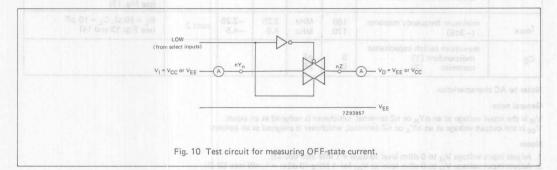
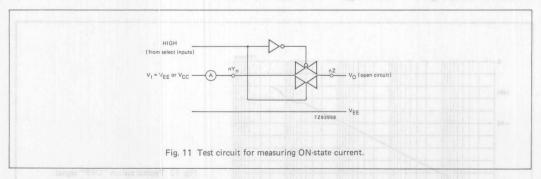


Fig. 9 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to V_{CC} - V_{EE} .





ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V _{CC}	V _{EE}	V _{is(p-p)}	CONDITIONS
	sine-wave distortion f =1 kHz	0.04 0.02	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_{L} = 10 \text{ k}\Omega$; $C_{L} = 50 \text{ pF}$ (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600 \Omega$; $C_L = 50 pF$ f = 1 MHz (see Figs 12 and 15)
	crosstalk between any two switches/ multiplexers	-60 -60	dB dB	2.25 4.5	-2.25 -4.5	note 1	R _L = 600 Ω; C _L = 50 pF; f = 1 MHz (see Fig. 16)
V _(p-p)	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5	10g gournes	R _L = 600Ω ; C _L = 50 pF ; f = 1 MHz (E or S _n , square-wave between V _{CC} and GND, t _r = t _f = 6 ns) (see Fig. 17)
f _{max}	minimum frequency response (-3dB)	160 170	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	$R_L = 50 \Omega$; $C_L = 10 pF$ (see Figs 13 and 14)
CS	maximum switch capacitance independent (Y) common (Z)	5	pF pF		440	Ankrytiil roetus e	

Notes to AC characteristics

General note

 V_{is} is the input voltage at an nY_n or nZ terminal, whichever is assigned as an input. V_{OS} is the output voltage at an nY_n or nZ terminal, whichever is assigned as an output.

- 1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω). 2. Adjust input voltage V_{is} to 0 dBm level at V_{OS} for 1 MHz (0 dBm = 1 mW into 50 Ω).

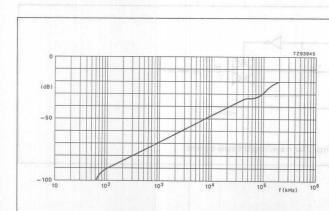
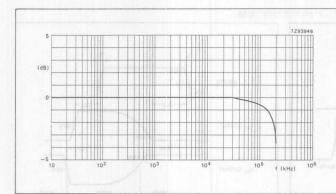


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions: $\begin{aligned} &\text{V}_{CC} = 4.5 \text{ V}; \text{GND} = 0 \text{ V}; \text{V}_{EE} = -4.5 \text{ V}; \\ &\text{R}_{L} = 50 \text{ } \Omega; \text{R}_{source} = 1 \text{ k} \Omega. \end{aligned}$

Fig. 13 Typical frequency response.

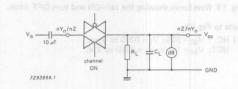


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

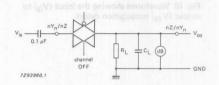


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

7222240

$$V_{is} \xrightarrow{nY_{in}/nZ} \xrightarrow{nZ/nY_{in}}$$

$$\begin{array}{c} nZ/nY_{in} \\ channel \\ ON \end{array}$$

$$(a)$$

Fig. 16 Test circuits for measuring crosstalk between any two switches/multiplexers. (a) channel OIV condition; (b) channel OFF condition.

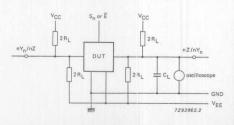


Fig. 17 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 17

(b)

OFF

The crosstalk is defined as follows (oscilloscope output):

AC WAVEFORMS

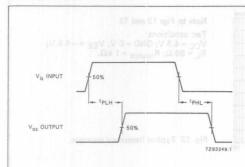


Fig. 18 Waveforms showing the input (V $_{is}$) to output (V $_{os}$) propagation delays.

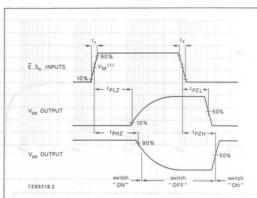


Fig. 19 Waveforms showing the turn-ON and turn-OFF times.

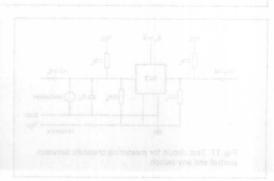
Note to Fig. 19

(1) HC :
$$V_M = 50\%$$
; $V_I = GND$ to V_{CC} .
HCT: $V_M = 1.3$ V; $V_I = GND$ to 3 V.

Fig. 14 Test circuit for measuring sine-wave discortion and minimum frequency response,

Fig. 16. Yest circuits for measuring creatally between any two switches/multiplexets.

a) whenever ON condition (b) channel OF F condition.



TEST CIRCUIT AND WAVEFORMS

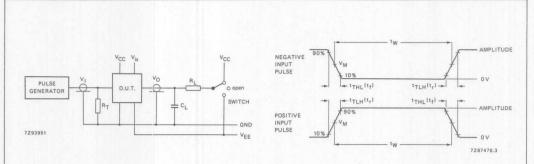


Fig. 20 Test circuit for measuring AC performance.

Fig. 21 Input pulse definitions.

Conditions

TEST	SWITCH	Vis
tPZH	VEE	VCC
tPZL	VCC	VEE
tPHZ	VEE	VCC
tPLZ	VCC	VEE
others	open	pulse

FAMILY			t _r ; t _f			
	AMPLITUDE	VM	f _{max} ; PULSE WIDTH	OTHER		
74HC 74HCT	V _{CC} 3.0 V	50% 1.3 V	< 2 ns	6 ns		

Definitions for Figs 20 and 21:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator,

 $t_r = t_f = 6$ ns; when measuring f_{max} , there is no constraint on t_r , t_f with 50% duty factor.

TEST CIRCUIT AND WAVEFORMS

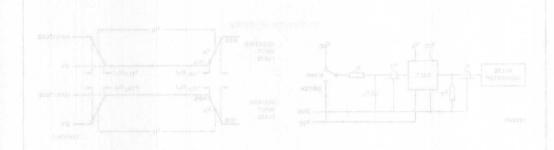


Fig. 20. Test struct the measuring AC destormance.

Fig. 21 Input pulse definitions

Conditions

Definitions for Figs 20 and 21:

- L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for column)
- Ry = terminal on resistance about the equal to the output impedance Zo of the pulse cenerators.
- t_r = t_f = 0 ns, when measuring t_{max}, there is no constraint on t_r, t_f with 50%, that t_f for t_f.

PROGRAMMABLE DIVIDE-BY-N COUNTER

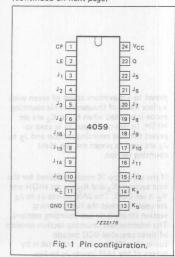
FEATURES

- Synchronous programmable divide-by-n counter
- Presettable down counter
- Fully static operation
- Mode select control of initial decade counting function (divide-by-10, 8, 5, 4 and 2)
- Master preset initialization
- Latchable output
- Easily cascadable with other counters
- Four operating modes: timer divide-by-n divide-by-10 000 master preset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4059 are high-speed Si-gate CMOS devices and are pin compatible with the "4059" of the "40008" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4059 are divide-by-n counters which can be programmed to divide an input frequency by any number (n) from 3 to 15 999. There are four operating modes, timer, divide-by-n, divide-by-10 000 and master preset, which are defined by the mode select inputs (K_a to K_c) and the latch enable input (LE) as shown in the Function table. (continued on next page)



SYMBOL		CONDITIONS	TYF	UNIT	
	PARAMETER WE AND FUNCTION	CONDITIONS	нс	нст	MIN N
tPHL/	propagation delay CP to Q	C _L = 15 pF V _{CC} = 5 V		20	ns
fmax	maximum clock frequency	100 00	40	40	MHz
CI	input capacitance	and and	3.5	3.5	pF
CPD power dissipation capacitance per package		notes 1 and 2	30	32	pF

GND = 0 V; Tamb = 25 °C; tr = tf = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD \times VCC² \times f_i + Σ (CL \times VCC² \times f₀) where:

fi = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 Σ (C_L × V_{CC}² × f₀) = sum of outputs

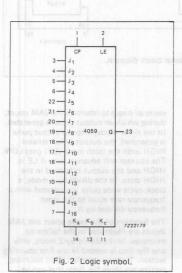
2. For HC the condition is V_I = GND to V_{CC}

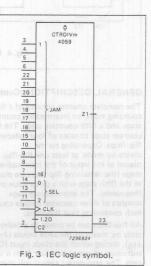
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

PACKAGE OUTLINES

24-lead DIL; plastic (SOT101A).

24-lead mini-pack; plastic (SO24; SOT137A).

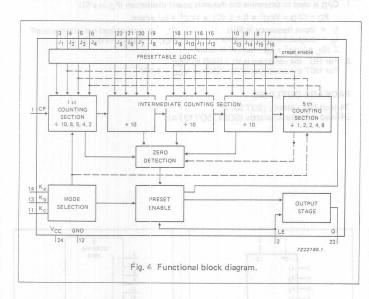




PROGRAMMABLE DIVIDE BY N COUNTER

PIN DESCRIPTION

PIN NO.	PIN NO. SYMBOL NAME AND FUNCTION							
1 20 05	CP LE	clock input (LOW-to-HIGH, edge-trig	gered)					
3, 4, 5, 6,	00	maximum clock frequency						
22, 21, 20, 19, 18, 17, 16, 15,	J ₁ to J ₁₆	programmable JAM inputs (BCD)						
10, 9, 8, 7 12	GND Some Season	ground (0 V) and construction						
14, 13, 11 23	K _a to K _c	mode select inputs divide-by-n output						
24	Vcc	positive supply voltage						



GENERAL DESCRIPTION (Cont'd)

The complete counter consists of a first counting stage, an intermediate counting stage and a fifth counting stage. The first counter stage consists of four independent flip-flops. Depending on the divide-by-mode, at least one flip-flop is placed at the input of the intermediate stage (the remaining flip-flops are placed at the fifth stage with a place value of thousands). The intermediate stage consists of three cascaded decade counters, each containing four flip-flops.

All flip-flops can be preset to a desired state by means of the JAM inputs (J $_1$ to J $_1$ 6), during which the clock input (CP) will cause all stages to count from ri to zero. The zero-detect circuit will then

cause all stages to return to the JAM count, during which an output pulse is generated. In the timer mode, after an output pulse is generated, the output pulse remains HIGH until the latch input (LE) goes LOW. The counter will advance, even if LE is HIGH and the output is latched in the HIGH state. In the divide-by-n mode, a clock cycle wide pulse is generated with a frequency rate equal to the input frequency divided by n.

The function of the mode select and JAM inputs are illustrated in the following examples. In the divide-by-2 mode, only one flip-flop is needed in the first counting section. Therefore the last (5th) counting section has three flip-flops that can be

APPLICATIONS

- Frequency synthesizer, ideally suited for use with PC74HC/HCT4046A and PC74HC/HCT7046A (PLLs)
- Fixed or programmable frequency division
- "Time out" timer

preset to a maximum count of seven with a place value of thousands. This counting mode is selected when K_a to K_c are set HIGH. In this case input J_1 is used to preset the first counting section and J_2 to J_4 are used to preset the last (5th) counting section.

If the divide-by-10 mode is desired for the first section, $\rm K_a$ and $\rm K_b$ are set HIGH and $\rm K_C$ is set LOW. The JAM inputs J₁ to J₄ are used to preset the first counting section (there is no last counting section consists of three cascaded BCD decade (divide-by-10) counters, presettable by means of the JAM inputs J₅ to J₁₆.

GENERAL DESCRIPTION

The preset of the counter to a desired divide-by-n is achieved as follows:

n = (MODE*) (1 000 x decade 5 preset

- + 100 x decade 4 preset
- + 10 x decade 3 preset
- + 1 x decade 2 preset)
- + decade 1 preset

* MODE = first counting section divider (10, 8, 5, 4 or 2).

To calculate preset values for any "n" count, divide the "n" count by the selected mode. The resultant is the corresponding preset value of the 5th to the 2nd decade with the remainder being equal to the 1st decade value; preset value = n/mode.

If n = 8 479, and the selected mode = 5, the preset value = 8 479/5 = 1 695 with a remainder of 4, thus the JAM inputs must be set as shown in Table 1.

To verify the results, use the given equation:

 $n = 5 (1000 \times 1 + 100 \times 6 + 10 \times 9)$ $+1 \times 5) + 4$

n = 8479.

If n = 12 382 and the selected mode = 8, the preset value = 12 382/8 = 1 547 with a remainder of 6, thus the JAM inputs must be set as shown in Table 2.

To verify:

n = 12 382.

If n = 8 479 and the selected mode = 10, the preset value = 8 479/10 with a remainder of 9, thus the JAM inputs must be set as shown in Table 3.

To verify:

$$n = 10 (1 000 \times 0 + 100 \times 8 + 10 \times 4 + 1 \times 7) + 9$$

n = 8479.

The three decades of the intermediate counting section can be preset to a binary 15 instead of a BCD 9. In this case the first cycle of a counter consists of 15 count pulses, the next cycles consisting of 10 counting pulses. Thus the place value of the three decades are still 1, 10 and 100. For example, in the divide-by-8 mode, the number from which the intermediate counting section begins to count-down can be preset to:

> 3rd decade: 1500 2nd decade: 150 15 1st decade:

The last counting section can be preset to a maximum of 1, with a place value of 1 000. The first counting section can be preset to a maximum of 7. To calculate n: $n = 8 (1 000 \times 1 + 100 \times 15 + 10 \times 15$

 $+1 \times 15) + 7$

n = 21 327.

(continued on next page)

FUNCTION TABLE

LATCH ENABLE INPUT	S	MODE SELECT INPUTS		FIR	SECTION DECADE	1	LA	ST COUNT SECTION DECADE	terraulii		INTER	OPERATION
clock pulse lode ingue f the count	Ka	K _b	Kc	MODE	MAX. PRESET STATE	JAM INPUTS USED	DIVIDE	MAX. PRESET STATE	JAM INPUTS USED	BCD MAX.	BINARY MAX.	The mode select inputs with decimal programm less significant digit. Fi
Hoff-qilf la	Н	Н	Н	2 101111	1	J ₁	8	7	J2J3J4	15 999	17 331	o of management to p
Highligheners	Lio	Н	H	4og bno	3	J ₁ J ₂	4 x bns	3	J3J4	15 999	18 663	in decimal steps of 100 into 8 steps of 125 kHz
mode, H	Н	L	Н	5	4	J ₁ J ₂ J ₃	2	1tool bus	J4	9 999	13 329	timer mode
Hustraulti	E		Н	8	7	J ₁ J ₂ J ₃	2 11000	rii au agoli	J ₄	15 999	21 327	20, 25 and 50 parts can
HE state 3H	Н	Н	L	10	9	J ₁ J ₂ J ₃ J ₄	1 m tanti	0	na l nuco	9 999	16 659	pode select inputs, This Fractional extension."
L	Н	Н	Н	2	1	J ₁ ban T	8 I mam	7 frod 5	J ₂ J ₃ J ₄	15 999	17 331	extension called "Half d
L	L	Н	Н	4	3	J ₁ J ₂	4	3	J ₃ J ₄	15 999	18 663	
L	Н	L	Н	5	4	J ₁ J ₂ J ₃	2	1	J4	9 999	13 329	
L	L	L	Н	8	7	J ₁ J ₂ J ₃	2	1	J4	15 999	21 327	divide-by-n mode
L	Н	Н	L	10	9	J ₁ J ₂ J ₃ J ₄	1	0	-	9 999	16 659	
Н	L	Н	L	10	9	J ₁ J ₂ J ₃ J ₄	1	0	- 1	9 999	16 659	
L	L	Н	L	р	reset inhib	ited	pı	eset inhibit	ted	fixed 10 000	-	divide-by-10 000 mode
X	X	L	L		master pre	set	r	naster prese	et	ATLAN A		master preset mode

Where:

H = HIGH voltage level

L = LOW voltage level

X = don't care

It is recommended that the device is in the master preset mode ($K_b = K_c = logic 0$) in order to correctly initialize the device prior to start-up. An example of a suitable external circuit is shown in Fig. 14.

Table 1

	1 1 noitee 5				5	nugo 9						4 + (6) + 4				
J ₁	J ₂	J3	J4	J ₅	J ₆	J7	Jg	Jg	J ₁₀	J11	J ₁₂	J ₁₃	J ₁₄	J ₁₅	J ₁₆	
L	L	Н	Н	Н	L	Н	L	Н	L	L	Н	L	Н	Н	L	

Table 2

	6		1	d no	mon.	7				4				5	7.500.1
J ₁	J ₂	J3	J4	J ₅	J ₆	J-7	J8	Jg	J ₁₀	J ₁₁	J ₁₂	J ₁₃	J ₁₄	J ₁₅	J ₁₆
L	Н	Н	Н	Н	Н	Н	L	L	L	Н	L	Н	L	Н	L

Table 3

9				61,11 80,32	o m.	7	10 T			4		be set as 8 own in Tab				
J ₁	J ₂	J ₃	J4	J ₅	J ₆	J7	J8	J9	J ₁₀	J ₁₁	J ₁₂	J ₁₃	J ₁₄	J ₁₅	J ₁₆	
Н	L	L	Н	Н	Н	Н	L	L	L	Н	L	L	(L-	L	Н	

GENERAL DESCRIPTION (Cont'd)

21 327 is the maximum possible count in the divide-by-8 mode. The highest count of the various modes is shown in the Function table, in the column entitled "binary counter range".

The mode select inputs permit, when used with decimal programming, a non-BCD least significant digit. For example, the channel spacing in a radio is 12.5 kHz, it may be convenient to program the counter in decimal steps of 100 kHz subclivided into 8 steps of 12.5 kHz controlled by the least significant digit. Also frequency synthesizer channel separations of 10, 12.5, 20, 25 and 50 parts can be chosen by the mode select inputs. This is called "Fractional extension". A similar extension called "Half channel offset" can

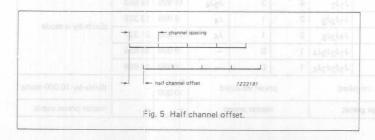
be obtained in modes 2, 4, 6 and 8, if the JAM inputs are switched between zero and 1, 2, 3 and 4 respectfully. This is illustrated in Fig. 5.

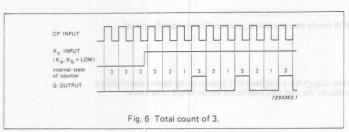
This features is used primarily is cases where radio channels are allocated according to the following formula: Channel frequency = channel spacing x (N + 0.5)

N is an integer.

Control inputs K_b and K_c can be used to initiate and lock the counter in the "master preset" mode. In this condition the flip-flops in the counter are preset in accordance with the JAM inputs and the counter remains in that mode as long as K_b and K_c both remain LOW. The counter

begins to count down from the preset state when a counting mode other than the "master preset" mode is selected. Whenever the "master preset" mode is used, control signals $K_b = K_c = LOW$ must be applied for at least 2 full clock pulses. After the "master preset" mode inputs have been changed to one of the counting modes, the next positive-going clock transition changes an internal flip-flop so that the count-down begins on the second positive-going clock transition. Thus, after a "master preset" mode, there is always one extra count before the output goes HIGH. Figure 6 illustrates the operation of the counter in the divide-by-8 mode starting from the preset state 3.





If the "master preset" mode is started two clock cycles or less before an output pulse, the output pulse will appear at the correct moment. When the output pulse appears and the "master preset" mode is not selected, the counter is preset according to the states of the JAM inputs.

When K_a , K_b , K_c and LE are LOW, the counter operates in the "preset inhibit" mode, during which the counter divides at a fixed rate of 10 000, independent of the state of the JAM inputs. However, the

first cycle length after leaving the "master preset" mode is determined by the JAM inputs.

When K_a , K_b and K_c are LOW and input LE = HIGH, the counter operates in the normal divide-by-10 mode, however, without the latch operation at the output.

This device is particularly advantageous in digital frequency synthesizer circuits (VHF, UHF, FM, AM etc.) for communication systems, where programmable divide-by-"n" counters are an integral part of the

synthesizer phase-locked-loop sub-system. The 74HC/HCT4059 can also be used to perform the synthesizer "fixed divide-by-n" counting function, as well as general purpose counting for instrumentation functions such as totalizers, production counters and "time out" timers.

Schmitt-trigger action at the clock input makes the circuit highly tolerant to slower clock rise and fall times.

DC CHARACTERISTIC FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

	8 913 84	EN E			r _{amb} (°C)	ab 1	\$		yelel	TEST CONDITIONS
0.44001					74H	С				.,	WAVEFORMS
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	VCC V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		idun	clock gulsa v
tPHL/	propagation delay CP to Q	in .	58 21 17	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 7
tPHL/	propagation delay LE to Q	M	50 18 14	175 35 30		220 44 37	Ġ	265 53 45	ns	2.0 4.5 6.0	Fig. 8
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
tw	clock pulse width CP	90 18 15	7 6 5		115 23 90		135 27 23		ns	2.0 4.5 6.0	Fig. 7
^t rem	removal time K _b , K _c to CP	75 15 13	19 7 6		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 9; note 1
f _{max}	maximum clock pulse frequency	4.2 21 25	12 36 43		3.4 17 20		2.8 14 17		MHz	2.0 4.5 6.0	Fig. 7

Note to the characteristic table

1. From master preset mode to any other mode.

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
CP	0.65
LE	0.65
Jn bivib	0.50
Ka	
Kh	
Kc	0.05

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_1 = 50 \text{ pF}$

		10 p	Aq-api	vib alde	amb (°C)	dw aen Ne dien	anes a		TEST CONDITIONS			
01/44001					74HC	Т			UNIT	FOR. 7	WAVEFORMS		
SYMBOL	PARAMETER	0868 V	+25	noins	-40	to +85	-40 t	o +125	UNIT	V _{CC}	the DC chemic shades		
		min.	typ.	max.	min.	max.	min.	max.			C category: WS1		
tPHL/ tPLH	propagation delay CP to Q		24	46		58		69	ns	4.5	Fig. 7 _{+7 = -1 1} V 0 = OM		
t _{PHL} /MO	propagation delay LE to Q		24	46	(3°) 6	58		69	ns	4.5	Fig. 8		
t _{THL} /	output transition time	125	7	15	3150 - 02 00	19	26	22	ns	4.5	Fig. 7. BA9 JOBNYS		
tw	clock pulse width CP	20	7	(f) (d)	25	m .xi	30	et .cite	ns	4.5	Fig. 7		
^t rem	removal time K _b , K _c to CP	15	7	1 0	9	0	22	8	ns	4.5	Fig. 9; note 1		
f _{max}	maximum clock pulse frequency	21	36	D	17	9	14	8	MHz	4.5	Fig. 7		

Note to the characteristic table

1. From master preset mode to any other mode.

AC WAVEFORMS

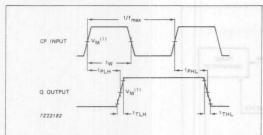
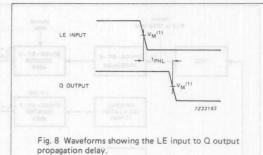


Fig. 7 Waveforms showing the clock (CP) to output (Q) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.



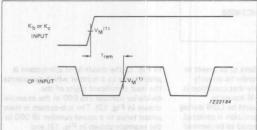


Fig. 9 Waveforms showing the $\rm K_b$ or $\rm K_c$ removal times, when the operating mode is switched from master preset to any other mode.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3$ V; $V_I = GND$ to 3 V.

APPLICATION INFORMATION

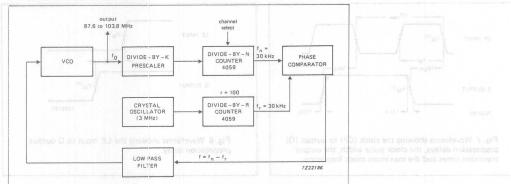


Fig. 10 Example showing the application of the PC74HC/HCT4059 in a phase-locked-loop (PL) for a FM band synthesizer.

Calculating the minimum and maximum divide-by-n values:

Output frequency range = 87.6 to 103.8 MHz (CCIR band 2)

Channel spacing frequency (f_c) = 300 kHz Division factor prescaler (k) = 10

Reference frequency (fr) =

$$\frac{f_c}{k} = \frac{300}{10} = 30 \text{ kHz}$$

Maximum divide-by-n value =

$$\frac{103.8 \text{ MHz}}{300 \text{ kHz}} = 346$$

Minimum divide-by-n value =

$$\frac{87.6 \text{ MHz}}{300 \text{ kHz}} = 292$$

Fixed divide-by-n value = $\frac{3 \text{ MHz}}{30 \text{ kHz}}$ = 100

Application of the "4059" as divide-by-n counter allows programming of the channel spacing (shown in equations as 300 kHz). A channel in the CCIR band 2 is selected by the divide-by-n counter as follows:

Figure 11 shows a BCD switch compatible arrangement suitable for divide-by-5 and divide-by-8 modes, which can be adapted (with minimal changes) to the other divide-by-modes. In order to be able to preset to any number from 3 to 256 000, while preserving the BCD switch compatible character of the JAM inputs, a rather complex cascading scheme is necessary because the "4059" can never be preset to count less than 3. Logic circuitry is required to detect a condition

where one of the numbers to be preset in the "4059" is < 3. In order to simplify the detection logic, only that condition is detected where the JAM inputs to terminals 6, 7 and 9 would be LOW during one count. If such a condition is detected, and if at least 1 is expected to be jammed into the MSB counter, the detection logic removes one from the number to be jammed into the MSB counter (with a place value of 2 000 times the divide-by-mode) and jams the same 2 000 into the "4059" by forcing pins 6, 7 and 9 HIGH

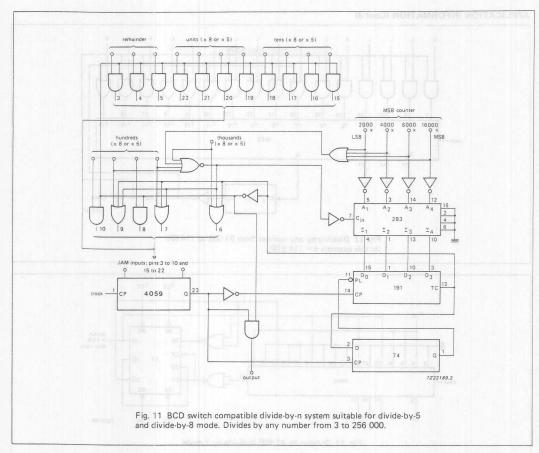
The general circuit in Fig. 11 can be simplified considerably if the range of the cascaded counters do not start at a very low value.

Figure 12 shows an arrangement in the divide-by-4 mode, where the counting range extends in a BCD switch compatible manner from 99 003 to 114 999. The arrangement shown in Fig. 12 is easy to follow; once during every cycle the programmed digits are jammed in (15 616 in this example) and then a round number of 11 000 is jammed in, nine times in succession, by forcing the JAM inputs via AND/OR gates.

Numbers larger than the extended counter range can also be produced by cascading the PC74HC/HCT4059 with some other counting devices. Figure 13 shows such an arrangement where only one fixed divide-by number is desired. The dual flip-flop wired to produce a divide-by-3 count can be replaced by other counters such as the "190", "191", "192", "193", "4017", "4510" and "4516".

In Fig. 13 the divide-by-n sub-system is preset once to a number which represents the least significant digits of the divide-by number (15 690 in the example shown in Fig. 13). The sub-system is then preset twice to a round number (8 000 in the example shown in Fig. 13) and multiplied by the number of the divide-by mode (2 in the example shown in Fig. 13).

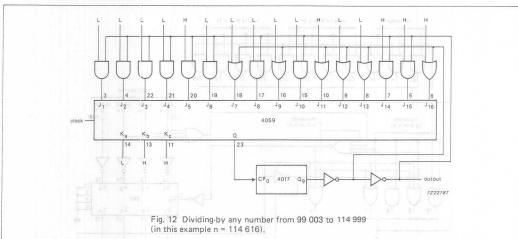
It is important that the second counting device has an output that is HIGH or LOW during only one of its counting states.

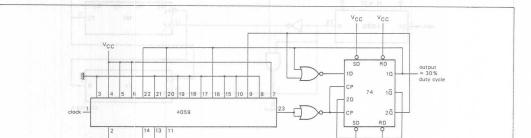


Note to Fig. 11

Each AND gate is 1/4 of PC74HC/HCT08. Each OR gate is 1/3 of PC74HC/HCT4075. Each NOR gate is 1/2 of PC74HC/HCT4002. Each inverter is 1/6 of PC74HC/HCT04.

APPLICATION INFORMATION (Cont'd)





e d'vcc

7222188

Fig. 13 Division by 47 690 in divide-by-2 mode.

-Vcc mazeya n-yd-sklylb eldirecmos

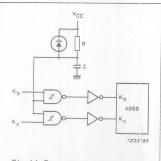


Fig. 14 External circuit for master preset at start-up.

Notes to Fig. 14

- 1. RC $\geqslant \frac{1}{0.2 \times f_{CP} (Hz)}$
- It is assumed that the f_{CP} starts directly after the power-on. Any additional delay in starting f_{CP} must be added to the RC time.

14-STAGE BINARY RIPPLE COUNTER WITH OSCILLATOR

FEATURES

- All active components on chip
- RC or crystal oscillator
- configuration
- Output capability: standard (except for R_{TC} and C_{TC})
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4060 are high-speed Si-gate CMOS devices and are pin compatible with "4060" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4060 are 14-stage ripple-carry counter/dividers and oscillators with three oscillator terminals (RS, R $_{TC}$ and C $_{TC}$), ten buffered outputs (Q $_3$ to Q $_9$ and Q $_{11}$ to Q $_{13}$) and an overriding asynchronous master reset (MR).

The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. In this case keep the other oscillator pins (R $_{TC}$ and C $_{TC}$) floating.

The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (Q3 to Q9 and Q11 to Q13 = LOW), independent of other input conditions.

In the HCT version, the MR input is TTL compatible, but the RS input has CMOS input switching levels and can be driven by a TTL output by using a pull-up resistor to V_{CC} .

		HSSIPATION FO	TYF	PICAL	AMYC
SYMBOL	PARAMETER HORALUMAOS JACISYT	CONDITIONS	НС	нст	UNIT
^t PHL/ ^t PLH ^t PHL	propagation delay RS to Q3 Q _n to Q _{n+1} MR to Q _n	C _L = 15 pF V _{CC} = 5 V	31 6 17	31 6 18	ns ns ns
fmax	maximum clock frequency	3°	87	88	MHz
CI	input capacitance TOHAT F	MSSIPATION FO	3.5	3.5	pF
CPD (Wal)	power dissipation capacitance per package	notes 1, 2 and 3	40	40	pF

Notes DOV x JOIZ + DOV x prof x gad

- 1. CPD is used to determine the dynamic power dissipation (PD in μ W):

 PD = CPD × VCC² × f₁ + Σ (CL × VCC² × f₀) where:
 - f_i = input frequency in MHz f_O = output frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V
- Σ (C_L x V_{CC}² x f₀) = sum of outputs
- 2. For HC the condition is V_I = GND to V_{CC}

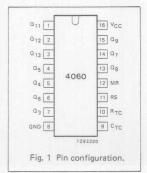
 For HCT the condition is V_I = GND to V_{CC} 1.5 V
- 3. For formula on dynamic power dissipation see next page.

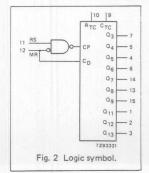
PACKAGE OUTLINES

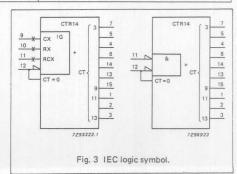
16-lead DIL; plastic (SOT38Z). 16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	Q ₁₁ to Q ₁₃	counter outputs
7, 5, 4, 6, 14, 13, 15	Q3 to Q9	counter outputs
8	GND	ground (0 V)
9	CTC	external capacitor connection
10	RTC	external resistor connection
11	RS	clock input/oscillator pin
12	MR	master reset
16	Vcc	positive supply voltage







DYNAMIC POWER DISSIPATION FOR 74HC

PARAMETER	VCC	TYPICAL FORMULA FOR P_D (μW) (note 1)	An active components on sma RC or crystal oscillator
total dynamic power dissipation when using the on-chip oscillator (PD)	2.0 4.5 6.0	$\begin{array}{c} \text{CpD} \times f_{\text{OSC}} \times \text{V}_{\text{CC}^2} + \Sigma (\text{C}_{\text{L}} \times \text{V}_{\text{CC}^2} \times f_{\text{o}}) + 2\text{C}_{\text{t}} \times \text{V}_{\text{CC}^2} \\ \text{CpD} \times f_{\text{OSC}} \times \text{V}_{\text{CC}^2} + \Sigma (\text{C}_{\text{L}} \times \text{V}_{\text{CC}^2} \times f_{\text{o}}) + 2\text{C}_{\text{t}} \times \text{V}_{\text{CC}^2} \\ \text{CpD} \times f_{\text{OSC}} \times \text{V}_{\text{CC}^2} + \Sigma (\text{C}_{\text{L}} \times \text{V}_{\text{CC}^2} \times f_{\text{o}}) + 2\text{C}_{\text{t}} \times \text{V}_{\text{CC}^2} \end{array}$	x fosc + 1 750 x VCC

GND = 0 V; Tamb = 25 °C

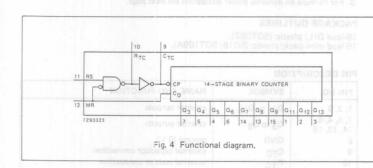
DYNAMIC POWER DISSIPATION FOR 74HCT

PARAMETER 04 6 60	v VCC	TYPICAL FORMULA FOR P _D (μW) (note 1)
total dynamic power dissipation when using the on-chip oscillator (PD)	4.5	$Cp_{D} \times f_{osc} \times V_{CC^2} + \Sigma (CL \times V_{CC^2} \times f_{o}) + 2C_{t} \times V_{CC^2} \times f_{osc} + 1750 \times V_{CC}$

GND = 0 V; T_{amb} = 25 °C (arenve (et x 500 V x 30) 2 + et x 500 V x 690 = 69

Notes

1. Where: f_0 = output frequency in MHz C_L = output load capacitance in pF f_{OSC} = oscillator frequency in MHz C_t = timing capacitance in pF $\Sigma \{C_L \times V_{CC}^2 \times f_0\}$ = surn of outputs V_{CC} = supply voltage in V

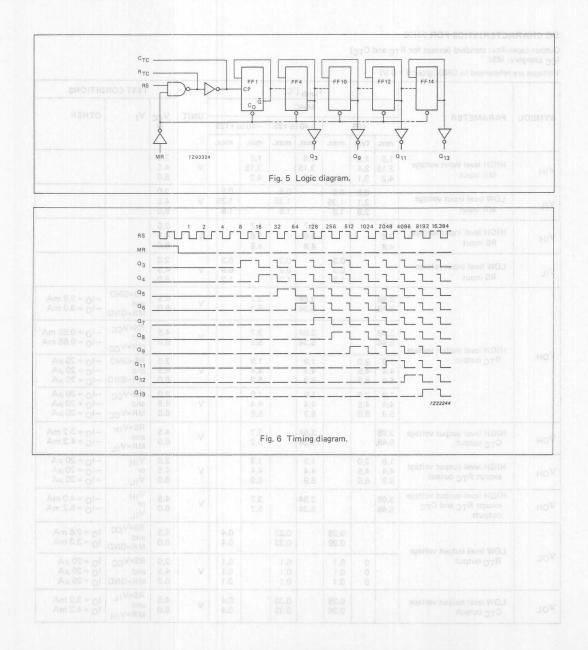


APPLICATIONS

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits







DC CHARACTERISTICS FOR 74HC

Output capability: standard (except for $R_{\mbox{\scriptsize TC}}$ and $C_{\mbox{\scriptsize TC}})$ $I_{\mbox{\scriptsize CC}}$ category: MSI

Voltages are referenced to GND (ground = 0 V)

					T _{amb} (°C)	-53		1-1-0		TEST CON	DITIONS
	The state of the s	0			74HC				UNIT	V	VI	OTHER
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNII	V _{CC}	V	OTHER
	The state of the s	min.	typ.	max.	min.	max.	min.	max.		4		
VIH	HIGH level input voltage MR input	1.5 3.15 4.2	1.3 2.4 3.1	mengel	1.5 3.15 4.2	8 .61-	1.5 3.15 4.2		V	2.0 4.5 6.0		
VIL	LOW level input voltage MR input		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
VIH	HIGH level input voltage RS input	1.7 3.6 4.8	J	F-135	1.7 3.6 4.8	ij	1.7 3.6 4.8	rún	V	2.0 4.5 6.0	ER BM	
VIL	LOW level input voltage RS input			0.3 0.9 1.2	J-	0.3 0.9 1.2	-[-	0.3 0.9 1.2	V	2.0 4.5 6.0	z (0)	
		3.98 5.48	- T - T - T		3.84 5.34		3.7 5.2		V	4.5 6.0	RS=GND and MR=GND	-I _O = 2.6 mA -I _O = 3.3 mA
	HIGH level output voltage R _{TC} output	3.98 5.48	ζ <u> </u>	Ħ.	3.84 5.34		3.7 5.2		V	4.5 6.0	RS=V _{CC} and MR=V _{CC}	-1 _O = 0.65 mA -1 _O = 0.85 mA
Vон		1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	RS=GND and MR=GND	$-1_{O} = 20 \mu A$ $-1_{O} = 20 \mu A$ $-1_{O} = 20 \mu A$
		1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	RS=V _{CC} and MR=V _{CC}	-1 _O = 20 μA -1 _O = 20 μA -1 _O = 20 μA
Vон	HIGH level output voltage CTC output	3.98 5.48		agram.	3.84 5.34	er a s	3.7 5.2		V	4.5 6.0	RS=V _{IH} and MR=V _{IL}	-I _O = 3.2 mA -I _O = 4.2 mA
Vон	HIGH level output voltage except R _{TC} output	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	7	V	2.0 4.5 6.0	V _{IH} or V _{IL}	-I _O = 20 μA -I _O = 20 μA -I _O = 20 μA
Vон	HIGH level output voltage except R _{TC} and C _{TC} outputs	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V _{IH} or V _{IL}	-I _O = 4.0 mA -I _O = 5.2 mA
	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4		4.5 6.0	RS=V _{CC} and MR=GND	I _O = 2.6 mA I _O = 3.3 mA
VOL	R _{TC} output		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	RS=V _{CC} and MR=GND	I _O = 20 μA I _O = 20 μA I _O = 20 μA
VoL	LOW level output voltage CTC output			0.26 0.26		0.33 0.33		0.4 0.4	v	4.5 6.0	RS=V _{IL} and MR=V _{IH}	I _O = 3.2 mA I _O = 4.2 mA

							T _{amb} ((°C)			CONTRACTOR OF THE PARTY OF THE	90	08 = 10	TEST CON	DITIONS
	TEST CONDIT						74H0	Cat				UNIT	Vcc	VI	OTHER
SYMBOL	PARAMETE				+25		-40	to +85	-40) to	+125	OWIT	V		
	WAVEFORM			min.	typ.	max.	min.	max.	min		max.			BTBMARA	SYMBOL P
VoL	LOW level of except R _T (tage	wen	0 0	0.1 0.1 0.1	m lal	0.1 0.1 0.1	im i	gyi	0.1 0.1 0.1	V	2.0 4.5 6.0	VIH or VIL	$I_{O} = 20 \mu A$ $I_{O} = 20 \mu A$ $I_{O} = 20 \mu A$
VoL	LOW level of except RT(96		0.26 0.26	78 88	0.33 0.33	08	900	0.4 0.4	V	4.5 6.0	V _{IH} or V _{IL}	1 _O = 4.0 mA 1 _O = 5.2 mA
±II	input leakage	e current	813	120 24 10		0.1	20	1.0	180	52	1.0	μА	6.0	V _{CC} or GND	ISTH SE
lcc	quiescent su	pply curr	ent	886 83 86		8.0	25. 44. 28.	80.0	11 35 36	900	160.0	μА	6.0	VCC or GND	IO = 0

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

ABH	TO VCC VI OT					T _{amb} (°C)				la la	TEST CONDITIO	NS
SYMBOL	PARAMETER		857+0×04 88+74HC- 85+								Vac	WAVEFORMS	
			+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORING	
			min.	typ.	max.	min.	max.	min.	max.	eparto	e spese	LOW level of	364
^t PHL [/]	propagation delay RS to Q3	٧	2.6 2.6	99 36 29	300 60 51	6	375 75 64	0	450 90 77	ns ^{eggri} o	2.0 4.5 6.0	Fig. 12	70%
^t PHL [/] ^t PLH	propagation delay Ω_n to Ω_{n+1}	Au	0.1	22 8 6	80 16 14	.1	100 20 17	d.	120 24 20	ns 34	2.0 4.5 6.0	Fig. 14	(1)
^t PHL 0 =	propagation delay MR to Q _n	Ащ	9,08	55 20 16	175 35 30	16	220 44 37	8	265 53 45	ns ^{1ma} 1	2.0 4.5 6.0	Fig. 13	50
^t THL [/]	output transition time			19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 12	
tw	clock pulse width RS; HIGH or LOW		80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 12	
tw	master reset pulse width MR; HIGH		80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 13	
t _{rem}	removal time MR to RS		100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 13	
f _{max}	maximum clock pulse frequency		6.0 30 35	26 80 95		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 12	

DC CHARACTERISTICS FOR 74HCT

Output capability: standard (except for $R_{\mbox{\scriptsize TC}}$ and $C_{\mbox{\scriptsize TC}})$ $I_{\mbox{\scriptsize CC}}$ category: MSI

Voltages are referenced to GND (ground = 0 V)

RSHT		201		700	Tamb	(°C)		TEST CONDITIONS					
CVMDOL	PARAMETER	74HCT								\/	V.	OTHER	
SYMBOL		+25			-40 to +85		-40 to +125		UNIT	VCC	VI	UTHER	
0=6		min.	typ.	max.	min.	max.	min.	max.	78613	uo ylad	uiescent su	l loc	
V _{IH} 1911	HIGH level input voltage	2.0		02	2.0	103	2.0		Vicus	4.5 to 5.5	ip lancifilib lancifilib	note 2	
VIL	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5	(f stor	note 2	
	s fable below.	3.98	svig s	f to be	3.84	s tot s	3.7	nsinus v	Vata	4.5	RS=GND and MR=GND	-I _O = 2.6 mA	
V -	HIGH level output voltage	3.98		1101235	3.84	H12 101	3.7	amostana	V	4.5	RS=V _{CC} and MR=V _{CC}	$-1_0 = 0.65 \text{ mA}$	
Vон	R _{TC} output	4.4	4.5		4.4		4.4		V	4.5	RS=GND and MR=GND	-1 _O = 20 μA	
		4.4	4.5		4.4		4.4		74HV	4.5	RS=V _{CC} and MR=V _{CC}	-I _O = 20 μA	
VOH	HIGH level output voltage CTC output	3.98			3.84	nsT	3.7		V	4.5	RS=V _{IH} and MR=V _{IL}	-I _O = 3.2 mA	
Vон	HIGH level output voltage except R _{TC} output	4.4	4.5	- 18	4.4		4.4		V	4.5	VIH OR VIL	-I _O = 20 μA	
Vон	HIGH level output voltage except R _{TC} and C _{TC} outputs	3.98	.6.	en oxi	3.84	es .xe	3.7	e nim	V	4.5	V _{IH} or V _{IL}	-I _O = 4.0 mA	
V/-	LOW level output voltage	. Art		0.26	20	0.33	ar i	0.4	V	4.5	RS=V _{CC} and MR=GND	I _O = 2.6 mA	
VoL	R _{TC} output	84	0	0.1	86	0.1	80 1	0.1	V	4.5	RS=V _{CC} and MR=GND	ΙΟ = 20 μΑ	
VoL	LOW level output voltage CTC output	2		0.26	Or .	0.33	āl	0.4	V	4.5	RS=V _{IL} and MR=V _{IH}	1 _O = 3.2 mA	
VOL	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V _{IH} or V _{IL}	ΙΟ = 20 μΑ	
VOL	LOW level output voltage except R _{TC} and C _{TC} outputs			0.26		0.33		0.4	V	4.5	V _{IH} or V _{IL}	I _O = 4.0 mA	
± 1 ₁	input leakage current			0.1		1.0		1.0	μΑ	5.5	VCC or GND	v men	

DC CHARACTERISTICS FOR 74HCT (continued)

Voltages are referenced to GND (ground = 0 V)

					T _{amb} (°C)		TEST CONDITIONS				
SYMBOL					74HC	т	(ground	NA STATE	of bearing	918 8096710 V		
	PARAMETER		+25		-40 t	to +85	-40 t	o +125	UNIT	VCC	VI	OTHER
		min.	typ.	max.	min.	max.	min.	max.		83	TAMARA	
l _{CC}	quiescent supply current	esi -	inin.	8.0	or or	80.0	- cy/5	160.0	μΑ	5.5	VCC or GND	I _O = 0
ΔI _{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360	0,5	450		490	egstio μΑ	4.5 to 5.5	Vcc -2.1 V	other inputs at V _{CC} or GND; I _O = 0

Notes to HCT types

The value of additional quiescent supply current (\(\Delta\CC\)) for a unit load of 1 is given here.
 To determine \(\Delta\CC\) per input, multiply this value by the unit load coefficient shown in the table below.
 Only input MR (pin 12) has TTL input switching levels for the HCT versions.

INPUT	UNIT LOAD COEFFICIENT
MR	0.40

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

Am 2.8 = g		V		3	Tamb	(°C)		3.98	oltage	Hughi	TEST CONDITION	VS OV
	PARAMETER	-	74HCT									
SYMBOL		V	+25			-40 to +85		-40 to +125		V _{CC}	WAVEFORMS	
	нг	min.	typ.	max.	min.	max.	min.	max.	505110		Hevel HOTH	
tPHL/ tPLH	propagation delay RS to Q3	•	33	66	900	83		99	ns	4.5	Fig. 12	HO.
tPHL/	propagation delay Q _n to Q _{n+1}	,4 V	8	16	.0	20	1,0	24	ns perio	4.5	Fig. 14	JoV
tPHL OS	propagation delay MR to Q _n	V L	21	44	1.0	55	0	66	ns	4.5	Fig. 13	
tTHL/ tTLH	output transition time	V h	7	15	0.5	19	10	22	ns ^{agasti}	4.5	Fig. 12	JoV
tw Aut OS =	clock pulse width RS; HIGH or LOW	16	6		20		24	0	ns aperi	4.5	Fig. 12	Jov
tw Amos	master reset pulse width MR; HIGH	16	6	6	20	8	24		ns agert	4.5	Fig. 13	ınV
^t rem	removal time MR to RS	26	13		33		39		ns	4.5	Fig. 13	
f _{max}	maximum clock pulse frequency	30	80		24		20		MHz	4.5	Fig. 12	- piz

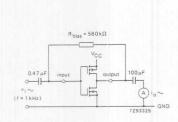


Fig. 7 Test set-up for measuring forward transconductance $g_S = di_0/dv_1$ at v_0 is constant (see also graph Fig. 8); MR = LOW.

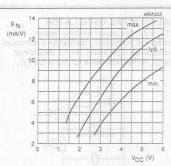


Fig. 8 Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at T_{amb} = 25 °C.

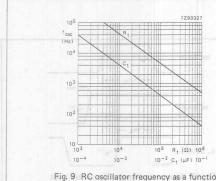


Fig. 9 RC oscillator frequency as a function of R_t and C_t at V_{CC} = 2.0 to 6.0 V; T_{amb} = 25 °C. C_t curve at R_t = 100 k Ω ; R2 = 200 k Ω . R_t curve at C_t = 1 nF; R2 = 2 x R_t .

RC OSCILLATOR

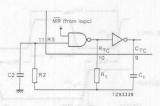


Fig. 10 Example of a RC oscillator. Typical formula for oscillator frequency: $f_{osc} = \frac{1}{2.5 \times R_t \times C_t}$

TIMING COMPONENT LIMITATIONS

The oscillator frequency is mainly determined by R_tC_t , provided $R2\approx 2R_t$ and $R2C2 \leqslant R_tC_t$. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the "ON" resistance in series with it, which typically is $280~\Omega$ at $V_{CC}=2.0~V$, $130~\Omega$ at $V_{CC}=4.5~V$ and $100~\Omega$ at $V_{CC}=6.0~V$. The recommended values for these components to maintain agreement with the typical oscillation formula are:

 $C_{t} > 50 \ pF$, up to any practical value,

 $10~k\Omega < R_{t} < 1~M\Omega.$

In order to avoid start-up problems, $R_{t}\geqslant 1~k\Omega.$

TYPICAL CRYSTAL OSCILLATOR

In Fig. 11, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 k Ω .

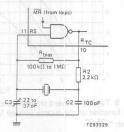


Fig. 11 External components connection for a crystal oscillator.

Fig. 7 Test sel-up for measuring forward remaind a constant (see also graph Fig. 8); MR = LOW.

AC WAVEFORMS

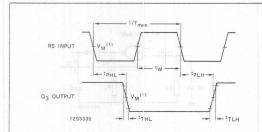


Fig. 12 Waveforms showing the clock (RS) to output (Q₃) propagation celays, the clock pulse width, the output transition times and the maximum clock frequency.

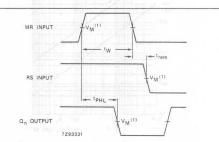


Fig. 13 Waveforms showing the master reset (MR) pulse width, the master reset to output (O_{Ω}) propagation delays and the master reset to clock (RS) removal time.

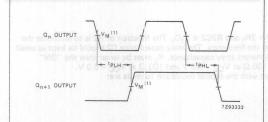


Fig. 14 Waveforms showing the output (Qn) to \mathbf{Q}_{n+1} propagation delays.

The oscillator frequency is mainly determined by R_1C_0 , provided influence of the forward voltage excess the input protection dicides as possible. In consideration of accuracy, C_1 must be larger than the resistance in series with it, which typically in 280.02 at $V_{C_0} = 2.0^\circ$. The accommended values for these components to maintain agrees $C_1 > 30$ pF, up to early practical value, $C_1 > 30$ pF, up to early practical value,

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD BILATERAL SWITCHES

FEATURES

- Very low "ON" resistance: 50 Ω (typ.) at V_{CC} = 4.5 V 45 Ω (typ.) at V_{CC} = 6.0 V 35 Ω (typ.) at V_{CC} = 9.0 V
- Output capability: non-standard
- ICC category: SSI

GENERAL DESCRIPTION

The 74HC/HCT4066 are high-speed Si-gate CMOS devices and are pin compatible with the "4006" of the "4008" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4066 have four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH enable input (nE). When nE is LOW the belonging analog switch is turned off.

The "4066" is pin compatible with the "4016" but exhibits a much lower "ON" resistance. In addition, the "ON" resistance is relatively constant over the full input signal range.

CVMBOL	FUNCTION TABLE	CONDITIONS	TYF		
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
tPZH/	turn-on time nE to V _{os}	CL = 15 pF	11	12	ns
tPHZ/ tPLZ	turn-off time nE to V _{OS}	$R_{L} = 1 k\Omega$ $V_{CC} = 5 V$	13	16	ns
CI	input capacitance	i diagram,	3.5	3.5	pF
C _{PD}	power dissipation capacitance per switch	notes 1 and 2	11	12	pF
CS	max. switch capacitance		8	8	pF

GND = 0 V; Tamb = 25 °C; tr = tf = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L + C_S) \times V_{CC}^2 \times f_o)$$
 where:

fi = input frequency in MHz

C_L = output load capacitance in pF C_S = max. switch capacitance in pF

 f_0 = output frequency in MHz $\Sigma \{ (C_L + C_S) \times V_{CC}^2 \times f_0 \} = \text{sum of outputs}$

VCC = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} -1,5 V

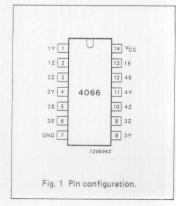
PACKAGE OUTLINES

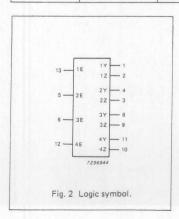
14-lead DIL; plastic (SOT27).

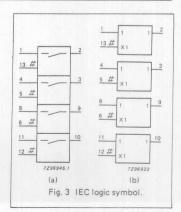
14-lead mini-pack; plastic (SO14; SOT108A).

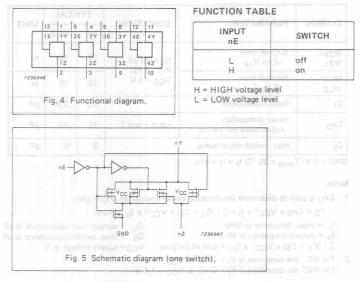
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	1Y to 4Y	independent inputs/outputs
2, 3, 9, 10	1Z to 4Z	independent inputs/outputs
7	GND	ground (0 V)
13, 5, 6, 12	1E to 4E	enable inputs (active HIGH)
14	Vcc	positive supply voltage









NAME AND FUNCTION		
	vov.	



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134) Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS	
Vcc	DC supply voltage	-0.5	+11.0	V		
±11K	DC digital input diode current	Dr. 44 (36)	20	mA	for $V_1 < -0.5 \text{ V}$ or $V_1 > V_{CC} + 0.5 \text{ V}$	SYMB
±1SK	DC switch diode current		20	mA	for V_S < -0.5 V or V_S > V_{CC} + 0.5 V	
±IS	DC switch current	IN AN	25	mA	for -0.5 V < V _S < V _{CC} + 0.5 V	
±ICC; ±IGND	DC VCC or GND current	ο Γ	50	mA	ON-essistance (peak) 84 98	иоп
T _{stg}	storage temperature range	-65	+150	°C	32 70	
Ptot V	power dissipation per package	1 f 0 f 1 8	750	mW	for temperature range: —40 to +125 °C 74HC/HCT above +70 °C: derate linearly with 12 mW/K	non
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K	
Ps 10 n	power dissipation per switch		100	mW	OM-resistance (reit) 000	NoR

Note to the Ratings

To avoid drawing V_{CC} current out of terminal nZ, when switch current flows in terminal nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no V_{CC} current will flow out of terminal nY. In this case there is no limit for the voltage drop across the switch, but the voltages at nY and nZ may not exceed V_{CC} or GND.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER 250 PARAMETER	duns est	74HC		Ino slan	74HC	2 V, the nsmit d	UNIT	CONDITIONS
STIMBUL	PARAMETER	min.	typ.	max.	min.	typ.	max.	UNIT	CONDITIONS
Vcc	DC supply voltage	2.0	5.0	10.0	4.5	5.0	5.5	V	
VI	DC input voltage range	GND		Vcc	GND		Vcc	٧	
Vs	DC switch voltage range	GND		Vcc	GND	-	Vcc	V	pont I
T _{amb}	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC
T _{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	CHARACTERISTICS
t _r , t _f	input rise and fall times		6.0	1000 500 400 250	iber MO	6.0	500	ns	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V V _{CC} = 10.0 V

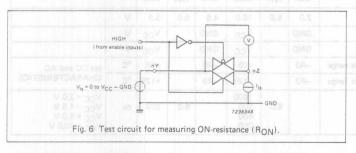
DC CHARACTERISTICS FOR 74HC/HCT

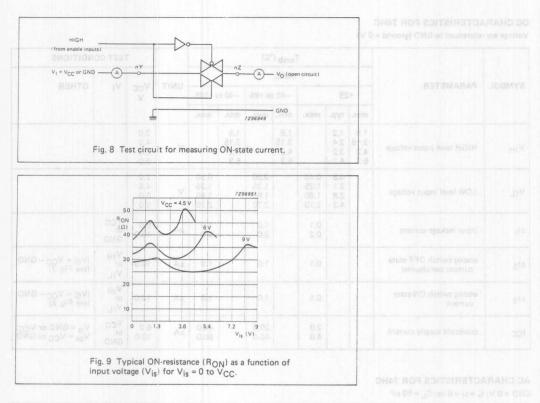
For 74HC: $V_{CC} = 2.0, 4.5, 6.0$ and 9.0 V For 74HCT: $V_{CC} = 4.5 \text{ V}$

		SNIC	ma	100	T _{amb} (°C)	.10	IN		85	TEST CO	NDITIO	ONS
				7	74HC/HCT		-0.5			egation	ylqqus .	a l	Joy
SYMBOL	PARAMETER OV < 14 to	+25			-40 to +85		-40 to +125		UNIT	VCC	ls μA	Vis	VI
		min.	typ.	max.	min.	max.	min.	max.	3mminu	diode o	riotive S sintiwe S		ilsk ste
R _{ON}	ON-resistance (peak)		- 54 42 32	95 84 70	Am 5°	- 118 105 88		142 126 105	Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	VCC to GND	VIH or VIL
RON	ON-resistance (rail)		80 35 27 20	- 75 65 55	Wati	95 82 70		115 100 85	Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	GND	V _{IH} or V _{IL}
R _{ON}	ON-resistance (rail)	95 ; O°	100 42 35 27	80 75 60	Win	106 94 78		128 113 95	Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	Vcc	VIH or VIL
ΔR _{ON}	maximum variation of ON-resistance between any two channels	A'in li rentaw ay not	- 5 4 3	V on 3 V on 3 ons Yn	t then to lank ts tage	itch cor ito term the void	nen sw lows in n, but	al nZ, w convent ne swite	Ω	2.0 4.5 6.0 9.0	the velt	V _{CC} to GND	VIH or VIL

Note to DC characteristics

1. At supply voltages approaching 2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.





DC CHARACTERISTICS FOR 74HC

Voltage are referenced to GND (ground = 0 V)

					T _{amb} (°C)					TEST CO	NDITIONS
01/11001				Chapita	74HC	-0-				.,	0-	OTHER
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	VI	OTHER
		min.	typ.	max.	min.	max.	min.	max.		1		
V _{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3	ervap st	1.5 3.15 4.2 6.3	ดูกเาษย	V	2.0 4.5 6.0 9.0	T 8 .pi	
VIL	LOW level input voltage		0.8 2.1 2.8 4.3	0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70	ās:	0.50 1.35 1.80 2.70	V	2.0 4.5 6.0 9.0		
±ΙΙ	input leakage current			0.1 0.2		1.0	e	1.0	μА	6.0	V _{CC} or GND	
±IS	analog switch OFF-state current per channel			0.1		1.0	1	1.0	μА	10.0	VIH or VIL	V _S = V _{CC} - GND (see Fig. 7)
±Ις	analog switch ON-state current			0.1		1.0		1.0	μА	10.0	VIH or VIL	V _S = V _{CC} - GND (see Fig. 8)
¹ cc	quiescent supply current			2.0 4.0		20.0 40.0	18	40.0 80.0	μА	6.0	V _{CC} or GND	V _{is} = GND or V _{CC} ; V _{os} = V _{CC} or GND

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

					T _{amb} (°C)				TEST CONDITIONS		
CVMPOL	DARAMETER	74HC									OTUED	
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	OTHER	
		min.	typ.	max.	min.	max.	min.	max.				
^t PHL [/] ^t PLH	propagation delay V _{is} to V _{os}		8 3 2 2	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 9.0	R _L = ∞; C _L = 50 pF (see Fig. 17)	
^t PZH [/] ^t PZL	turn-on time nE to V _{OS}		36 13 10 8	100 20 17 13		125 25 21 16		150 30 26 20	ns	2.0 4.5 6.0 9.0	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Figs 18 and 19)	
^t PHZ [/] ^t PLZ	turn-off time nE to V _{OS}		44 16 13 16	150 30 26 24		190 38 33 16		225 45 38 20	ns	2.0 4.5 6.0 9.0	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Figs 18 and 19)	

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

ENON					T _{amb} (°C)					TEST CO	NDITIONS	
					74HC	T				.,	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	OTHER	
SYMBOL	PARAMETER	acr +25 as			-40 to +85		-40 to +125		UNIT	VCC	NE IV	OTHER DAMYS	
		min.	typ.	max.	min.	max.	min.	max.					
V _{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0	8	٧	4.5 to 5.5	yətten de o V _{os}		
78 08 = 1	LOW level input voltage	8	1.2	0.8	30	0.8	24	0.8	V	4.5 to 5.5	o V _{os}	2-10,172 /2,143, 2-30 72,53 1-10,172 /4/2,63	
±I _I	input leakage current			0.1		1.0		1.0	μА	5.5	VCC or GND	3 30 230	
±1 _S	analog switch OFF-state current per channel			0.1		1.0	н/эна	1.0	μА	5.5	VIH or VIL	IV _S I = V _{CC} - GND (see Fig. 7)	
±IS	analog switch ON-state current	(q-q	ai V	0.1	T	1.0	,9YT	1.0	μА	5.5	V _{IH} or V _{IL}	V _S = V _{CC} - GND (see Fig. 8)	
¹ cc	quiescent supply current		0.B	2.0		20.0	0.04	40.0	μА	4.5 to 5.5	V _{CC} or GND	V _{is} = GND or V _{CC} ; V _{os} = V _{CC} or GND	
ΔICC	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450	0.12 0.08 —50	490	μА	4.5 to 5.5	V _{CC} -2.1 V	other inputs at VCC or GND	

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nE	1.00

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns$

			T _{amb} (°C)							TEST CONDITIONS			
	MBOL PARAMETER	F1001	74HCT							., 9	OTHERS JOSMY		
SYMBOL	PARAMETER	25	+25	15 4	-40	to +85	-40 t	o +125	UNIT	V _{CC}	OTHER		
	min.	typ.	max.	min.	max.	min.	max.						
t _{PHL} /	propagation delay V _{is} to V _{os}	V.	3	012		15	8	18 0 3	ns agai	4.5	R _L = ∞; C _L = 50 pF (see Fig. 17)		
t _{PZH} /	turn-on time nE to V _{os}		12	24	8.0	30	10 0	36	ns	4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 18 and 19)		
t _{PHZ} /	turn-off time		20	35		44		53	ns	4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 18 and 19)		

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

 $GND = 0 \ V : t_r = t_f = 6 \ ns$

SYMBOL	PARAMETER	a 0.1	TYP.	UNIT	Vcc V	V _{is(p-p)}	CONDITIONS
VCC of GND	sine-wave distortion f = 1 kHz	u. 0.68	0.04	%	4.5 9.0	4.0 8.0	$R_L = 10 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig. 15)
19.274000	sine-wave distortion f =10 kHz	n 080	0.12 0.06	% %	4.5 9.0	4.0 8.0	$R_{L} = 10 \text{ k}\Omega; C_{L} = 50 \text{ pF}$ (see Fig. 15)
5112	switch "OFF" signal feed-through		-50 -50	dB dB	4.5 9.0	note 1	$R_L = 600 \Omega$; $C_L = 50 pF$; f = 1 MHz (see Figs 10 and 16)
	crosstalk between any two switches	,ecet	-60 -60	dB dB	4.5 9.0	note 1	$R_L = 600 \Omega$; $C_L = 50 pF$; $f = 1 MHz$ (see Fig. 12)
V _(p-p)	crosstalk voltage between or address input to any st (peak-to-peak value)		110 220	mV mV	4.5 9.0	Ag armen stut A	R _L = 600Ω ; C _L = $50 pF$; f = 1 MHz (nE, square wave between V _{CC} and GND, t _r = t _f = $6 ns$) (see Fig. 13)
f _{max}	minimum frequency respo (-3 dB)	nse	180 200	MHz MHz	4.5 9.0	note 2	$R_L = 50 \Omega$; $C_L = 10 pF$ (see Figs 11 and 14)
Cs	maximum switch capacital	nce	8	pF			

Notes to the AC characteristics

 V_{ig} is the input voltage at nY or nZ terminal, whichever is assigned as an input. V_{OS} is the output voltage at nY or nZ terminal, whichever is assigned as an output.

- 1. Adjust input voltage V_{js} is 0 dBm level (0 dBm = 1 mW into 600 Ω). 2. Adjust input voltage V_{is} is 0 dBm level at V_{OS} for 1 MHz (0 dBm = 1 mW into 50 Ω).

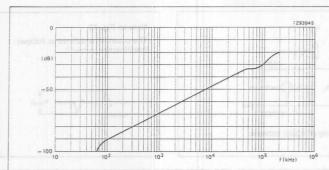


Fig. 10 Typical switch "OFF" signal feed-through as a function of frequency.

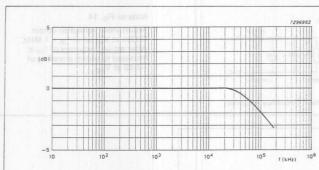
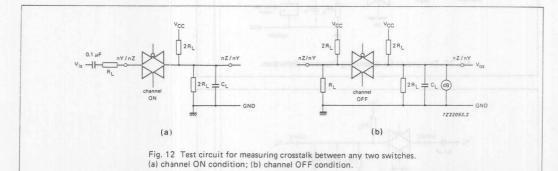


Fig. 11 Typical frequency response.

Note to Figs 10 and 11 Test conditions: $V_{CC} = 4.5 \text{ V; GND} = 0 \text{ V;} \\ R_L = 50 \Omega; R_{source} = 1 \text{ k}\Omega.$



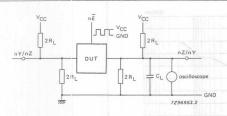


Fig. 13 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 13 The crosstalk is defined as follows (oscilloscope output):

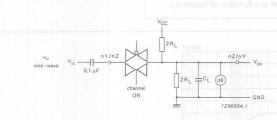


Fig. 14 Test circuit for measuring minimum frequency response.

Note to Fig. 14

Adjust input voltage to obtain 0 dBm at V_{os} when $f_{in} = 1$ MHz. After set-up frequency of f_{in} is increased to obtain a reading of -3 dB at V_{os} .

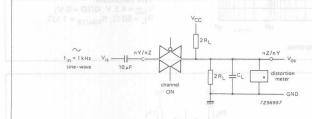
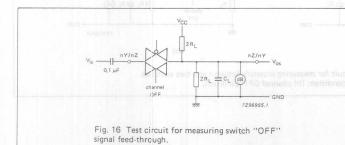
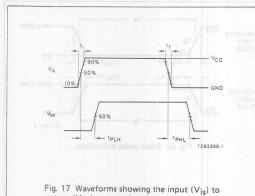


Fig. 15 Test circuit for measuring sine-wave distortion.



AC WAVEFORMS



output (Vos) propagation delays.

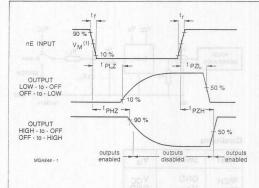


Fig. 18 Waveforms showing the turn-on and turn-off times.

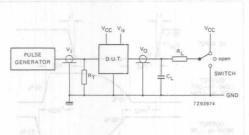
Note to AC waveforms

(1) HC : $V_{M} = 50\%$; $V_{I} = GND$ to V_{CC} . HCT: $V_{M} = 1.3 \text{ V}$; $V_{I} = \text{GND to } 3 \text{ V}$.



TEST CIRCUIT AND WAVEFORMS

AC WAVEFORMS



Conditions

TEST	SWITCH	Vis
tPZH	GND	VCC
tPZL	VCC	GND
tPHZ	GND	VCC
tPLZ	VCC	GND
others	open	pulse

Fig. 19 Test circuit for measuring AC performance.

Definitions for Figs 19 and 20:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

 $t_r = t_f = 6$ ns, when measuring f_{max} , there is no constraint on t_r , t_f with 50% duty factor.

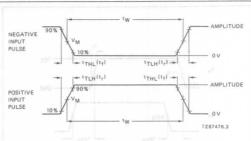


Fig. 20 Input pulse definitions.

Fig. 17. Waveforms showing the input (V₁₈) to output (V₀₈) propagation delays.

16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- Low "ON" resistance: 80 Ω (typ.) at V_{CC} = 4.5 V 70 Ω (typ.) at V_{CC} = 6.0 V 60 Ω (typ.) at V_{CC} = 9.0 V typical "break before make" built-in
- Output capability: non-standard
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4067 are high-speed Si-gate CMOS devices and are pin compatible with the "4067" of the "4008" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4067 are 16-channel analog multiplexers/demultiplexers with four address inputs (S_0 to S_3), an active LOW enable input (\overline{E}), sixteen independent inputs/outputs (Y_0 to Y_{15}) and a common input/output (Z).

The "4067" contains sixteen bidirectional analog switches, each with one side connected to an independent input/output (γ_0 to γ_{15}) and the other side connected to a common input/output (Z).

With E LOW, one of the sixteen switches is selected (low impedance ON-state) by S₀ to S₃. All unselected switches are in the high impedance OFF-state. With E HIGH, all switches are in the high impedance OFF-state, independent of S₀ to S₃.

The analog inputs/outputs (Y0 to Y15, and Z) can swing between V $_{CC}$ as a positive limit and GND as a negative limit. V $_{CC}$ to GND may not exceed 10 V.

SYMBOL	DADAMETED	CONDITIONS	TYF	io ini	
SAMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
^t PZL [/] ^t PZH	turn-on time E to V _{os} S _n to V _{os}	C _L = 15 pF	26 29	32 33	ns ns
^t PLZ [/] ^t PHZ	E to Vos S _n to Vos turn-off time E to Vos S _n to Vos	$R_L = 1 k\Omega$ $V_{CC} = 5 V$	27 29	26 30	ns ns
CI	input capacitance	dans.	3,5	3.5	pF
C _{PD}		notes 1 and 2	29	29	pF
CS	independent (Y)		5 45	5 45	pF pF

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

Notes

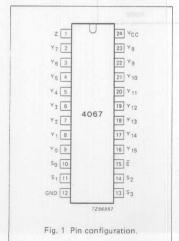
1. CpD is used to determine the dynamic power dissipation (PD in μ W):

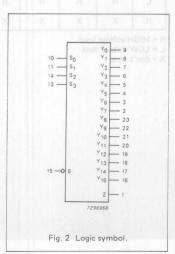
$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$$
 where:

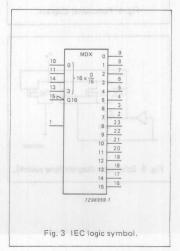
- fo = output frequency in MHz
- $\Sigma \left\{ (C_L + C_S) \times V_{CC}^2 \times f_0 \right\} = \text{sum of outputs}$ VCC = supply voltage in V
- 2. For HC the condition is $V_1 = GND$ to V_{CC}
- For HCT the condition is $V_1 = GND$ to V_{CC} For HCT the condition is $V_1 = GND$ to $V_{CC} = 1.5 \text{ V}$

PACKAGE OUTLINES

- 24-lead DIL; plastic (SOT101A).
- 24-lead mini-pack; plastic (SO24; SOT137A).







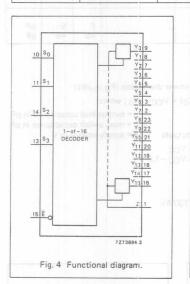
Cs = max. switch capacitance in pF

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	2001110
1	Z	common input/output	
9, 8, 7, 6,	26	E tei V _{es}	
5, 4, 3, 2, 23, 22, 21, 20,	Y ₀ to Y ₁₅	independent inputs/outputs	
19, 18, 17, 16	-5.V	Smit tib-mul	
10, 11, 14, 13	So to S3	address inputs	
12	GND	ground (0 V)	
15	Ē	enable input (active LOW)	
24	Vcc	positive supply voltage	

APPLICATIONS

- Analog multiplexing and demultiplexing $\sqrt{\ln (gya)} \Omega$ 08
- Digital multiplexing and demultiplexing
 Signal gating



FUNCTION TABLE

	(S) hon	INPUTS	3		CHANNEL
E	S ₃	s ₂	s ₁	s ₀	ON
umeryb + lar)		L of G	L 690 D =H39 D =H39	L	Y ₀ - Z Y ₁ - Z Y ₂ - Z Y ₃ - Z
L to pus or clus	HAMED VS	H H H	H	H	Y ₄ - Z Y ₅ - Z Y ₆ - Z Y ₇ - Z
L L L (A	10 H 03	pittalge	CK-JGE leacHold leacHold	J 24	Y ₈ - Z Y ₉ - Z Y ₁₀ - Z Y ₁₁ - Z
L L L	н н н	H	L H H	H L H	Y ₁₂ - Z Y ₁₃ - Z Y ₁₄ - Z Y ₁₅ - Z
Н	X	X	X	X	none



L = LOW voltage level

X = don't care

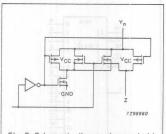
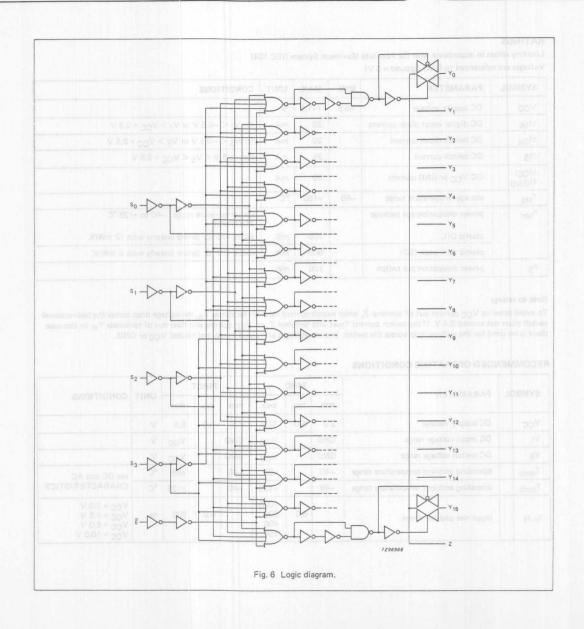


Fig. 5 Schematic diagram (one switch).



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
Vcc	DC supply voltage	-0.5	+11.0	V	
±11K	DC digital input diode current		20	mA	for $V_1 < -0.5 \text{ V}$ or $V_1 > V_{CC} + 0.5 \text{ V}$
±1SK	DC switch diode current		20	mA	for V_S < -0.5 V or V_S > V_{CC} + 0.5 V
±1S	DC switch current		25	mA	for $-0.5 \text{ V} < \text{V}_{\text{S}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$
±ICC; ±IGND	DC V _{CC} or GND current		50	mA	
T _{stg}	storage temperature range	-65	+150	°C	
P _{tot}	power dissipation per package	-			for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
Ps	power dissipation per switch	-	100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Y_n , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Y_n . In this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or GND.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74HC			74HC1		UNIT	CONDITIONS	
STIMBOL	FANAMETEN	min.	typ.	max.	min.	typ.	max.	UNIT	CONDITIONS	
Vcc	DC supply voltage	2.0	5.0	10.0	4.5	5.0	5.5	V		
VI	DC input voltage range	GND		Vcc	GND		Vcc	V		
Vs	DC switch voltage range	GND	7	Vcc	GND		Vcc	V		
T _{amb}	operating ambient temperature range	-40	AL	+85	-40		+85	°C	see DC and AC	
T _{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	CHARACTERISTIC	
t _r , t _f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V V _{CC} = 10.0 V	

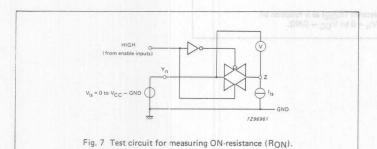
DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: $V_{CC}-GND$ = 2.0, 4.5, 6.0 and 9.0 V For 74HCT: $V_{CC}-GND$ = 4.5 V

					T _{amb} (°C)	De	1		TEST CONDITIONS						
RON	DADAMETER			7	4HC/F	UNIT	Vac	1-	Vis	٧.						
SAMBOL	PARAMETER	+25		-40	to +85 -40 to +125		-40 to +125		-40 to +125		-40 to +125		V _{CC}	I _S μA	V IS	VIH or VIL VIH or VIL VIH or VIL
		min.	typ.	max.	min.	max.	min.	max.	1				VIH or VIL VIH or VIL			
RON	ON-resistance (peak)		110 95 75	- 180 160 130	dña	225 200 165	IS MO	- 270 240 195	Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	V _C C to GND	or			
RON	ON-resistance (rail)		150 90 80 70	- 160 140 120		- 200 175 150	#15c1	- 240 210 180	Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	GND or VCC	or			
ΔR _{ON}	maximum variation of ON-resistance between any two channels		9 8 6			V		Ä	ΩΩΩ	2.0 4.5 6.0 9.0		VCC to GND	or			

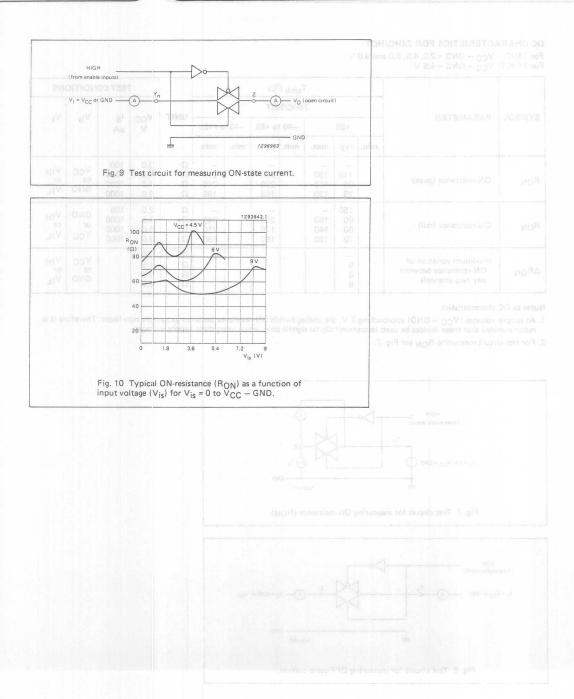
Notes to DC characteristics

- At supply voltages (V_{CC} GND) approaching 2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- 2. For test circuit measuring RON see Fig. 7.



7296962

Fig. 8 Test circuit for measuring OFF-state current.



DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

	TEST CONDI				Tamb (°C)			TEST CONDITIONS				
					74H	С	LIBUT	.,		OTHER			
SYMBOL	PARAMETER V TIMU		+25	- 88	-40 to +85		-40 to +125		UNIT	V _{CC}	VIBMA	OTHER OBNES	
		min.	typ.	max.	min.	max.	min.	max.					
V _{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3	8 7 8	V	2.0 4.5 6.0 9.0	sgateon d to V _{OS} .	NAME AND ASSESSED.	
VIL	LOW level input voltage	06 81 81 81 81	0.8 2.1 2.8 4.3	0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70	08 8 01 01 9	0.50 1.35 1.80 2.70	V	2.0 4.5 6.0 9.0	o noisaga o V os n Y		
±II	input leakage current	875 15 14		0.1 0.2	200	1.0	es i i	1.0 2.0	μА	6.0 10.0	V _{CC} or GND	-mro /2Hdg	
±IS	analog switch OFF-state current per channel	971		0.1	88 88	1.0	86 1 85 6 98 1	1.0	μА	10.0	VIH or VIL	V _S = V _{CC} - GNI (see Fig. 8)	
±IS	analog switch OFF-state current all channels	54 57 57		0.8	100	8.0	88 1 86 1	8.0	μА	10.0	V _{IH} or V _{IL}	V _S = V _{CC} - GNI (see Fig. 9)	
±Is	analog switch ON-state current	E1		0.8	10 E	8.0	58 1 A7 1 A2	8.0	μА	10.0	VIH OF	VS = VCC - GNI (see Fig. 9)	
lcc	quiescent supply current	135		8.0 16.0	36	80.0 160	1 58	160 320	μΑ	6.0	V _{CC} or GND	V _{is} = GND or V _{CC} V _{os} = V _{CC} or GN	

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

244	TEST CONDITIO					Tamb (°C)					TEST CONDI	TIONS
						74H	С				.,	OTHER	
SYMBOL	PARAMETER		25	+25	A-7-88	-40 to +85		-40 to +125		UNIT	V _{CC}	OTHER	
			min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay V _{is} to V _{os} ; Y _n to Z	V		25 9 7 5	75 15 13 9	21.5	95 19 16 11	2 .4 .2 .7	110 22 19 14	ns see	2.0 4.5 6.0 9.0	R_ = ∞; C ₁ = 50 pF	14174
^t PHL [/] ^t PLH	propagation delay V _{is} to V _{os} ; Z to Y _n			18 6 5 4	60 12 10 8		75 15 13 10	.8 0 1.1 2.8 2.2	90 18 15 12	ns 📆	2.0 4.5 6.0 9.0	(see Fig. 16)	
t _{PHZ} /	turn-off time E to Yn	Ą	0	74 27 22 20	250 50 43 38	2.1	315 63 54 48	0	375 75 64 57	ns	2.0 4.5 6.0 9.0	Bushel Tugni Burs solans Ted menuo Anties golana Tie xnerrus Anties golana Tie xnerrus	ţl.
t _{PHZ} /	turn-off time S _n to Y _n	A		83 30 24 21	250 50 43 38	A I	315 63 54 48	.0	375 75 64 57	ns	2.0 4.5 6.0 9.0		
t _{PHZ} /	turn-off time E to Z	A	ie	85 31 25 24	275 55 47 42	1.8	345 69 59 53	:0	415 83 71 63	ns erre	2.0 4.5 6.0 9.0		
^t PHZ [/] ^t PLZ	turn-off time S _n to Z	A	08	94 34 27 25	290 58 47 45	08	365 73 62 56	18.	435 87 74 68	ns	2.0 4.5 6.0 9.0	R _L = 1 kΩ;	
^t PZH [/] ^t PZL	turn-on time E to Yn			80 29 23 17	275 55 47 42		345 69 59 53		415 83 71 63	ns	2.0 4.5 6.0 9.0	C _L = 50 pF (see Fig. 17)	
^t PZH [/] ^t PZL	turn-on time S _n to Y _n			88 32 26 18	300 60 51 45		375 75 64 56		450 90 77 68	ns	2.0 4.5 6.0 9.0		
tpZH/ tpZL	turn-on time E to Z			85 31 25 18	275 55 47 42		345 69 59 53		415 83 71 63	ns	2.0 4.5 6.0 9.0		
^t PZH [/]	turn-on time S _n to Z			94 34 27 19	300 60 51 45		375 75 64 56		450 90 77 68	ns	2.0 4.5 6.0 9.0		

Note to AC characteristics for 74HC

Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

	DWOO TEST			- 0	T _{amb} (°C)					TEST CO	NDITIONS	
SYMBOL	PARAMETER				74HC	Т		V	VIAR	OTHER			
STIVIBUL PA	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	VI	OTHER	
		min.	typ.	max.	min.	max.	min.	max.					
VIH	HIGH level input voltage	2.0	1.6	6	2.0	21	2.0		V	4.5 to 5.5	opagation is to Vot	FIND,	
VIL	LOW level input voltage	31	1.2	0.8		0.8	a	0.8	V	4.5 to 5.5	opagation to Y or to Y or	/ HTds / /THds	
±I ₁	input leakage current	- 88		0.1		1.0	38	1.0	μА	5.5	VCC or GND	7 2 141 2 2 141 7 2 141	
±ΙS	analog switch OFF-state current per channel	09		0.1		1.0	DE	1.0	μА	5.5	V _{IH} or V _{IL}	V _S = V _{CC} - GND (see Fig. 8)	
± Is	analog switch OFF-state current all channels	08		0.8		8.0	35	8.0	μА	5.5	VIH or VIL	V _S = V _{CC} - GNE (see Fig. 9)	
±I _S	analog switch ON-state current	00		0.8		8.0	58	8.0	μА	5.5	VIH or VIL	VS = VCC - GNE (see Fig. 9)	
¹ cc	quiescent supply current	88		8.0		80.0		160	μА	4.5 to 5.5	V _{CC} or GND	V _{is} = GND or V _{CC} V _{os} = V _{CC} or GNE	
ΔICC	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)	.88	100	360		450	80	490	μΑ	4.5 to 5.5	V _{CC} -2.1 V	other inputs at VCC or GND	

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT	
E S _n	0.6 0.5	

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \ V; t_r = t_f = 6 \ ns$

					15	T _{amb} (°C)					TEST CONDI	TIONS
SYMBOL	BADAMETER					74HC	т			UNIT		OTUED	
STIVIBUL	PARAMETER		+125	+25		-40 to +85		-40 to +125		UNIT	VCC	OTHER	
			min.	typ.	max.	min.	max.	min.	max.				
tPHL/ tPLH	propagation delay V _{is} to V _{os} ; Y _n to Z	V		9 0.3	15	2.0	19	8.1	22	ns	4.5	R _L = ∞; C _L = 50 pF	Hel
tPHL/ tPLH	propagation delay V _{is} to V _{os} ; Z to Y _n	٧	8.0	6	12 8.0		15 8 6	1.2	18	ns	4.5	(see Fig. 16)	
tPHZ/ tPLZ	turn-off time E to Yn	Aug	0.1	26	55		69		83	ns	4.5	input lesis	
tPHZ/ tPLZ	turn-off time S _n to Y _n			31	55		69		83	ns	4.5	Bivve potenti	
tPHZ/	turn-off time E to Z	Ац	31	30	60		75		90	ns	4.5	Current S	
tPHZ/	turn-off time S _n to Z	Aug	8.8	35	60		75		90	nsetsta	4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$	
tPZH/	turn-on time E to Y _n	Acr	0.8	32	60		75		90	ns	4.5	(see Fig. 17)	
tPZH/ tPZL	turn-on time S _n to Y _n			35	60		75		90	ns	4.5	anembo	
tPZH/ tPZL	turn-on time	Ац	160	38	65		81 0:8		98	ns	4.5	guiascenta	
tPZH/	turn-on time S _n to Z		006	38	65		81	nav	98	ns	4.5	additional	

Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

 $GND = 0 V; t_r = t_f = 6 ns$

SYMBOL	PARAMETER	TYP.	UNIT	Vcc V	V _{is(p-p)}	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	%	4.5 9.0	4.0 8.0	$R_{L} = 10 \text{ k}\Omega$; $C_{L} = 50 \text{ pF}$ (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	4.5 9.0	4.0 8.0	$R_{\perp} = 10 \text{ k}\Omega$; $C_{\perp} = 50 \text{ pF}$ (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	4.5 9.0	note 1	$R_L = 600 \Omega$; $C_L = 50 pF$ f = 1 MHz (see Figs 11 and 15)
f _{max}	minimum frequency response (-3 dB)	90 100	MHz MHz	4.5 9.0	note 2	R _L = 50 Ω ; C _L = 10 pF (see Figs 12 and 13)
CS	maximum switch capacitance independent (Y) common (Z)	5 45	pF pF			

Notes to the AC characteristics

 V_{is} is the input voltage at Y_{in} or Z terminal, whichever is assigned as an input. V_{os} is the output voltage at Y_{in} or Z terminal, whichever is assigned as an output.

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

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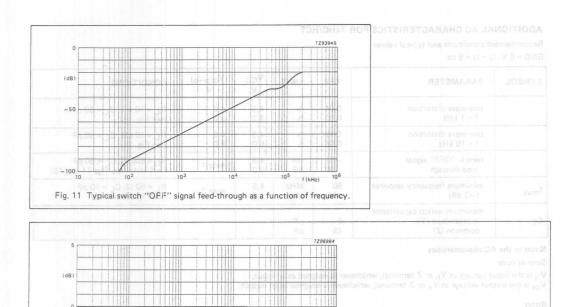
103

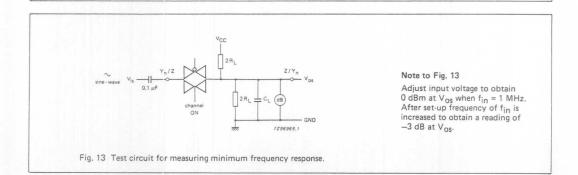
Fig. 12 Typical frequency response.

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Note to Figs 11 and 12 Test conditions:

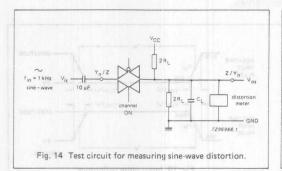
 $V_{CC} = 4.5 \text{ V; GND} = 0 \text{ V;}$ $R_L = 50 \Omega; R_{source} = 1 \text{ k}\Omega.$





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f (kHz) 10⁶



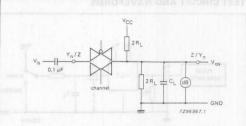
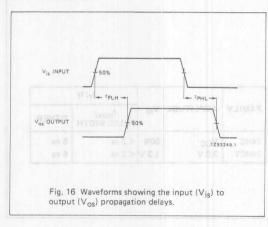
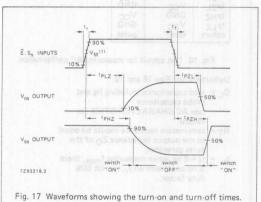


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

AC WAVEFORMS

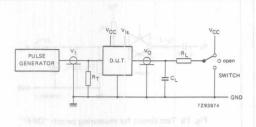




Note to Fig. 17

(1) HC : $V_M = 50\%$; $V_1 = GND$ to V_{CC} . HCT: VM = 1.3 V; VI = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS





TEST	SWITCH	Vis
^t PZH	GND	VCC
^t PZL	VCC	GND
^t PHZ	GND	VCC
^t PLZ	VCC	GND
others	open	pulse

Fig. 18 Test circuit for measuring AC performance.

Definitions for Figs 18 and 19:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for

values). R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

 $t_r = t_f = 6$ ns, when measuring f_{max} , there is no constraint on t_r , t_f with 50% duty factor.

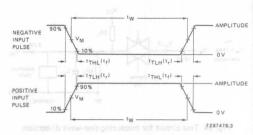


Fig. 19 Input pulse definitions.

AC WAVEFORMS

			tr; tf			
FAMILY	AMPLITUDE	VM	f _{max} ; PULSE WIDTH	OTHER		
74HC 74HCT	VCC 3.0 V		< 2 ns < 2 ns	6 ns 6 ns		

Fig. 16 Waveforms showing the input [Mig] to output (Virg) probagation delays.

Note to Fig. 17 (1) HC: $V_M = 50\%$; $V_J = 600$ to V_C

TRIPLE 3-INPUT OR GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT4075 are high-speed Si-gate CMOS devices and are pin compatible with the "4075" of the "40008" series. They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT4075 provide the 3-input OR function.

			TYF	TYPICAL		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT	
tPHL/ tPLH	propagation delay nA, nB, nC to nY	C _L = 15 pF V _{CC} = 5 V	8	10	ns	
CI	input capacitance	g vs	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	28	32	pF	

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

 $PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$ where:

f_i = input frequency in MHz f_o = output frequency in MHz CL = output load capacitance in pF
VCC = supply voltage in V

fo = output frequency in MHz VCC = supply voltage in

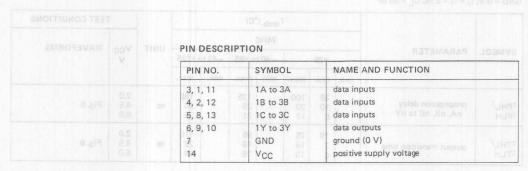
 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

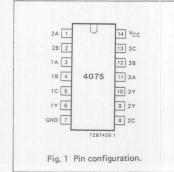
2. For HC the condition is V_I = GND to VCC DHAT HOS 2017219310 ARAHO 20

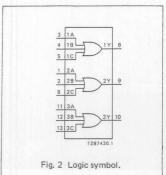
For HCT the condition is V_I = GND to VCC - 1.5 V

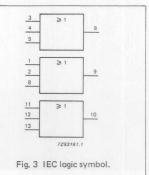
PACKAGE OUTLINES

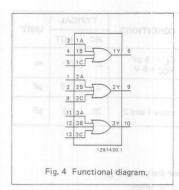
14-lead DIL; plastic (SOT27). 14-lead mini-pack; plastic (SO14; SOT108A). THE ROP SOUTZIASTON RAND DA

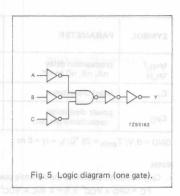












FUNCTION TABLE

	INPUTS		OUTPUT
nA	nB nC		nΥ
L	Lizo	makana	BO JARBUS
Н	X	X	Н
X	HIE	X	TANHETHET
X	X	H	o SOM Step-

H = HIGH voltage level

L = LOW voltage level

X = don't care among 350%TOH\OH&T eriT

DC CHARACTERISTICS FOR 74HC 33V of 9/02 = (ver additional error 30 V of 9/02 = (Ver a

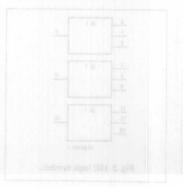
For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: SSI

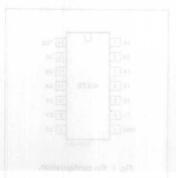
AC CHARACTERISTICS FOR 74HC | A801TO2 | M1CRI Street | M1CRI Stree

 $GND = 0 V; t_r = t_f = 6 ns; C_1 = 50 pF$

						T _{amb} (°C)					TEST CONDITIONS	
SYMBOL	PARAMETER		74HC						UNIT	Vcc	WAVEFORMS		
	MOLTOMAT		+25			-40 to +85		-40 to +125		ONT	V CC	WAVELORIVIS	
	11041301011	II IN PA	min.	typ.	max.	min.	max.	min.	max.				
tPHL/	propagation delay nA, nB, nC to nY		ni eral ni eral ni eral	28 10 8	100 20 17	2 or 31 2 or 31 2 or 31	125 25 21	12	150 30 26	ns	2.0 4.5 6.0	Fig. 6	
t _{THL} / t _{TLH}		V 0)-	o etes binuere vizisor	19 7 6	75 15 13		95 19 16	. 10	110 22 19	ns	2.0 4.5 6.0	Fig. 6	







DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC	1.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)				TEST CONDITIONS		
SYMBOL	PARAMETER				74H	т			UNIT	Vac	WAVEFORMS	
	PARAMETER		+25		-401	to +85	-40 t	o +125	ONT	V _{CC}	WAVEFORING	
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/ tPLH	propagation delay nA, nB, nC to nY		12	24		30		36	ns	4.5	Fig. 6	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 6	

AC WAVEFORMS

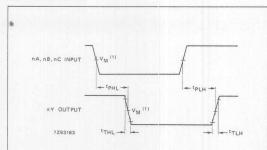


Fig. 6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

DO CHARACTERISTICS FOR 74HCT

For the DC character stars see chapter "HCMOS family characteristics", section "Family specificationis".

Ourout capability: standard

loc nampory: SSI

same TDE of an

The value of additional quiespent supply outrent (alogg) for a unit load of 1 is given in the family specifications. To determine Along ten input, multiply this value by the unit load coefficient shown in the table below,

AC CHARACTERISTICS FOR 74HCT

GMD 0 V; 1, = 1 (= 6 ns; 0) = 50 pf

AC WAVEFORMS



Fig. 6 Waveforms showing the input (nA, nB), nC) to output (nY) propagation delays and the output transition times.

fore to AC waveforms 1) HC: $V_{M} = 50\%$; $V_{1} = 600$ to V_{CC} HCT: $V_{M} = 1.3$ V; $V_{1} = 600$ to 3 V.

8-STAGE SHIFT-AND-STORE BUS REGISTER

FEATURES

- Ouput capability: standard
- ICC catagory: MSI

GENERAL DESCRIPTION

The 74HC/HCT4094 are high-speed Si-gate CMOS devices and are pin compatible with the "4094" of the "40008" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4094 are 8-stage serial shift registers having a storage latch associated with each stage for strobing data from the serial input (D) to the parallel buffered 3-state outputs (QP₀ to QP₇). The parallel outputs may be connected directly to common bus lines. Data is shifted on the positive-going clock (CP) transitions. The data in each shift register stage is transferred to the storage register when the strobe input (STR) is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) signal is HIGH.

Two serial outputs (QS_1 and QS_2) are available for cascading a number of "4094" devices. Data is available at QS_1 on the positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at QS_2 on the next negative-going clock edge and is for cascading "4094" devices when the clock rise time is slow.

APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register

		CONDITIONS	TYF	UNIT	
SYMBOL	PARAMETER	CONDITIONS	нс	19 18 21 19 86 3.5	ONT
^t PHL [/]	propagation delay CP to QS ₁ CP to QS ₂ CP to QP _n STR to QP _n	C _L = 15 pF V _{CC} = 5 V	15 13 20 18	18 21	ns ns ns ns
f _{max}	maximum clock frequency	BEAR	95	86	MHz
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	83	92	pF

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

f_i = input frequency in MHz f_o = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_CC

For HCT the condition is V_I = GND to V_CC – 1.5 V

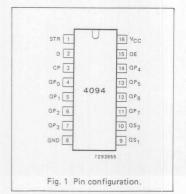
PACKAGE OUTLINES

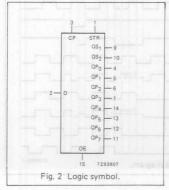
16-lead DIL; plastic (SOT38Z).

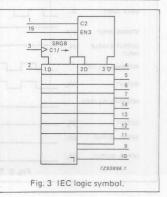
16-lead mini-pack; plastic (SO16; SOT109A).

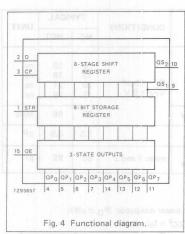
PIN DESCRIPTION

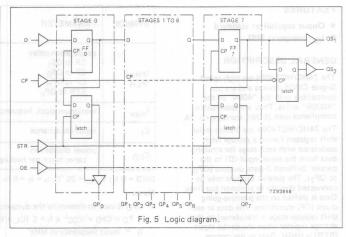
PIN NO.	SYMBOL	NAME AND FUNCTION
1	STR	strobe input
3	D CP	serial input clock input
4, 5, 6, 7, 14, 13, 12, 11	QP ₀ to QP ₇	parallel outputs
8	GND	ground (0 V) househart 50 Woulde Hold = 1
9, 10	QS ₁ , QS ₂	serial outputs output enable input
16	Vcc	positive supply voltage







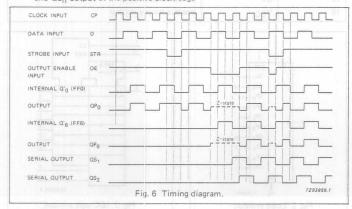




FUNCTION TABLE

	INP	UTS		PARA		SERIAL OUTPUTS		
СР	OE	STR	D	QP ₀	QPn	QS ₁	QS ₂	
1	L	X	X	Z	Z (08)	0'6	NC	
1	L	X	X	101Z08:8	Z	NC	QP7	
1	Н	L	X	NC	NC	Q'6	NC	
†	Н	Н	L	L	QP _{n-1}	0'6	NC	
1	Н	и Нетом	H	HAZH.	QPn-1	0'6	NC	
+	Н	Н	Н	NC	NC	NC	QP7	

- = HIGH voltage level
- = LOW voltage level
- = don't care
- = high impedance OFF-state
- NC = no change
- = LOW-to-HIGH CP transition (V D) Dhuoxp
- = HIGH-to-LOW CP transition
- Q'6 = the information in the seventh register stage is transferred to the 8th register stage and QSn output at the positive clock edge





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	4.5 Fig. 10 6.0	T _{amb} (°C)								TEST CONDITIONS		
SYMBOL PARAM		74HC										
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
	2.0	min.	typ.	max.	min.	max.	min.	max.		antion of	and the comment of th	
tPHL/	propagation delay CP to QS ₁		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
t _{PHL} /	propagation delay CP to QS ₂	iticequ	44 16 13	135 27 23	pec ,"ex	170 34 29	nsrlo y	205 41 35	ns	2.0 4.5 6.0	Fig. 7	
t _{PHL} /	propagation delay CP to QP _n		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 7	
t _{PHL} /	propagation delay STR to QP _n	imat e	58 21 17	180 36 31	t to bar	225 45 38	c) for i	270 54 46	ns	2.0 4.5 6.0	Fig. 8	
^t PZH [/]	3-state output enable time OE to QP _n		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9	
^t PHZ [/] ^t PLZ	3-state output disable time OE to QP _n		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 9	
^t THL [/] ^t TLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5	Fig. 7	
tw	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
tw	strobe pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	
^t su	set-up time D to CP	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10	
t _{su}	set-up time CP to STR	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8	

AC CHARACTERISTICS FOR 74HC (Continued)

	cations".	Tamb (°C) STANDER VILLES CO. 74HC								TEST CONDITIONS		
	DADAMETER										utput capability; standard	
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			0 ten 8 = 17 = 17 t	
t _h SVIC	hold time D to CP	3 3 3	-6 -2 -2		3 3 3	urus ^T	3 3 3		ns	2.0 4.5 6.0	Fig. 10	
th	hold time CP to STR	0 0	-14 -5 -4	5 -4	0 0 0	\$	0 0	£+	ns	2.0 4.5 6.0	Fig. 8	JOBMY
f _{max}	maximum clock pulse frequency	6.0 30 35	28 87 103	tim ,	4.8 24 28	sizn .	4.0 20 24	in. typ	MHz	2.0 4.5 6.0	Fig. 7	Vines

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

		0.0						
INPUT	UNIT LOA	ENT						
OE, CP D STR	1.50 0.40 1.00	2.0 4.5 6.0						

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

SYMBOL	PARAMETER				T _{amb} (°C)	-(17	TEST CONDITIONS			
		(1)(0)	7	TURNI	74HC	Т		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	Water Toront		
		+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/	propagation delay CP to QS ₁	\	23	39	d .	49		59	ns	4.5	Fig. 7
tPHL/ tPLH	propagation delay CP to QS ₂		21	36		45		54	ns	4.5	Fig. 7
t _{PHL} /	propagation delay CP to QP _n		25	43		54	H	65	ns	4.5	Fig. 7
tPHL/ tPLH	propagation delay STR to QP _n		22	39		49	95	59	ns	4.5	Fig. 8
t _{PZH} /	3-state output enable time OE to QP _n	in and th and	20	35		44		53	ns ma	4.5	Fig. 9
t _{PHZ} /	3-state output disable time OE to QP _n		21	35		44		53	ns	4.5	Fig. 9
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 7
tw	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 7
tW	strobe pulse width HIGH	16	5	11901 92	20		24	10-1597	ns	4.5	Fig. 8
t _{su}	set-up time D to CP	10	4		13		15	w/	ns	4.5	Fig. 10
t _{su}	set-up time CP to STR	20	9		25		30) 	ns	4.5	Fig. 8
^t h	hold time D to CP	4	0	p., co., w	4		4		ns	4.5	Fig. 10
t _h resease	hold time CP to STR	0	-4		0		0		ns	4.5	Fig. 8
f _{max}	maximum clock pulse frequency	30	80		24		20	fané sna	MHz	4.5	Fig. 7

AC WAVEFORMS

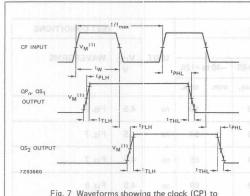


Fig. 7 Waveforms showing the clock (CP) to output (ΩP_n , ΩS_1 , ΩS_2) propagation delays, the clock pulse width and the maximum clock frequency.



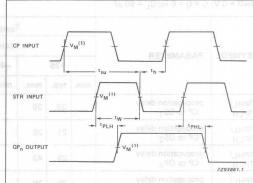


Fig. 8 Waveforms showing the strobe (STR) to output (QPn) propagation delays and the strobe pulse width and the clock set-up and hold times for the strobe input.

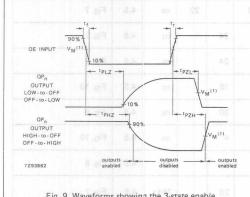
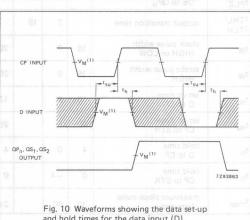


Fig. 9 Waveforms showing the 3-state enable and disable times for input OE.



and hold times for the data input (D).

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_1 = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Note to Fig. 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

QUAD BILATERAL SWITCHES

FEATURES

- Low "ON" resistance: 160 Ω (typ.) at $V_{CC} - V_{EE} = 4.5 \text{ V}$ 120 Ω (typ.) at $V_{CC} - V_{EE} = 6.0 \text{ V}$ 80 Ω (typ.) at $V_{CC} - V_{EE} = 9.0 \text{ V}$
- Logic level translation: to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4316 are high-speed Si-gate CMOS devices.
They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4316 have four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH select input (nS). When the enable input (E) is HIGH, all four analog switches are turned off.

Current through a switch will not cause additional V_{CC} current provided the voltage at the terminals of the switch is maintained within the supply voltage range; V_{CC} \gg (V γ , V $_Z$) \gg V_{EE}. Inputs nY and nZ are electrically equivalent terminals.

 V_{CC} and GND are the supply voltage pins for the digital control inputs (\overline{E} and nS). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC}-V_{EE}$ may not exceed 10.0 V. See the "4016" for the version without

logic level translation.

01/11001		CONDITIONS	TYF	ICAL	G MIS
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
^t PZH	turn "ON" time E to V _{os} nS to V _{os}		40	19 17	ns ns
^t PZL	turn "ON" time E to Vos nS to Vos	$R_1 = 1 k\Omega$	19 16	24 21	ns ns
^t PHZ [/] ^t PLZ	turn "OFF" time E to V _{os} nS to V _{os}	2 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	20 16	21 19	ns ns
Ci	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per switch	notes 1 and 2	13	14	pF
CS	max. switch capacitance		5	5	pF

 $V_{EE} = GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

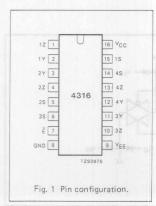
1. CPD is used to determine the dynamic power dissipation (PD in μ W):

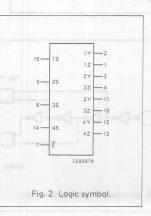
$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$$
 where:

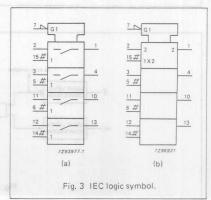
- $f_1 = \text{input frequency in MHz}$ $C_1 = \text{output}$
 - C_L = output load capacitance in pF C_S = max. switch capacitance in pF
- f_{o}^{\prime} = output frequency in MHz C_{S}^{\prime} = max. switch capacite $\Sigma \left\{ \left(C_{L} + C_{S} \right) \times V_{CC}^{2} \times f_{o} \right\} = \text{sum of outputs}$ V_{CC} = supply voltage in V
- 2. For HC the condition is V $_{I}$ = GND to V $_{CC}$ For HCT the condition is V $_{I}$ = GND to V $_{CC}$ 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z). 16-lead mini-pack; plastic (SO16; SOT109A).







PIN DESCRIPTION NAME AND FUNCTION SYMBOL PIN NO. independent inputs/outputs 1Z to 4Z 1, 4, 10, 13 independent inputs/outputs 1Y to 4Y 2, 3, 11, 12 Ē enable input (active LOW) 7 ground (0 V) GND 9 VEE negative supply voltage 15, 5, 6, 14 1S to 4S select inputs (active HIGH) positive supply voltage 16 VCC

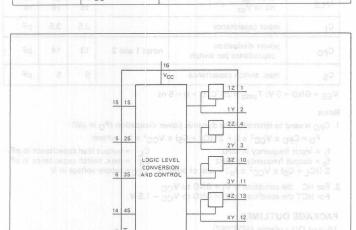


Fig. 4 Functional diagram.

VEE

7Z93978

GND

FUNCTION TABLE

INP	UTS	
0.8E-33	nS V	120 D (syp.) s
F = 310	- DOV II	off
esimbinano	ogid to c	on no or
H 2	X	off

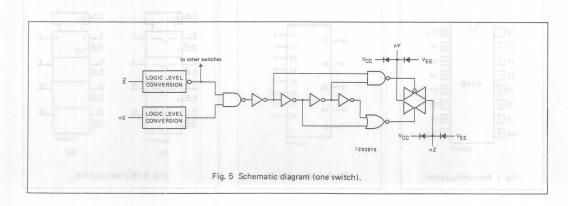
- H = HIGH voltage level 1980 300000 ...
- L = LOW voltage level vicepose 30
- X = don't care

APPLICATIONS

- Signal gating
- Modulation
- Demodulation
- Chopper

The digital control inputs (E and nS), the V_{CC} to GND ranges are 2.0 to 10.0 V or HCT.

an swing between Vocas a positive limit. CC – VEE may not exceed 10.0 V.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to VEE = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
Vcc	DC supply voltage	-0.5	+11.0	V	
±IIK	DC digital input diocle current		20	mA	for $V_1 < -0.5 \text{ V or } V_1 > V_{CC} + 0.5 \text{ V}$
±ISK	DC switch diode current		20	mA	for $V_S < -0.5 \text{ V}$ or $V_S > V_{CC} + 0.5 \text{ V}$
±IS	DC switch current		25	mA	for -0.5 V < V _S < V _{CC} + 0.5 V
±1EE	DC V _{EE} current		20	mA	
±I _{CC} ; ±I _{GND}	DC V _{CC} or GND current		50	mA	0(8 0 2 0 B
T _{stg}	storage temperature range	-65	+150	°C	
P _{tot}	power dissipation per package	Fig. 7 C supply v			for temperature range: -40 to +125 °C as a 2 74HC/HCT
	plastic DIL	-	750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SC)		500	mW	above +70 °C; derate linearly with 8 mW/K
Ps	power dissipation per switch		100	mW	4HC Ven - 6ND or Ven - Ves = 2.0, 4.5; 6.0 at

Note to ratings

To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Y_n , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminal Y_n . In this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or V_{EE} .

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	8	74HC	290	98	74HC1			001101710110	
OTIMBOL	COL OF OR OTHER	min.	typ.	max.	min.	typ.	max.	UNIT	CONDITIONS	
VCC	DC supply voltage V _{CC} -GND	2.0	5.0	10.0	4.5	5.0	5.5	V earn	see Figs 6 and 7	
Vcc	DC supply voltage V _{CC} -V _{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7	
VI	DC input voltage range	GND	5	VCC	GND		Vcc	٧		
Vs	DC switch voltage range	VEE	2	Vcc	VEE		Vcc	V	RESTRUCTION NOT	
T _{amb}	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC	
T _{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	CHARACTERISTICS	
t _r , t _f	input rise and fall times	180	6.0	1000 500 400 250	8	6.0	500	ns	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V V _{CC} = 10.0 V	

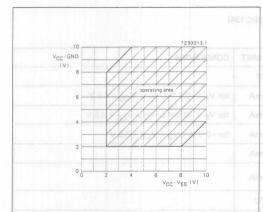


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4316.

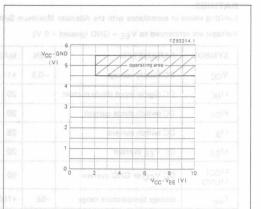


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4316.

Ω

Ω

4.5 0

6.0

4.5

-4.5

to or

VEE VIL

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} - GND or V_{CC} - V_{EE} = 2.0, 4.5, 6.0 and 9.0 V For 74HCT: V_{CC} - GND = 4.5 and 5.5 V; V_{CC} - V_{EE} = 2.0, 4.5, 6.0 and 9.0 V

Tamb (°C) TEST CONDITIONS 74HC/HCT SYMBOL PARAMETER UNIT VEE VI Vcc Vis Is +25 -40 to +85 -40 to +125 V V μΑ min. typ. max. min. max. min. max. 2.0 0 0 100 VCC VIH 160 320 400 480 Ω 4.5 1000 ON resistance (peak) RON to 0 6.0 120 240 300 360 Ω VEE VIL 85 170 215 255 Ω 4.5 -4.5 1000 160 Ω 2.0 0 100 V_{1H} 240 160 200 Ω 80 4.5 0 1000 ON resistance (rail) VEE or RON 2 0 70 140 175 210 6.0 1000 VIL 60 120 150 180 Ω 4.5 -4.5 1000 170 Ω 100 VIH 90 180 225 270 Ω 4.5 0 1000 RON ON resistance (rail) VCC 240 Ω 0 80 160 200 6.0 1000 VIL 65 135 170 205 Ω 4.5 -4.5 1000 Ω 2.0 Vcc VIH

Notes to DC characteristics

ARON

1. At supply voltages (V_{CC} - V_{E(E)}) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

16

9

2. For test circuit measuring RON see Fig. 8.

maximum $\triangle ON$ resistance

between any two channels

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

	аиоз тват				T _{amb} (°C)	-11				TEST	COND	ITIONS
0./140.01		74HC								.,		N/I A S	OTHER
SYMBOL	PARAMETER	25 +25		- 88+	-40 to +85		-40 to +125		UNIT	VCC	VEE	VI	OTHER
		min.	typ.	max.	min.	max.	min.	max.					
VIH (81)	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.3	0 0 0	1.5 3.15 4.2 6.3	0 0 0	1.5 3.15 4.2 6.3		v	2.0 4.5 6.0 9.0	1	propag Vi _s to	(BFTH)
VILC SI S	LOW level input voltage	310 62 83 86	0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	1 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1	0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0	ac'		728 ₅ /H285
kΩ;) pF t± s 19, 20	input leakage current	265 53 45		0.1 0.2		1.0	6 8 8	1.0 2.0	μА	6.0 10.0	0	V _{CC} or GND	124) /H241
±Is sox	analog switch OFF-state current	330		0.1		1.0 00	2 2	1.0	μА	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} - V _{EE} (see Fig. 10)
±1s	analog switch ON-state current	56 59 265		0.1	in in	1.0	1 2	1.0	μА	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} - V _{EE} (see Fig. 11)
lcc and	quiescent supply current	53 46 54		8.0 16.0	104	80.0 160.0	0 8 8	160.0 320.0	μΑ	6.0	0	V _{CC} or GND	V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V; } t_r = t_f = 6 \text{ ns; } C_L = 50 \text{ pF}$

DC CHARACTERISTICS FOR 74HC

	TEST CONDIT					T _{amb} (°C)					TEST	CONDITIONS
01/11/01						74HC	:			V	OTHER JOHNYS		
SYMBOL	PARAMETER		125	+25	- 284	-40	to +85	-40 to	+125	UNIT	V CC	VEE	OTHER MANY
			min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay V _{is} to V _{os}	v		17 6 5 4	60 12 10 8	15 1.15 1.2 1.2	75 15 13 10	11,2 2,4 3,2 4,3	90 18 15	nsgari	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = ∞; C _L = 50 pF (see Fig. 18)
^t PZH [/] ^t PZL	turn "ON" time E to V _{OS}	V	3.5 1.35 1.8	61 22 18 19	205 41 35 37		255 51 43 47	0.8 0 2.1 2.8 4.3	310 62 53 56	ns opes	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 19, 20 and 21)
t _{PZH} / t _{PZL}	turn "ON" time nS to V _{OS}	Aug	0.1	52 19 15 17	175 35 30 34		220 44 37 43	0	265 53 45 51	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 19, 20 and 21)
^t PHZ/ ^t PLZ	turn "OFF" time E to V _{OS}	Au	0.1	63 23 18 21	220 44 37 39		275 55 47 49	0	330 66 56 59	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 19, 20 and 21)
^t PHZ/ ^t PLZ	turn "OFF" time nS to V _{OS}	Au	60.08	55 20 16 18	175 35 30 36	6	220 44 37 45		265 53 45 54	ns	2.0 4.5 6.0 4.5	0 0 0 - 4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 19, 20 and 21)

DC CHARACTERISTICS FOR 74HCT

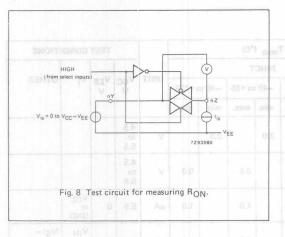
Voltages are referenced to GND (ground = 0)

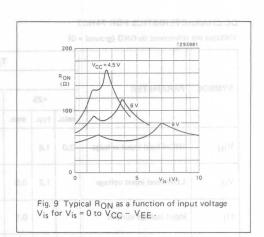
	WEAR-OF				T _{amb}	(°C)				TEST CONDITIONS			
SYMBOL	A CANALATED A	74HCT								1,	.,	HER MAINTENANT	OTHER
STWIBOL	PARAMETER	-	+25		-40 to +85		-40 t	o +125	UNIT	v _{CC}	VEE	VI	OTHER
		min.	typ.	max.	min.	max.	min.	max.					Onetic V
>-							7	-		4.5	1		
VIH	HIGH level input voltage	2.0	1.6		2.0	33	2.0	417	V	to 5.5			
VIL	LOW level input voltage	0	1.2	0.8		0.8		0.8	v	4.5 to 5.5			
sgnAlov 31 ±1 ₁		Typi V V ₁₉	Vis fi	0.1		1.0	V	1.0	μА	5.5	0	VCC or GND	
±IS	analog switch OFF-state current			0.1		1.0		1.0	μА	10.0	0	VIH or VIL	VS = VCC - VE (see Fig. 10
±IS	analog switch ON-state current			0.1	-o<1	1.0		1.0	μА	10.0	0	V _{IH} or V _{IL}	IV _S I = V _{CC} - V _E (see Fig. 11
¹ cc	quiescent supply current	-0-	30	8.0 16.0		80.0 160.0	88 88 81	160.0 320.0	μΑ	5.5 5.0	0 -5.0	V _{CC} or GND	V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}
∆Icc	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)	CSP 183 Y	100	360		450		490	μΑ	4.5 to 5.5	0	V _{CC} -2.1V	other input at V _{CC} or GND

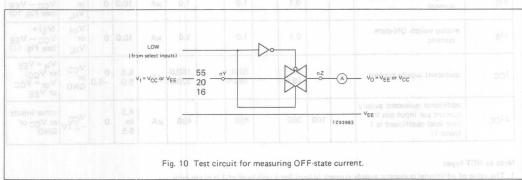
Note to HCT types

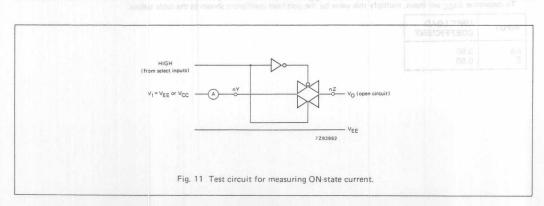
1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nS	0.50
E	0.50









AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

					T _{amb} (°C)				TEST CONDITIONS			
SYMBOL	PARAMETER	(d-distance		74HC	TIME	29V2		UNIT	VCC	VEE	OTHER		
	08 = 10 (Ω4 01 = yR	+25		-40	to +85	-40 to +125			V	V			
	(see Fig. 14)	min.	typ.	max.	min.	max.	min.	max.			sHal	1 = 1	
tPHL/	propagation delay V _{is} to V _{os}	0.8	6 4	12 8	4.5	15 10	1.20	18 12	ns	4.5 4.5	0 -4.5	R _L = ∞; C _L = 50 pF (see Fig. 18)	
^t PZH	turn "ON" time E to Vos	T stor	22 21	44 42	4,5	55 53	-80	66 63	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$	
^t PZL	turn "ON" time E to Vos	1 9301	28 21	56 42	8.1	70 53	38-	84 63	ns	4.5 4.5	0 -4.5	(see Figs 19, 20 and 21)	
tPZH aa	turn "ON" time nS to V _{os}		20 17	40 34	2.0	53 43	- 01	60 51	ns	4.5 4.5	0 -4.5	O - 30 Pi	
^t PZL	turn "ON" time nS to V _{os}		25 17	50 34	0.0	63 43		75 51	ns	4.5 4.5	0 -4.5	(see Figs 19, 20 and 21)	
^t PHZ/ ^t PLZ	turn "OFF" time E to V _{os}	note 2	25 23	50 46	2.2	63 58	08	75 69	ns	4.5 4.5	0 - 4.5		
^t PHZ/ ^t PLZ	turn "OFF" time nS to V _{OS}		22 20	44 40	na bam	55 50	marini e	66 60	ns	4.5 4.5	0	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Figs 19, 20 and 21)	

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	Vcc V	V _{EE}	V _{is(p-p)}	CONDITIONS	and a
	sine-wave distortion f = 1 kHz	0.80 0.40	%	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10 \text{ k}\Omega; C_L = 50 \text{ pF}$ (see Fig. 14)	
9q 00 = 30 pP	sine-wave distortion f = 10 kHz	2.40 1.20	% 31	2.25 4.5	- 2.25 - 4.5	4.0 8.0	$R_L = 10 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig. 14)	UH9
:DH	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600 \Omega$; $C_L = 50 pF$ (see Figs 12 and 15)	Hild
0 pe 9s 18, 26	crosstalk between any two switches	-60 -60	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600 \Omega$; $C_L = 50 pF$; $f = 1 MHz$; (see Fig. 16)	i o h
V _(p-p) = 0	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5		$R_L = 600 \Omega$; $C_L = 50 pF$; f = 1 MHz (E or nS, square-wave between V_{CC} and GND , $t_r = t_f = 6 ns$) (see Fig. 17)	HZ9
f _{max}	minimum frequency response (-3 dB)	150 160	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	R _L = 50 Ω; C _L = 10 pF (see Figs 13 and 14)	leus.
CS	maximum switch capacitance	5	pF		04 - SS		E to Vos	2.19

Notes to AC characteristics

Vis is the input voltage at an nY or nZ terminal, whichever is assigned as an input. Vos is the output voltage at an nY or nZ terminal, whichever is assigned as an output.

- 1. Adjust input voltage $\rm V_{is}$ to 0 dBrn level (0 dBm = 1 mW into 600 $\Omega),$ 2. Adjust input voltage $\rm V_{is}$ to 0 dBrn level at $\rm V_{OS}$ for 1 MHz (0 dBm = 1 mW into 50 $\Omega).$

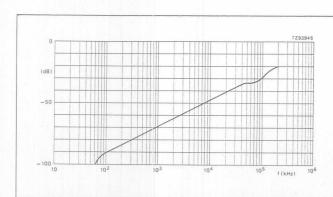
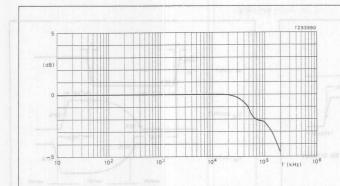


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions: $\begin{aligned} &V_{CC} = 4.5 \text{ V; GND} = 0 \text{ V; V}_{EE} = -4.5 \text{ V;} \\ &R_L = 50 \text{ }\Omega; \text{ }R_{Source} = 1 \text{ }k\Omega. \end{aligned}$

Fig. 13 Typical frequency response.

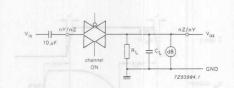


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

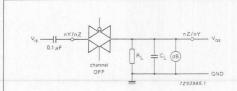
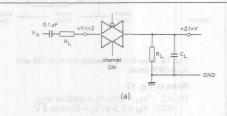


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.



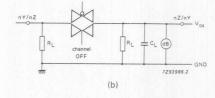


Fig. 16 Test circuit for measuring crosstalk between any two switches. (a) channel ON condition; (b) channel OFF condition.

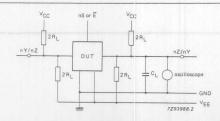
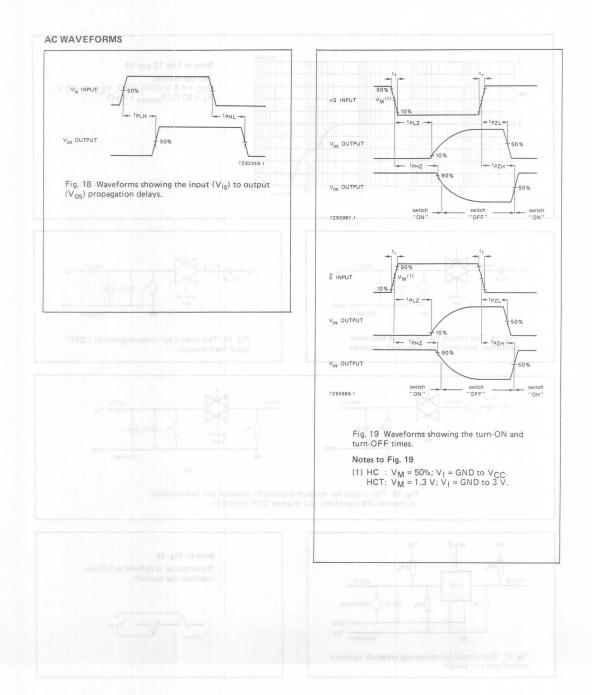


Fig. 17 Test circuit for measuring crosstalk between control and any switch.

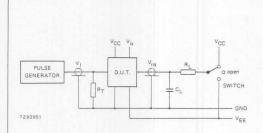
Note to Fig. 17

The crosstalk is defined as follows (oscilloscope output):





TEST CIRCUIT AND WAVEFORMS



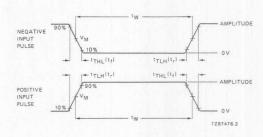


Fig. 20 Test circuit for measuring AC performance.

Fig. 21 Input pulse definitions.

Conditions

TEST	SWITCH	Vis
tPZH tPZL tPHZ tPLZ others	VEE VCC VEE VCC open	VCC VEE VCC VEE

			t _r ; t _f				
FAMILY	AMPLITUDE	VM	f _{max} ; PULSE WIDTH	OTHER			
74HC	Vcc	50%	< 2 ns	6 ns			
74HCT	3.0 V	1.3 V	< 2 ns	6 ns			

Definitions for Figs 20 and 21:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

 $t_r = t_f = 6$ ns; when measuring t_{max} , there is no constraint on t_r , t_f with 50% duty factor.

TEST CIRCUIT AND WAVEFORMS

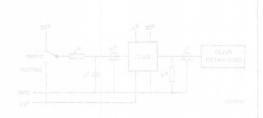


Fig. 20 Test orguit for measuring AC performance.



Fig. 21 Input pulse definitions.

Conditions

Definitions for Figs 20 and 21

- Ct = load capacitance including jie and probe capacitance (see AC CHARACTERISTICS for
- RT = termination resistance should be equal to the output impedance Z_Q of the output impedance Z_Q of the
- ty = 6 as; when measuring f_{max}, there
 is no constraint on t_r, t_f with 50%
 dusy factor.

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH LATCH

FEATURES TO ROSE LARBUED

- Wide analog input voltage range: ± 5 V
- Low "ON" resistance: 80 Ω (typ.) at V_{CC} - V_{EE} = 4.5 V 70 Ω (typ.) at V_{CC} - V_{EE} = 6.0 V 60 Ω (typ.) at V_{CC} - V_{EE} = 9.0 V
- Logic level translation: to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Address latches provided
- · Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4351 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4351 are 8-channel analog multiplexers/demultiplexers with three select inputs (S₀ to S₂), two enable inputs (E₁ and E₂), a latch enable input (LE), eight independent inputs/outputs (Yo to Y7) and a common input/output (Z).

With $\overline{\mathsf{E}}_1$ LOW and E_2 is HIGH, one of the eight switches is selected (low impedance ON-state) by S₀ to S₂. The data at the select inputs may be latched by using the active LOW latch enable input (LE). When LE is HIGH the latch is transparent. When either of the two enable inputs, E₁ (active LOW) and E₂ (active HIGH), is inactive, all 8 analog switches are turned off.

(continued on next page)

avuspa.	BADAMETED.		TY	PIN DI	
SYMBOL	PARAMETER MOLTOMUS SWA	CONDITIONS	нс	нст	UNIT
t _{PZH} /	turn "ON" time \overline{E}_1 , E_2 or S_n to V_{os}	C _L = 15 pF	27	35	ns
t _{PHZ} / t _{PLZ}	turn "OFF" time E ₁ , E ₂ or S _n to V _{os}	$R_L = 1 k\Omega$ $V_{CC} = 5 V$	21	23	ns 🖁
CI	input capacitance	ne la caractería	3.5	3.5	pF
CPD	power dissipation capacitance per switch	notes 1 and 2	25	25	pF
CS	max. switch capacitance independent (Y) common (Z)	on YY of	5 25	5 25	pF pF

$$V_{EE} = GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

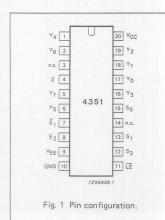
$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$$
 where:

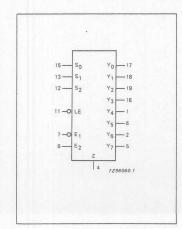
CL = output load capacitance in pF CS = max. switch capacitance in pF f_o = output frequency in MHz C_S = max, switch capacite $\Sigma ((C_L + C_S) \times V_{CC}^2 \times f_o)$ = sum of outputs V_{CC} = supply voltage in V

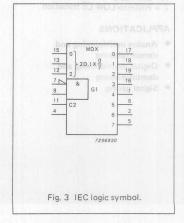
2. For HC
$$\,$$
 the condition is V $_{I}$ = GND to V $_{CC}$ $\,$ For HCT the condition is V $_{I}$ = GND to V $_{CC}$ $-$ 1.5 V

PACKAGE OUTLINES

20-lead DIL; plastic (SOT146) 20-lead mini-pack; plastic (SO20; SOT163A).







BOTAL HTM REXEMBERING MULTIPLEXER/DEMULTIPLEXER WITH LATCH

PIN NO.	SYMBOL	NAME AND FUNCTION	
4 3, 14	Z n.c. 3681	110 C COITH CC CCC	
7 8 an 55	E ₁		
9	V _{EE} GND	negative supply voltage ground (0 V)	
11 15, 13, 12	S ₀ to S ₂	latch enable input (active LOW)	
17, 18, 19, 16, 1, 6, 2, 5 20	Y ₀ to Y ₇	independent inputs/outputs positive supply voltage	

FUNCTION TABLE

		INP	UTS		D. L.	CHANNEL	iotes
Ē ₁	E ₂	LE	s ₂	s ₁	s ₀	ON	. Сро із úsad to dater Ро = Сро х Усс
H X	X	×	X	×	×	none	f = input frequency fo = output frequency Z ((C) * Ce) x V _{ch} :
	H H H	H H H	L	L a L H H	L	Y ₀ Y ₁ Y ₂	For HC. The condition HCT the condu-
	Н Н Н	H H H	H H H	L AA L H H	Ea _H TO L H	TAIL LANGE	0-lead DLL; plastit (0-lead mini-pack; pk
L X	H X	L ↓	X	X	×	*	

* Last selected channel "ON".

** Selected channels latched.

- H = HIGH voltage level
- L = LOW voltage level
- X = don't care
- ↓ = HIGH-to-LOW LE transition

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

GENERAL DESCRIPTION

 V_{CC} and GND are the supply voltage pins for the digital control inputs (S0 to S2, $\overline{LE},\,\overline{E}_1$ and E_2). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (Y_0 to Y_7 , and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC}-V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, VEE is connected to GND (typically ground).

GENERAL DESCRIPTION

The /AHC/HCT4051 are high-speed Si-gate CMOS devicer. They are specified in compliance with LEDEC translated on The /AHC/HCT4051 are 8-channel analog unitriblexic rudemultipissers with three

select inputs (Sg to Sg), two anable inputs [E] and Eg], a latch enable input [TE], each first-grandent input-Natiguts (Yg to approximately).

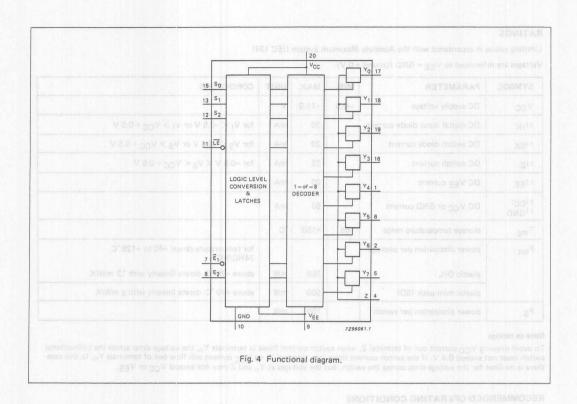
With E₃ LOW and E₂ is rHGH, one of the eight are tenes is selected (low impedance ON-state) by Sq to S₂. The data at the

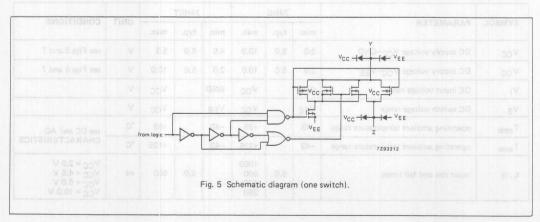
sensor inquits may be incohed by using ma occive LOW latch enable inquit (LE). When LE is HIGH the latch is transparent. When sither of the two enable inputs.

Fr (active LOW) and Ep (active HIGH), is inactive, all 8 analog switches are burned off.









RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to VEE = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
Vcc	DC supply voltage	-0.5	+11.0	V	7 m m
±11K	DC digital input diode current		20	mA	for $V_1 < -0.5 \text{ V}$ or $V_1 > V_{CC} + 0.5 \text{ V}$
±1SK	DC switch diode current		20	mA	for $V_S < -0.5 \text{ V}$ or $V_S > V_{CC} + 0.5 \text{ V}$
±IS	DC switch current		25	mA	for $-0.5 \text{ V} < \text{V}_{\text{S}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$
±1EE	DC VEE current		20	mA	v83.00002 188aveido
±1CC; ±1GND	DC V _{CC} or GND current	H	50	mA	SHOTAJ
T _{stg}	storage temperature range	-65	+150	°C	
P _{tot}	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
Ps	power dissipation per switch		100	mW	QUO.

Note to ratings

To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Y_{n} , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Y_{n} . In this case there is no limit for the voltage drop across the switch, but the voltages at Y_{n} and Z may not exceed V_{CC} or V_{EE} .

RECOMMENDED OPERATING CONDITIONS

			74HC			74HC	г		
SYMBOL	PARAMETER	min.	typ.	max.	min.	typ.	max.	UNIT	CONDITIONS
Vcc	DC supply voltage V _{CC} -GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
Vcc	DC supply voltage V _{CC} -V _{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
VI	DC input voltage range	GND		VCC	GND		Vcc	V	
٧s	DC switch voltage range	VEE		Vcc	VEE		Vcc	V	
T _{amb}	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC
T _{amb}	operating ambient temperature range	-40	0	+125	-40		+125	°C	CHARACTERISTICS
t _r , t _f	input rise and fall times	eno) n	6.0	1000 500 400 250	Fg. 5 S	6.0	500	ns	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V V _{CC} = 10.0 V

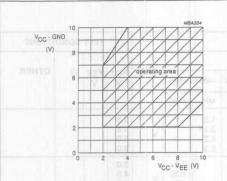


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4351.

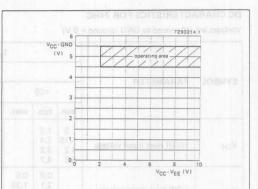


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4351.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} – GND or V_{CC} – V_{EE} =2.0, 4.5, 6.0 and 9.0 V For 74HCT: V_{CC} – GND =4.5 and 5.5 V; V_{CC} – V_{EE} =2.0, 4.5, 6.0 and 9.0 V

see Fig. 10)					T _{amb} (°C)				TEST CONDITIONS					
SYMBOL	PARAMETER	74HC/HCT AG							UNIT	из-ИО	ripties	golen		W. SI	
F1 1 Box 201	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	VEE	IS μA	Vis	VI	
SA A SE	95V 0 0.8	min.	min. typ. max. min. max. min.		max.		to move to								
RON	ON resistance (rail)	2.0.0	100 90 70	- 180 160 130		- 225 200 165		- 270 240 195	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	VCC to VEE	VIN or VIL	
R _{ON}	ON resistance (rail)		150 80 70 60	- 140 120 105		- 175 150 130		210 180 160	ΩΩΩ	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	VEE	VIH or VIL	
R _{ON}	ON resistance (rail)		150 90 80 65	- 160 140 120		_ 200 175 150		- 240 210 180	Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	Vcc	VIH or VIL	
ΔRON	maximum △ON resistance between any two channels		9 8 6						ΩΩΩ	2.0 4.5 6.0 4.5	0 0 0 -4.5		V _{CC} to V _{EE}	VIH or VIL	

Notes to DC characteristics

At supply voltages (V_{CC} - V_{EE}) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
 For test circuit measuring R_{ON} see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

	3					Ha Iv	No.	1	T _{amb}	(°C)	1	M	1	M	TEST	COND	ITIONS
CVMDO		DADAA	AFTER						74H	C		M	UNIT	Vac	VEE	Vı	OTHER
SYMBO	JL	PARAM	METER				+25		-40	to +85	-40 t	o +125	ONT	V _{CC}	V	V.1	OTHER
	1					min.	typ.	max.	min.	max.	min.	max.					
VIH		HIGHI	evel inp	ut volta	ge	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0		2	
V _{IL}		LOW le	vel inpu			Sua 1	0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	tion o	0.5 1.35 1.8 2.7	V V MCA351	2.0 4.5 6.0 9.0	basın zanati	Suara	Fig. 6
±II		input le	eakage c	urrent				0.1		1.0		1.0 2.0	μА	6.0	0	V _{CC} or GND	
±IS		analog :	switch C it per ch		e			0.1	4.0	1.0		1.0	μΑ	10.0	0	V _{IH} or V _{IL}	IV _S I = V _{CC} - V _E I (see Fig. 10
±IS	HOLK	analog s	switch C		e			0.4	(C)	4.0	+ 33 V	4.0	μΑ	10.0	0	V _{IH} or V _{IL}	IV _S I = V _{CC} - V _E I (see Fig. 10
±IS	ei V	analog s	switch C			740 1	s de fill	0.4	TOHIO	4.0	RE	4.0	μА	10.0	0	V _{IH} or V _{IL}	IV _S I = V _{CC} - V _{EI} (see Fig. 11
lcc		quiesce	nt suppl	y curre	nt 🔐	.2050	1 .0	8.0	in ni	80.0 160.0	m .g	160.0 320.0	μА	6.0	0	VCC or GND	V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}
	BBV VEE	1000	0 -4.5	4.5 8.0 4.5	0 0	99			22 26 26 16			18		(ligy)	apner	sim H	иог
					2002												

AC CHARACTERISTICS FOR 74HC GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

	TEST COND				(5	T _{amb} (°C)				TEST CONDITIONS			
SYMBOL	DADAMETED					74H0	2			UNIT	Van	\/	OTHER	
SAIMBOL	PARAMETER		+125	+25	C8+ c	-40 t	to +85	-40 to	+125	OWIT	VCC	VEE	OTHER	
			min.	typ.	max.	min.	max.	min.	max.					
^t PHL/ ^t PLH	propagation delay V _{is} to V _{OS}	V		14 5 4 4	60 12 10 8	2.0	75 15 13 10	8.1	90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = ∞; C _L = 50 pF (see Fig. 17)	
^t PZH [/] ^t PZL	turn "ON" time E ₁ to V _{os}	v	0.8	85 31 25 28	300 60 51 55		375 75 64 69	1.2	450 90 77 83	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Fig. 18)	
t _{PZH} /	turn "ON" time E ₂ to V _{os}	Ag	0.1	85 31 25 25	300 60 51 55		375 75 64 69		450 90 77 83	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = 1 k Ω ; C _L = 50 pF (see Fig. 18)	
^t PZH [/]	turn "ON" time LE to V _{os}	Au	4.0	91 33 26 27	300 60 51 55		375 75 64 69		450 90 77 83	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Fig. 18)	
t _{PZH} / t _{PZL}	turn "ON" time S _n to V _{os}	Asq	4,0	88 32 26 25	300 60 51 50		375 75 64 63		450 90 77 75	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Fig. 18)	
^t PHZ [/]	turn "OFF" time E ₁ to V _{os}	Au	160.0	69 25 20 20	250 50 43 40		315 63 54 50		375 75 64 60	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 18)	
^t PHZ [/] ^t PLZ	turn "OFF" time E ₂ to V _{os}	Au	490	72 26 21 19	250 50 43 40		315 63 54 50	190	375 75 64 60	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_{\perp} = 1 \text{ k}\Omega;$ $C_{\perp} = 50 \text{ pF}$ (see Fig. 18)	
^t PHZ [/] ^t PLZ	turn "OFF" time LE to Vos	i elder e	aron o	83 30 24 26	275 55 47 45	i sinu s	345 69 59 56	yel au	415 83 71 68	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig. 18)	
^t PHZ [/] ^t PLZ	turn "OFF" time S _n to V _{os}			80 29 23 24	275 55 47 48		345 69 59 60		415 83 71 72	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig. 18)	
^t su	set-up time S _n to LE		60 12 10 18	17 6 5 9			75 15 13 23		90 18 15 27	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig. 19)	
^t h	hold time S _n to LE	5 5 5 5	-8 -3 -2 -4			5 5 5 5		5 5 5 5	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig. 19)		
tw	LE minimum pulse width			11 1 3 7			125 25 21 31		150 30 26 38	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig. 19)	

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

AC CHARACTERISTICS FOR 74HC

	TEST COM			1	amb (°C)					TEST	COND	ITIONS
SYMBOL	PARAMETER			Y	74HC	Т			UNIT	v. 8	V/	VI	OTHER
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		ONT	V _{CC}	VEE	V	OTHER
		min.	typ.	max.	min.	max.	min.	max.					
V _I H	HIGH level input voltage	2.0	1.6	26 15 33	2.0	80 12 10	2.0		v	4.5 to 5.5	jatton o V _{os}	kgông LaiV	HTdt /THdt
VIL S	LOW level input voltage	480°	1.2	0.8		0.8	86 31 26	0.8	v	4.5 to 5.5	- VIO	naoi E e A	/8Zd1
±1 ₁	input leakage current	88 450		0.1		1.0	28 85	1.0	μА	5.5	0	V _C C or GND	
±IS	analog switch OFF-state current per channel	77 88 85 450		0.1		1.0	25 25	1.0	μА	10.0	0	VIH or VIL	IV _S I = V _{CC} - V _{EE} (see Fig. 10)
±IS MA	analog switch OFF-state current all channels	90 77 88		0.4		4.0	33 28 27	4.0	μА	10.0	0 / 6	V _{IH} or V _{IL}	V _S I = V _{CC} - V _{EE} (see Fig. 10)
±IS DE E	analog switch ON-state current	450 80 77		0.4		4.0	88 32 26	4.0	μА	10.0	80 V	V _{IH} or V _{IL}	IV _S I = V _{CC} - V _{EE} (see Fig. 11)
Icc	quiescent supply current	275		8.0 16.0		80.0 160.0	69 25 20	160.0 320.0	μΑ	5.5 5.0	0 -5.0	V _{CC} or GND	V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}
△Icc	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)	379 75 64	100	360		450	72 26 21	490	μА	4.5 to 5.5	OF O	V _{CC} -2.1V	other inputs at V _{CC} or GND

Note to HCT types

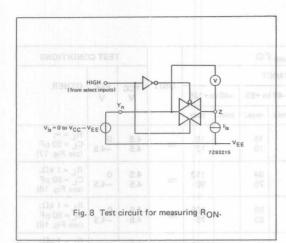
The value of additional quiescent supply current (\(\Delta\CC\)) for a unit load of 1 is given here.
 To determine \(\Delta\ICC\) per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LO	IENT				
E ₁ , E ₂ S _n LE	0.50 0.50 1.5	4.5 2.0 4.5 6.0				

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	V80-129V	001			T _{amb} (°C)					TEST C	ONDITIONS
OVMDOL	DADAMETER OF	1 - 150 r			74HC	T:			UNIT	1	V FIDI	OTHER
SYMBOL	PARAMETER		+25		-40 t	-40 to +85		+125	UNIT	V _{CC}	VEE	OTHER
		min.	typ.	max.	min.	max.	min.	max.		-	1	
tPHL/	propagation delay V _{is} to V _{os}	Dk OE	6 4	12 8		15 10	overe	18 12	ns	4.5 4.5	0 -4.5	R _L = ∞; C _L = 50 pF (see Fig. 17)
t _{PZH} /	turn "ON" time E ₁ to V _{os}	P.	40 31	75 60		94 75		113 90	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 18
^t PZH [/] ^t PZL	turn "ON" time	Typios Vig = 1	35 26	70 50		88 63	400	105 75	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 18)
^t PZH [/] ^t PZL	turn "ON" time LE to V _{os}		42 37	75 60		94 75		113 90	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 18)
^t PZH/ ^t PZL	turn "ON" time S _n to V _{os}		39 30	75 60	2021	94 75		113 90	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 18)
^t PHZ [/] ^t PLZ	turn "OFF" time E ₁ to V _{os}	-0	27 20	55 40		69 50	15° (83 60	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 18)
^t PHZ [/] ^t PLZ	turn "OFF" time E ₂ to V _{os}		32 26	60 50		75 63		90 75	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 18)
^t PHZ [/] ^t PLZ	turn "OFF" time LE to V _{os}		33 30	60 55		75 69		90 83	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 18)
^t PHZ/	turn "OFF" time S _n to V _{os}		33 29	65 55		81 69		98 83	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 18)
t _{su}	set-up time S _n to LE	12 14	6 7			15 18		18 21	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 19)
^t h	hold time S _n to LE	5 5	-1 -2			5 5		5 5	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Fig. 19)
t _W	LE minimum pulse width HIGH	25 25	13 13			31 31		38 38	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Fig. 19)



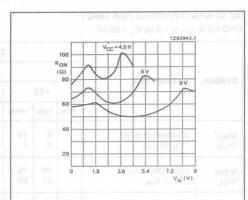
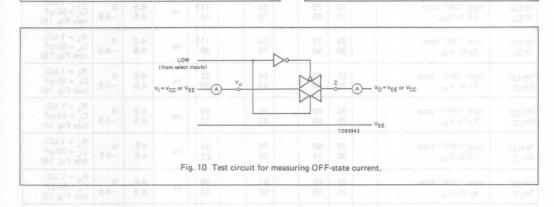
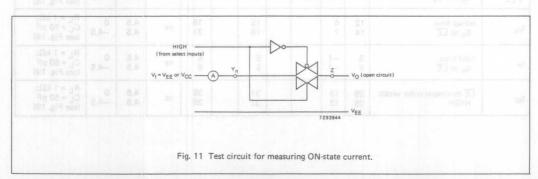


Fig. 9 Typical R_{ON} as a function of input voltage V_{is} for $V_{is} = 0$ to $V_{CC} - V_{EE}$.





ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C | bm 21 ap 3 cs until

SYMBOL	PARAMETER	typ.	UNIT	V _{CC}	V _{EE}	V _{is(p-p)}	CONDITIONS
	sine-wave distortion f =1 kHz	0.04 0.02	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10 \text{ k}\Omega; C_L = 50 \text{ pF}$ (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_{L} = 10 \text{ k}\Omega; C_{L} = 50 \text{ pF}$ (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600 \Omega$; $C_L = 50 pF$ (see Figs 12 and 15)
V _(p-p)	crosstalk voltage between control and any switch (peak-to-peak value)	120 220	mV mV	4.5 4.5	0 -4.5	11 8,760	$R_L = 600 \ \Omega; C_L = 50 \ pF;$ $f = 1 \ MHz \ (E_1, E_2 \ or S_n,$ square-wave between V_{CC} and $GND, t_r = t_f = 6 \ ns)$ (see Fig. 16)
f _{max}	minimum frequency response (-3dB)	160 170	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	R_L = 50 Ω; C_L = 10 pF (see Figs 13 and 14)
C _S	maximum switch capacitance independent (Y) common (Z)	5 25	pF pF		and some	yis .	36V 8V

Notes to AC characteristics

 V_{is} is the input voltage at a Y_n or Z terminal, whichever is assigned as an input. V_{os} is the output voltage at a Y_n or Z terminal, whichever is assigned as an output.

- 1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
 2. Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

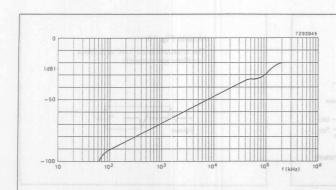
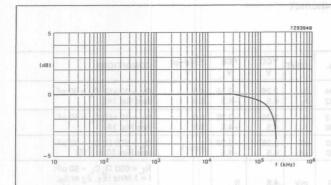


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions: V_{CC} = 4.5 V; GND = 0 V; V_{EE} = -4.5 V; R_L = 50 Ω ; R_{source} = 1 $k\Omega$.

Fig. 13 Typical frequency response.

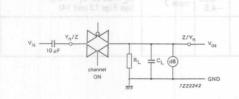


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

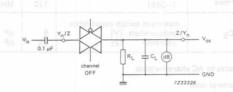


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

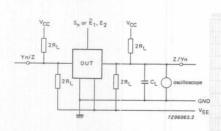


Fig. 16 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 16

The crosstalk is defined as follows (oscilloscope output):



AC WAVEFORMS

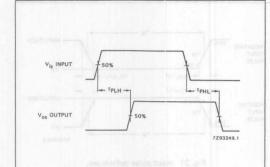


Fig. 17 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

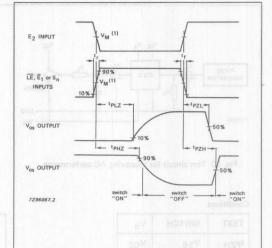


Fig. 18 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 18

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3$ V; $V_I = GND$ to 3 V.

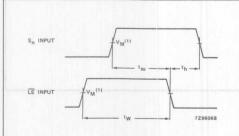


Fig. 19 Waveforms showing the set-up and hold times from S_n inputs to \overline{LE} input, and minimum pulse width of \overline{LE} .

Note to Fig. 19

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

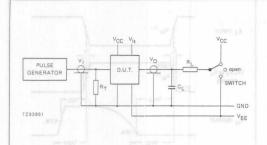


Fig. 20 Test circuit for measuring AC performance,

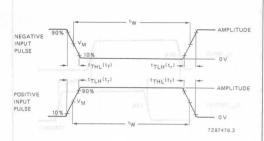


Fig. 21 Input pulse definitions.

Conditions

TEST	SWITCH	Vis	
^t PZH	VEE	VCC	
^t PZL	VCC	VEE	
^t PHZ	VEE	VCC	
^t PLZ	VCC	VEE	
others	open	pulse	

Definitions for Figs 20 and 21:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

 R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

 $t_r = t_f = 6$ ns; when measuring f_{max} , there is no constraint on t_r , t_f with 50% duty factor.

			t _r ; t _f					
FAMILY	AMPLITUDE	VM	f _{max} ; PULSE WIDTH	OTHER				
74HC	Vcc	50%	< 2 ns	6 ns				
74HCT	3.0 V	1.3 V	< 2 ns	6 ns				

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH LATCH

- Wide analog input voltage range: ± 5 V
- Low "ON" resistance:
- 80 Ω (typ.) at $V_{CC} V_{EE} = 4.5 \text{ V}$ 70 Ω (typ.) at V_{CC} - V_{EE} = 6.0 V 60 Ω (typ.) at V_{CC} - V_{EE} = 9.0 V
- Logic level translation: to enable 5 V logic to communicate with ± 5 V analog signals
- · Typical "break before make" built in
- Address latches provided
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

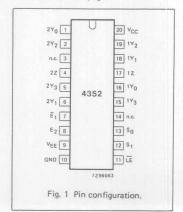
The 74HC/HCT4352 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4352 are dual 4-channel analog multiplexers/demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs (nY₀ to nY₃) and a common input/output

The common channel select logics include two select inputs (So and S1), an active LOW enable input (\overline{E}_1) , an active HIGH enable input (E2) and a latch enable input

With E1 LOW and E2 HIGH, one of the four switches is selected (low impedance ON-state) by S₀ and S₁. The data at the select inputs may be latched by using the active LOW latch enable input (LE). When LE is HIGH, the latch is transparent. When either of the two enable inputs. $\overline{\mathsf{E}}_1$ (active LOW) and E_2 (active HIGH), is inactive, all analog switches are turned off.

(continued on next page)



01/44501	DADAMETER	CONDITIONS	TY	SEG N	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
t _{PZH} /	turn "ON" time \overline{E}_1 , E_2 or S_n to V_{os}	C _L = 15 pF	31	33	ns
t _{PHZ} / t _{PLZ}	turn "OFF" time E ₁ , E ₂ or S _n to V _{OS}	$R_L = 1 k\Omega$ $V_{CC} = 5 V$	20	20	ns
CI	input capacitance (VO) 6	uong	3.5	3.5	pF
C _{PD}	power dissipation capacitance per switch	notes 1 and 2	55	55	pF
CS	max. switch capacitance independent (Y) common (Z)	pieos gril	5 12	5 12	pF pF

$$V_{EE} = GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L + C_S) \times V_{CC}^2 \times f_o)$$
 where:

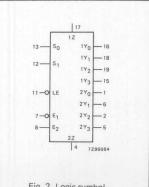
CL = output load capacitance in pF Cs = max. switch capacitance in pF

$$f_0$$
 = output frequency in MHz C_S = max. switch capacite $\Sigma \{ (C_L + C_S) \times V_{CC}^2 \times f_0 \} = \text{sum of outputs}$ V_{CC} = supply voltage in V

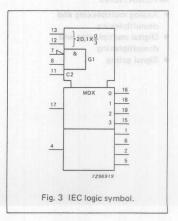
2. For HC the condition is
$$V_I = GND$$
 to V_{CC}
For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5$ V

PACKAGE OUTLINES

20-lead DIL; plastic (SOT146). 20-lead mini-pack; plastic (SO20; SOT163A).







PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	SYMBOL
1, 6, 2, 5 3, 14	11.6.	The second of th	724), /HZ4),
7 8 an OS 9	E ₁ E ₂ VEE	enable input (active LOW) enable input (active HIGH) negative supply voltage	
3.5 pF 01		ground (0 V)	
11 13, 12	S ₀ , S ₁	latch enable input (active LOW) select inputs	
16, 18, 19, 15 17, 4 20	1Y ₀ to 1Y ₃ 1Z, 2Z VCC	independent inputs/outputs common inputs/outputs positive supply voltage	

FUNCTION TABLE

	CHANNEL	and at feet	INPUTS									
onsuper	ON	s ₀		bs UE uga	E ₂	E ₁						
	none none	X	X	X	X ni a	H X						
econdin	$ \begin{array}{r} nY_0 - nZ \\ nY_1 - nZ \\ nY_2 - nZ \\ nY_3 - nZ \end{array} $	H L H	LV a.s	Н Н Н	Н Н Н	L L L						
	aste (SD20; SD	X	X	L ↓	H X	L X						

* Last selected channel "ON"

Selected channels latched

H = HIGH voltage level L = LOW voltage level

X = don't care

↓ = HIGH-to-LOW LE transition

APPLICATIONS

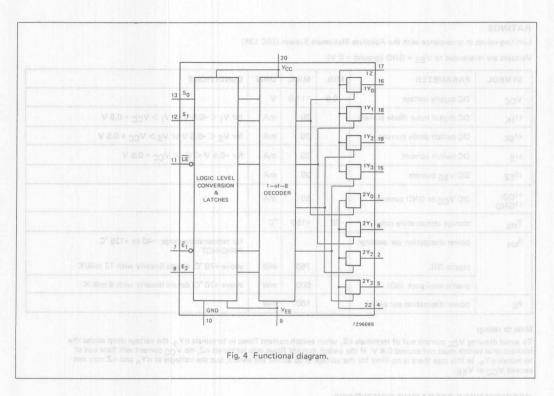
- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

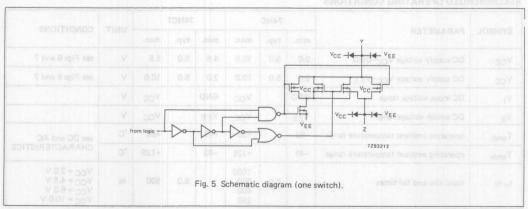
GENERAL DESCRIPTION

V_{CC} and GND are the supply voltage pins for the digital control inputs (So, S1, LE, \overline{E}_1 and \overline{E}_2). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (n'Y₀ to nY3, and nZ) can swing between VCC as a positive limit and VEE as a negative limit. VCC - VEE may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, VEE is connected to GND (typically ground).







RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to VEE = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
Vcc	DC supply voltage	-0.5	+11.0	V	08 81
±11K	DC digital input diode current		20	mA	for $V_1 < -0.5 \text{ V}$ or $V_1 > V_{CC} + 0.5 \text{ V}$
±1SK	DC switch diode current		20	mA	for V_S < -0.5 V or V_S > V_{CC} + 0.5 V
±IS	DC switch current		25	mA	for $-0.5 \text{ V} < \text{V}_{\text{S}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$
±1EE	DC VEE current	3	20	mA	38V29 3(36J
±ICC; ±IGND	DC V _{CC} or GND current	H	50	mA	EBICITAL
T _{stg}	storage temperature range	-65	+150	°C	
Ptot	power dissipation per package	H	750	mW	for temperature range: -40 to +125 °C 74HC/HCT above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)	H	500	mW	above +70 °C: derate linearly with 6 mW/K
Ps	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminals nZ, when switch current flows in terminals nY_n , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ_n , no V_{CC} current will flow out of terminals nY_n . In this case there is no limit for the voltage drop across the switch, but the voltages at nY_n and nZ may not exceed V_{CC} or V_{EE} .

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74HC			74HC	Г	UNIT	CONDITIONS	
STIVIBUL	PARAMETER	min.	typ.	max.	min.	typ.	max.	UNIT		
Vcc	DC supply voltage V _{CC} -GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7	
Vcc	DC supply voltage V _{CC} -V _{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7	
VI	DC input voltage range	GND		Vcc	GND		VCC	V		
Vs	DC switch voltage range	VEE		VCC	VEE		Vcc	V		
T _{amb}	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC	
T _{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	CHARACTERISTICS	
t _r , t _f	input rise and fall times	rano) n	6.0	1000 500 400 250	S 8 .9i9	6.0	500	ns	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V V _{CC} = 10.0 V	

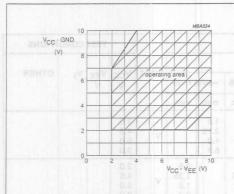


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4352.

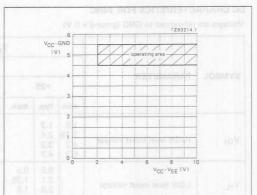


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4352.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} – GND or V_{CC} – V_{EE} =2.0, 4.5, 6.0 and 9.0 V For 74HCT: V_{CC} – GND =4.5 and 5.5 V; V_{CC} – V_{EE} =2.0, 4.5, 6.0 and 9.0 V

	10 0 0,01 Am	2:0		1 0	T _{amb} (°C)	0			elenns	TEST	COND	ITION	S
SYMBOL	PARAMETER	-	74HC/HCT									e palen	1	V-
STIVIBUL	PARAMETER	+25			-40 to +85		-40 to +12		125 UNIT		VEE	Is μA	Vis	VI
	33V 0 0.8	min.	typ.	max.	min.	max.	min.	max.						
RON	ON resistance (peak)	320.0	_ 100 90 70	180 160 130		225 200 165		270 240 195	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	VCC to VEE	VIN or VIL
RON	ON resistance (rail)		150 80 70 60	140 120 105		- 175 150 130		210 180 160	ΩΩΩΩ	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	VEE	VIH or VIL
RON	ON resistance (rail)		150 90 80 65	160 140 120		_ 200 175 150		- 240 210 180	ΩΩΩ	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	Vcc	VIH or VIL
ΔR _{ON}	maximum ∆ON resistance between any two channels		9 8 6						ΩΩΩ	2.0 4.5 6.0 4.5	0 0 0 -4.5		V _{CC} to V _{EE}	VIH or VIL

Notes to DC characteristics

At supply voltages (V_{CC} - V_{EE}) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
 For test circuit measuring R_{ON} see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

	NAME OF THE OWNER, AND THE OWNER, AN			1	amb	(°C)				1	TEST	COND	ITIONS
					74H	С		ZZ					OTUED.
SYMBOL	PARAMETER		+25		-40 to +85 -40 to		0 +125	UNIT	V _{CC}	VEE	VI	OTHER	
		min.	typ.	max.	min.	max.	min.	max.					
VIH	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		٧	2.0 4.5 6.0 9.0		8	
VIL	LOW level input voltage	วิทธายเป	0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	o noiz	0.5 1.35 1.8 2.7	V sers pri	2.0 4.5 6.0 9.0	besire	Suara	ê ,gFl
±II	input leakage current	nov yiq	pue arl	0.1		1.0 2.0		1.0	μА	6.0	0	VCC or GND	ua esti
±Ις	analog switch OFF-state current per channel			0.1	V	1.0 0.0 bms	.5, 6,0	1.0	μА	10.0	0	VIH or VIL	V _S I = V _{CC} - V _E I (see Fig. 10
±IS ano	analog switch OFF-state current all channels			0.2	(Uið 3	2.0	· aav	2.0	μА	10.0	0	VIH or VIL	V _S = V _{CC} - V _E (see Fig. 10
±IS V at	analog switch ON-state current	180	t of Div	0.2	3H/3I	2.0	+25	2.0	μА	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} - V _{EI} (see Fig. 11
lcc	quiescent supply current	.xon	r uni	8.0 16.0	in. Inii	80.0 160.0	yp. n	160.0 320.0	μΑ	6.0	0	VCC or GND	V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}
										(NEBO)	egnax	PRINT MO	NOH

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	TEST CONDIT				Tamb (°C)					TEST C	ONDITIONS
					74H0					.,	.,	OTHER
SYMBOL	PARAMETER		asr++25 as		-40 to +85 -		-40 to +125		UNIT	V _{CC}	VEE	OTHER
		min	typ.	max.	min.	max.	min.	max.				
^t PHL [/] ^t PLH	propagation delay V _{is} to V _{os}	Y	17 6 5 5	60 12 10 8		75 15 13 10	Đ	90 18 15 12	ns 46	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = ∞; C _L = 50 pF (see Fig. 18)
^t PZH [/] ^t PZL	turn "ON" time E ₁ ; E ₂ to V _{os} LE to V _{os}	V	99 36 29 25	325 65 55 46	0.1	405 81 69 58	2 0.8	490 98 83 69	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 19)
^t PZH [/]	turn "ON" time S _n to V _{os}	6.A. I	99 36 29 25	325 65 55 46		405 81 69 58	1.0	490 98 80 69	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = 1 k Ω ; C _L = 50 pF (see Fig. 19)
t _{PHZ} /	turn "OFF" time E1; E2 to Vos LE to Vos		58 21 17 21	200 40 34 40	as:	250 50 43 50	1.0	300 60 51 60	ns ***	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 19)
t _{PHZ} /	turn "OFF" time S _n to V _{os}	u (63 23 18 24	200 40 34 40	2.1	250 50 43 50	0.0	300 60 51 60	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Fig. 19)
t _{su}	set-up time S _n to LE	90 18 15 18	17 6 5 9	0.0	115 23 20 23	0	135 27 23 27		ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Fig. 20)
10 35 V th	hold time S _n to LE	5 5 5 5	-6 -2 -2 -3	0	5 5 5 5		5 5 5 5	II.	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig. 20)
tw	LE minimum pulse width HIGH	80 16 14 16		of 1 is		tu a rol Iol Timo	120 24 20 24	zneme: sulsv gl	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = 1 k Ω ; C _L = 50 pF (see Fig. 20)

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

	TEST CONDIT	T _{amb} (°C)								TEST CONDITIONS			
SYMBOL	PARAMETER									.,			OTHER
		+25			-40 to +85		-40 to +125		UNIT	V _{CC}	VEE	VI	OTHER
		min.	typ.	max.	min.	max.	min.	max.					
V _{IH} R ₀ R ₀ F ₀ F ₀ F ₀ F ₀	HIGH level input voltage	2.0	1.6		2.0		2.0	10	v	4.5 to 5.5	ion de	ropagat V _{is} to	PECT I
VIL (Ost)	LOW level input voltage	8	1.2	0.8	04 18	0.8	32	0.8	v	4.5 to 5.5	mid "I	10" mu	/HZ9
(e1gr ±1 ₁ ;Ωx f	input leakage current	90	ð A	0.1	58	1.0	20 32	1.0	μА	5.5	0 80	VCC or GND	724
±1 _S (81 .91	analog switch OFF-state current per channel	0	55	0.1	98 88	1.0	46	1.0	μА	10.0	0	VIH or VIL	V _S = V _{CC} - V _{EE} (see Fig. 10)
±1 _S /81 /81	analog switch OFF-state current all channels	0		0.2	88 43 60	2.0	40 34 40	2.0	μА	10.0	0	VIH or VIL	IV _S I = V _{CC} - V _{EE} (see Fig. 10)
± Is (\$2.4) 50 pF 814	analog switch ON-state	00	8 8 8	0.2	25 50 43	2.0	20 40 34	2.0	μА	10.0	0 4	VIH or VIL	IV _S I = V _{CC} - V _{EE} (see Fig. 11)
1 k2; 22l 50 pr	quiescent supply current			8.0 16.0	2	80.0 160.0	Oliv	160.0 320.0	μΑ	5.5 5.0	0 -5.0	VCC or GND	V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}
∆Icc Salt	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450	8 5 5	490	μΑ	4.5 to 5.5	0	V _{CC} -2.1V	other inputs at V _{CC} or GND

Note to HCT types

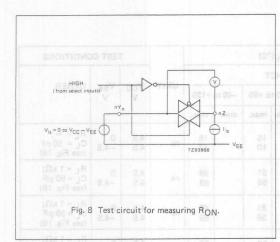
The value of additional quiescent supply current (\(\Delta\Log\C)\) for a unit load of 1 is given here.
 To determine \(\Delta\Log\C)\) per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT					
E ₁ , E ₂	0.50					
S _n	0.50					
LE	1.5					

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

	Y ESPERANCE .	- 1001			T _{amb} (°C)	3,614				TEST C	ONDITIONS
0./440.01	PARAMETER		7		74HC	Т			LINUT			OTHER
SYMBOL	PARAMETER	+25			-40 to +85 -40			+125	UNIT	V _{CC}	VEE	OTHER
		min.	typ.	max.	min.	max.	min.	max.	1			
^t PHL/	propagation delay V _{is} to V _{os}	(13	6 5	12		15 10	el É	18 12	ns	4.5 4.5	0 -4.5	R _L = ∞; C _L = 50 pF (see Fig. 18)
^t PZH [/] ^t PZL	turn "ON" time E1; E2 to Vos LE to Vos	9	38 28	65 46		81 58		98 69	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 19)
t _{PZH} /	turn "ON" time	Spigy V _{is} = 0	38 27	65 46		81 58		98 69	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 19)
t _{PHZ} /	turn "OFF" time E1 to Vos LE to Vos		20 20	40 40		50 50		60 60	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 19)
^t PHZ [/] ^t PLZ	turn "OFF" time Ē ₂ , S _n to V _{os}		25 25	43 43		54 54		65 65	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 19)
t _{su}	set-up time S _n to LE	16 18	7 9		20 23		24 27	io.	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 20)
^t h	hold time S _n to LE	5	-1 -1	K	5		5		ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Fig. 20)
tw	LE minimum pulse width	16 16	3 4		20 20		24 24	- 01	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Fig. 20)



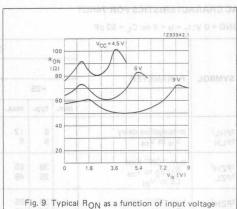
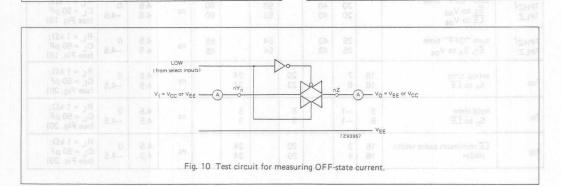


Fig. 9 Typical R_{ON} as a function of input voltage Vis for Vis = 0 to VCC - VEE.



ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V _{CC}	V _{EE}	V _{is(p-p)}	CONDITIONS		
	sine-wave distortion f = 1 kHz	0.04	%	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10 \text{ k}\Omega; C_L = 50 \text{ pF}$ (see Fig. 14)		
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig. 14)		
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600 \Omega$; $C_L = 50 pF$ f = 1 MHz (see Figs 12 and 15)		
	crosstalk between any two switches/ multiplexers	-60 -60	dB dB	2.25 4.5	-2.25 -4.5	note 1	R _L = 600 Ω; C _L = 50 pF; f = 1 MHz (see Fig. 16)		
V _(p-p)	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5	rrisa	$R_L = 600 \ \Omega; C_L = 50 \ pF;$ $f = 1 \ MHz \ (E_1, E_2 \ or S_n,$ square-wave between V_{CC} and $GND, t_r = t_f = 6 \ ns)$ (see Fig. 17)		
fmax	minimum frequency response (-3dB)	160 170	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	$R_L = 50 \Omega$; $C_L = 10 pF$ (see Figs 13 and 14)		
CS	maximum switch capacitance independent (Y) common (Z)	5 12	pF pF				Fig. 14. Test circuit for mean		

Notes to AC characteristics

 V_{is} is the input voltage at an nY $_{n}$ or nZ terminal, whichever is assigned as an input. V_{os} is the output voltage at an nY $_{n}$ or nZ terminal, whichever is assigned as an output.

1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω). 2. Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

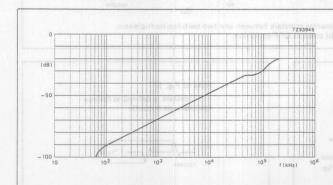
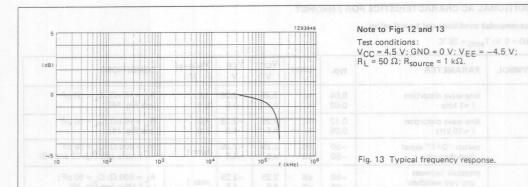


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions: V_{CC} = 4.5 V; GND = 0 V; V_{EE} = -4.5 V; R_L = 50 Ω ; R_{source} = 1 k Ω .

Fig. 13 Typical frequency response.

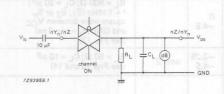


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

Fig. 16 Test circuits for measuring crosstalk between any two switches/multiplexers. (a) channel ON condition; (b) channel OFF condition.

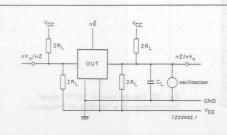
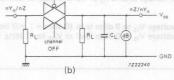


Fig. 17 Test circuit for measuring crosstalk between control and any switch.



Note to Fig. 17

The crosstalk is defined as follows (oscilloscope output):

AC WAVEFORMS

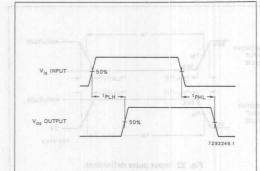


Fig. 18 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

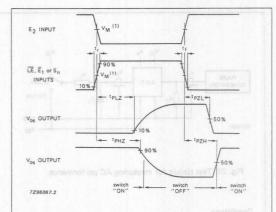


Fig. 19 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 19

(1) HC :
$$V_M$$
 = 50%; V_I = GND to V_{CC} .
HCT: V_M = 1.3 V; V_I = GND to 3 V.

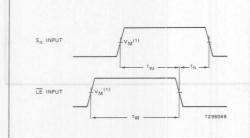


Fig. 20 Waveforms showing the set-up and hold times from S_n inputs to \overline{LE} input, and minimum pulse width of $\overline{LE}.$

Note to Fig. 20

(1) HC :
$$V_M$$
 = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

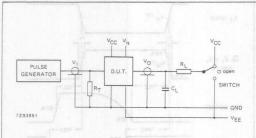


Fig. 21 Test circuit for measuring AC performance.

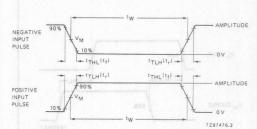


Fig. 22 Input pulse definitions.

Conditions

TEST	SWITCH	Vis
tPZH	VEE	VCC
tPZL	VCC	VEE
tPHZ	VEE	VCC
tPLZ	VCC	VEE
others	open	pulse

			delays	noispegoso tritf turnuo					
FAN	IILY	AMPLITUDE	VM	f _{max} ; PULSE WIDTH	OTHER				
74H	0	Vcc	50%	< 2 ns	6 ns				
74H	CT	3.0 V	1.3 V	< 2 ns	6 ns				

Definitions for Figs 21 and 22:

- C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
- $R_T =$ termination resistance should be equal to the output impedance Z_O of the pulse generator.
- $t_r = t_f = 6$ ns; when measuring f_{max} , there is no constraint on t_r , t_f with 50% duty factor.

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH LATCH

FEATURES TELESCENES LASSING

- Wide analog input voltage range: ± 5 V
- Low "ON" resistance: 80 Ω (typ.) at V_{CC} - V_{EE} = 4.5 V 70 Ω (typ.) at V_{CC} - V_{EE} = 6.0 V 60 Ω (typ.) at V_{CC} - V_{EE} = 9.0 V Logic level translation:
- to enable 5 V logic to communicate with ± 5 V analog signals
- · Typical "break before make" built in
- Address latches provided
- Output capability: non-standard
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4353 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4353 are triple 2-channel analog multiplexers/demultiplexers with two common enable inputs (E₁ and E₂) and a latch enable input (LE). Each multiplexer has two independent inputs/outputs (nYo and nY1), a common input/output (nZ) and select inputs (S₁ to S₃).

(continued on next page)

SYMBOL	DADAMETER	CONDITIONS	TY	PICAL	PIN D
STIMBUL	PARAMETER MUE AND FUNCTION		НС	нст	UNIT
t _{PZH} /	turn "ON" time \overline{E}_1 , E_2 or S_n to V_{os}	C _L = 50 pF	29	21	ns a
^t PHZ [/]	turn "OFF" time E ₁ , E ₂ or S _n to V _{os}	$R_{L} = 1 k\Omega$ $V_{CC} = 5 V$	20	22	ns 8
Cl	input capacitance	10	3.5	3.5	pF
C _{PD}	power dissipation capacitance per switch	notes 1 and 2	23	23	pF
CS	max. switch capacitance independent (Y) common (Z)		5 8	5 21 1	pF pF

$$V_{EE} = GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

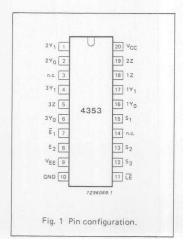
$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L + C_S) \times V_{CC}^2 \times f_o)$$
 where:

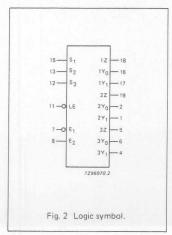
C_L = output load capacitance in pF C_S = max. switch capacitance in pF $\Sigma \{(C_L + C_S) \times V_{CC}^2 \times f_0\} = \text{sum of outputs} \quad V_{CC} = \text{supply voltage in V}$

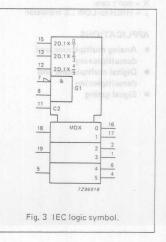
2. For HC the condition is VI = GND to VCC For HCT the condition is $V_1 = GND$ to $V_{CC} - 1.5 V$

PACKAGE OUTLINES

20-lead DIL; plastic (SOT146). 20-lead mini-pack; plastic (SO20; SOT163A).







PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	
2, 1	2Y ₀ , 2Y ₁ 3Z	independent inputs/outputs common input/output	7241 JHZ41
6, 4 3, 14	3Y ₀ , 3Y ₁ n.c.	independent inputs/outputs not connected	
7 8 8.8	E ₁ E ₂	enable input (active LOW) enable input (active HIGH)	
9	VEE GND	negative supply voltage ground (0 V)	
11 15, 13, 12	LE S ₁ to S ₃	latch enable input (active LOW) select inputs	
16, 17 18	1Y ₀ , 1Y ₁ 1Z	common input/output	
19 20	V _{CC}	common input/output positive supply voltage	

FUNCTION TABLE

	INP	V atuorus	CHANNEL	
Ē ₁	E ₂	LE	Sn	ON ON
H X	X L	X	×	none none
L	H H	H	L //HEart	$nY_0 - nZ$ $nY_1 - nZ$
L X	H X	L ↓	X	*

* Last selected channel "ON".

** Selected channels latched.

H = HIGH voltage level

L = LOW voltage level

X = don't care

↓ = HIGH-to-LOW LE transition

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

GENERAL DESCRIPTION

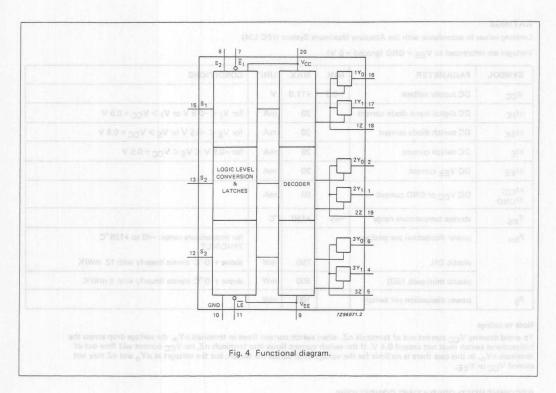
Each multiplexer/demultiplexer contains two bidirectional analog switches, each with one side connected to an independent input/output (nY₀ and nY₁) and the other side connected to a common input/output (nZ).

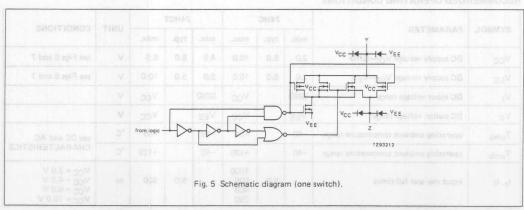
With \overline{E}_1 LOW and E_2 HIGH, one of the two switches is selected (low impedance ON-state) by S_1 to S_3 . The data at the select inputs may be latched by using the active LOW latch enable input ($\overline{\text{LE}}$). When $\overline{\text{LE}}$ is HIGH, the latch is transparent. When either of the two enable inputs, \overline{E}_1 (active LOW) and E_2 (active HIGH), is inactive, all analog

switches are turned off.

 V_{CC} and GND are the supply voltage pins for the digital control inputs (S₁ to S₃, $\overline{\rm LE}, E_1$ and E_2). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY₀ and nY₁, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC}-V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, VEE is connected to GND (typically ground).





RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to VEE = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
Vcc	DC supply voltage	-0.5	+11.0	V	
±11K	DC digital input diode current	H	20	mA	for $V_1 < -0.5 \text{ V}$ or $V_1 > V_{CC} + 0.5 \text{ V}$
±ISK	DC switch diode current		20	mA	for $V_S < -0.5 \text{ V}$ or $V_S > V_{CC} + 0.5 \text{ V}$
±IS	DC switch current		25	mA	for $-0.5 \text{ V} < \text{V}_{\text{S}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$
±1EE	DC VEE current	H	20	mA	VB3-DIBGU VB
±ICC; ±IGND	DC V _{CC} or GND current		50	mA	8 13H37A0
T _{stg}	storage temperature range	-65	+150	°C	
P _{tot}	power dissipation per package	D _h			for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL	Land Land	750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)	HI	500	mW	above +70 °C: derate linearly with 8 mW/K
PS	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminals nZ, when switch current flows in terminals nY_n , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ_n no V_{CC} current will flow out of terminals nY_n . In this case there is no limit for the voltage drop across the switch, but the voltages at nY_n and nZ may not exceed V_{CC} or V_{EE} .

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74HC			74HC1	Г	LIBUT	CONDITIONS	
STIMBUL	PARAMETER	min.	typ.	max.	min.	typ.	max.	UNIT	CONDITIONS	
VCC	DC supply voltage V _{CC} -GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7	
Vcc	DC supply voltage V _{CC} -V _{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7	
VI	DC input voltage range	GND		Vcc	GND		VCC	V		
VS	DC switch voltage range	VEE	CF.	Vcc	VEE		Vcc	V		
T _{amb}	operating ambient temperature range	-40		+85	-40	~J-1	+85	°C	see DC and AC	
T _{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	CHARACTERISTICS	
t _r , t _f	input rise and fall times	enc) m	6.0	1000 500 400 250	Fig. 5	6.0	500	ns	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V V _{CC} = 10.0 V	

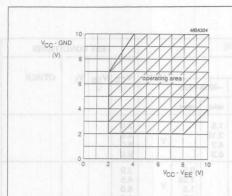


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4353.

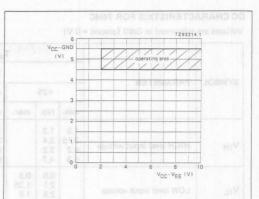


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4353.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: $V_{CC}-$ GND or $V_{CC}-V_{EE}$ =2.0, 4.5, 6.0 and 9.0 V For 74HCT: $V_{CC}-$ GND =4.5 and 5.5 V; $V_{CC} V_{EE}$ =2.0, 4.5, 6.0 and 9.0 V

	16 0 0.01 Ag				T _{amb} (°C)				TEST CONDITIONS					
SYMBOL	PARAMETER	74HC/HCT								spekio	datio	ra golon			
	DOV 0 0.00 Au	+25		-40 to +85		-40 to +125		UNIT	V _{CC}	VEE	IS μA	Vis	VI		
ACC: Acz p		min.	typ.	max.	min.	max.	min.	max.	300	suo yl	base to	epasio	95	1	
RON	ON resistance (peak)		100 90 70	180 160 130		225 200 165		270 240 195	Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	V _{CC} to V _{EE}	VIN or VIL	
RON	ON resistance (rail)		150 80 70 60	140 120 105		- 175 150 130		- 210 180 160	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	VEE	VIH or VIL	
R _{ON}	ON resistance		150 90 80 65	160 140 120		_ 200 175 150		240 210 180	Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	Vcc	VIH or VIL	
ΔRON	maximum ΔΟΝ resistance between any two channels		9 8 6						Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5		V _{CC} to V _{EE}	VIH or VIL	

Notes to DC characteristics

1. At supply voltages ($V_{CC} - V_{EE}$) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

2. For test circuit measuring RON see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

	6					dato L	10		T _{amb} (°C)	X	JUN.	TA	K	TEST	ST CONDITIONS		
CVMD	01	BARAS	AETER						74H0				UNIT	W-	V-	V.	OTHER	
SYMB	UL	PARAM	METER				+25		-40 to +85 -40 to -					V _{CC}	VEE	VI	OTHER	
						min.	typ.	max.	min.	max.	min.	max.						
VIH		HIGHI	evel inp	out volta	ige	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0		- 3		
VIL	to no	LOW le		ut voltaç	ge	ens'ison	0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	nt to n	0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0	s no be	Instau	Fig. 6 1	
±IĮ		input le		current	Tot.	engatic	w yiqq	0.1		1.0 2.0		1.0 2.0	μΑ	6.0 10.0	0	VCC or GND	y ylagut	
±IS			switch (it per ch	OFF-stan	te			0.1	V	1.0	5, 6.0	1.0	μА	10.0	0	VIH or VIL	IV _S I = V _{CC} - V _{EI} (see Fig. 10	
±IS	MOI	analog s	switch (te			0.1	(D°) di	1.0	BBV	1.0	μА	10.0	0	VIH or VIL	IV _S I = V _{CC} - V _E I (see Fig. 10	
±IS	ži'	analog s	switch (ON-state	TIMU	828	0.01	0.1	13H/3	1.0	25	1.0	μА	10.0	0	V _{IH} or V _{IL}	IV _S I = V _{CC} - V _{EI} (see Fig. 11	
Icc		quiesce	nt supp	ly curre	nt	.X80	ı İ.n	8.0 16.0	m "ni	80.0 160.0	m Lq	160.0 320.0	μΑ	6.0 10.0	0	V _{CC} or GND	V _{is} = V _{EE} o V _{CC} ; V _{os} = V _{CC} or V _{EE}	
NIA.	SO V		0 0	4.5	ΩΩ	170 140 95			22 20 16	0		9		(peak)	907673	ISST VIO	NON	

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

3140				1983	T _{amb} (°C)				TEST CONDITIONS			
0.44501		74HC								.,	.,	OTHER	
SYMBOL	PARAMETER	+25			-40	-40 to +85 -40 to			UNIT	V CC	VEE	OTHER	
		min.	typ.	max.	min.	max.	min.	max.					
^t PHL/	propagation delay V _{is} to V _{os}		14 5 4 4	60 12 10 8	9	75 15 13 10	Э,	90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = ∞; C _L = 50 pF (see Fig. 18)	
t _{PZH} /	turn "ON" time E ₁ ; E ₂ to V _{os}	6.	61 22 18 18	250 50 43 40	0	315 63 54 50	2 0	375 75 64 60	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 19)	
tpZH/ tpZL	turn "ON" time	0.	55 20 16 17	200 40 34 40		250 50 43 50	ie i	300 60 51 60	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 19)	
t _{PZH} / t _{PZL}	turn "ON" time S _n to V _{os}	0.	61 22 18 17	225 45 38 40	ar I	280 56 48 50	0	340 68 58 60	ns all	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Fig. 19)	
t _{PHZ} /	turn "OFF" time E ₁ ; E ₂ to V _{os}	0.	66 24 19 19	250 50 43 40	ī	315 63 54 50	0	375 75 64 60	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 19)	
t _{PHZ} / t _{PLZ}	turn "OFF" time S _n to V _{os} ; LE to V _{os}	20.0	55 20 16 19	200 40 34 40		250 50 43 50	it i	300 60 51 60	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Fig. 19)	
t _{su}	set-up time S _n to LE	60 12 10 18	17 6 5 8		75 15 13 23		90 18 15 27		ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Fig. 20)	
th	hold time S _n to LE	5 5 5 5	-6 -2 -2 -3	el i to t Majoriti	5 5 5	for a u	5 5 5 5	toerrug ulsv sid	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 20)	
t _W	LE minimum pulse width	80 16 14 16	11 4 3 6		100 20 17 20		120 24 20 24		ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 20)	

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

		TEST CONDIT				T _{amb} (°C)					TEST	CONDI	TIONS
		- V 7 140				74HC	т					.,		OTHER
SYMBOL		PARAMETER	257-+25			-40 to +85		-40 to +125		UNIT	VCC	VEE	VI	OTTL
			min.	typ.	max.	min.	max.	min.	max.					
VIH	19F	HIGH level input voltage	2.0	1.6		2.0	5	2.0	8 8	V	4.5 to 5.5	b nois	geopie V _{is} to	71642
VIL	(Ω)	LOW level input voltage	52.	1.2	0.8		0.8	8 8	0.8	V	4.5 to 5.5	nir "N	3" mas	1029
±I[(2)	input leakage current	0		0.1	200	1.0	3 4 8 4 5 2	1.0	μА	5.5	0	V _{CC} or GND	72.6
±IS	18)	analog switch OFF-state current per channel	0		0.1	ic ia ia	1.0	14 C 14 Y	1.0	μΑ	10.0	0	VIH or VIL	V _S = V _{CC} - V _{EE} (see Fig. 10)
±IS	190	analog switch OFF-state current all channels	200		0.1		1.0		1.0	μΑ	10.0	0	VIH or VIL	IV _S I = V _{CC} - V _{EE} (see Fig. 10
±IS	1:03: Rg	analog switch ON-state current	175 5		0.1	18 18	1.0	1 50	1.0	μА	10.0	0	V _{IH} or V _{IL}	IVSI = VCC - VEE (see Fig. 11)
lcc	;Ω)	quiescent supply current	00		8.0 16.0	25	80.0 160.0	3 61 5 20 5 48	160.0 320.0	μА	5.5 5.0	0 -5.0	V _{CC} or GND	V _{is} = V _{EE} o V _{CC} ; V _{os} = V _{CC} or V _{EE}
ΔICC	153	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)	0	100	360	-63 -63 -63 -63 -63 -63 -63 -63 -63 -63	450	SA 6	490	μΑ	4.5 to 5.5	0	V _{CC} -2.1 V	other inputs at V _{CC} or GND

Note to HCT types

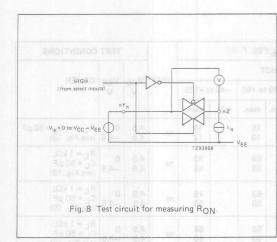
1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
E ₁ , E ₂	0.50
S _n	0.50
LE	1.5

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

		100			Tamb	(°C)				TEST CONDITIONS		
01/24001	PARAMETER	100		14	74HC	т	人		LINUT		.,	OTHER
SYMBOL		+25			-40 to +85 -40 to +12			o +125	UNIT	VCC	VEE	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/	propagation delay V _{is} to V _{os}	Ga	5 4	12		15 10	- 9	18 12	ns	4.5 4.5	0 -4.5	R _L = ∞; C _L = 50 pf (see Fig. 18)
t _{PZH} /	turn "ON" time E ₁ to V _{os}	20 -	26 22	55 45		69 56		83 68	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 19)
^t PZH [/]	turn "ON" time E ₂ to V _{os}	TypiqaT	22 18	50 40		63 50	1/2	75 60	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 19)
^t PZH [/]	turn "ON" time	21.V	21 17	45 40		56 50		68 60	ns	4.5 4.5	0 -4.5	$R_L = 1 \text{ k}\Omega;$ $C_L = 50 \text{ pF}$ (see Fig. 19)
t _{PZH} /	turn "ON" time S _n to V _{os}		25 19	50 45		63 56		75 68	ns	4.5 4.5	0 -4.5	$R_L = 1 \text{ k}\Omega;$ $C_L = 50 \text{ pF}$ (see Fig. 19)
^t PHZ [/] ^t PLZ	turn "OFF" time E ₁ to V _{os}		23 19	50 40	-<	63 50		75 60	ns	4.5 4.5	0 -4.5	$R_L = 1 \text{ k}\Omega;$ $C_L = 50 \text{ pF}$ (see Fig. 19)
^t PHZ [/] ^t PLZ	turn "OFF" time	-0	27 23	50 40		63 50	- (75 60	ns	4.5 4.5	0 -4.5	$R_L = 1 \text{ k}\Omega;$ $C_L = 50 \text{ pF}$ (see Fig. 19)
^t PHZ [/] ^t PLZ	turn "OFF" time	1.50	19 19	40 40		50 50		60 60	ns	4.5 4.5	0 -4.5	$R_L = 1 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig. 19)
tPHZ/	turn "OFF" time S _n to V _{os}	ate cut	22 22	45 45	8ff) 10	56 56) Test	68 68	ns	4.5 4.5	0 -4.5	$R_L = 1 \text{ k}\Omega;$ $C_L = 50 \text{ pF}$ (see Fig. 19)
^t su	set-up time S _n to LE	12 15	7 9		15 19		18 22		ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 20)
^t h	hold time S _n to LE	5	0 -2		5		5 5	Villa	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega;$ $C_L = 50 pF$ (see Fig. 20)
tw.	LE minimum pulse width	16 16	3 5	-15	20 20		24 24	Q	ns	4.5 4.5	0 -4.5	$R_L = 1 k\Omega$; $C_L = 50 pF$ (see Fig. 20)



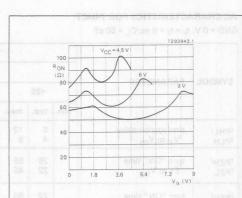
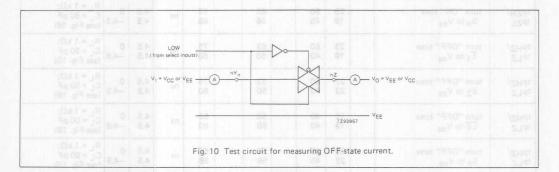
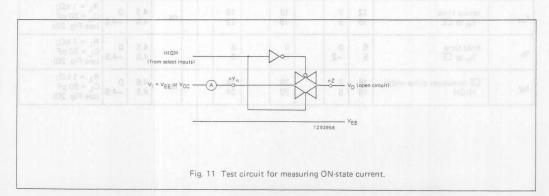


Fig. 9 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to V_{CC} - V_{EE} .





ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; Tamb = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	Vcc V	V _{EE}	V _{is(p-p)}	CONDITIONS
	sine-wave distortion f =1 kHz	0.04 0.02	%	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_{L} = 10 \text{ k}\Omega; C_{L} = 50 \text{ pF}$ (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600 \Omega$; $C_L = 50 pF$ f = 1 MHz (see Figs 12 and 15)
38.	crosstalk between any two switches/ multiplexers	-60 -60	dB dB	2.25 4.5	-2.25 -4.5	note 1	R _L = 600 Ω; C _L = 50 pF; f = 1 MHz (see Fig. 16)
V _(p-p)	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5	tice.	$R_L = 600 \ \Omega$; $C_L = 50 \ pF$; $f = 1 \ MHz \ (E_1, E_2 \ or S_n)$; square-wave between V_{CC} and GND , $t_r = t_f = 6 \ ns$) (see Fig. 17)
f _{max}	minimum frequency response (-3dB)	160 170	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	$R_L = 50 \Omega$; $C_L = 10 pF$ (see Figs 13 and 14)
C _S	maximum switch capacitance independent (Y) common (Z)	5 12	pF pF		015		est 1 Metess

Notes to AC characteristics

 V_{is} is the input voltage at an nY $_{n}$ or nZ terminal, whichever is assigned as an input. V_{os} is the output voltage at an nY $_{n}$ or nZ terminal, whichever is assigned as an output.

1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω). 2. Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

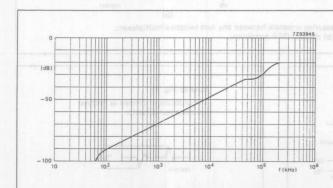
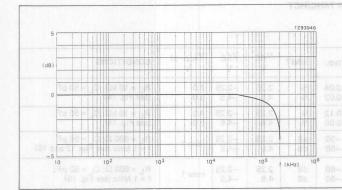


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions: V_{CC} = 4.5 V; GND = 0 V; V_{EE} = -4.5 V; R_L = 50 Ω ; R_{source} = 1 k Ω .

Fig. 13 Typical frequency response.

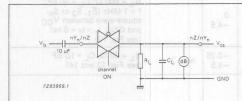


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

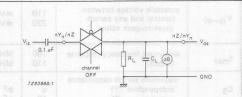


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

$$V_{1s} = \bigcap_{\substack{0,1 \ \mu \in \\ \text{ON}}} \bigcap_{\substack{n \in \\ \text{NL}}} \bigcap_{\substack{n \in \\ \text{NL$$

Fig. 16 Test circuits for measuring crosstalk between any two switches/multiplexers. (a) channel ON condition; (b) channel OFF condition.

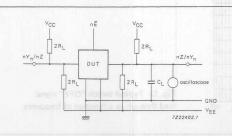
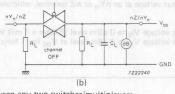
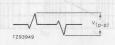


Fig. 17 Test circuit for measuring crosstalk between control and any switch.



Note to Fig. 17

The crosstalk is defined as follows (oscilloscope output):



AC WAVEFORMS

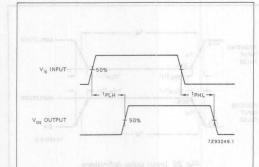


Fig. 18 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

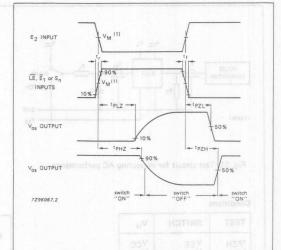


Fig. 19 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 19

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3$ V; $V_I = GND$ to 3 V.

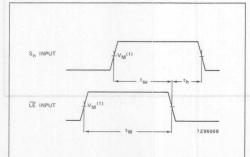


Fig. 20 Waveforms showing the set-up and hold times from S_n inputs to \overline{LE} input, and minimum pulse width of $\overline{LE}.$

Note to Fig. 20

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

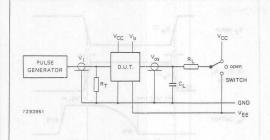


Fig. 21 Test circuit for measuring AC performance.

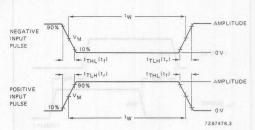


Fig. 22 Input pulse definitions.

Conditions

TEST	SWITCH	Vis	
^t PZH ^t PZL ^t PHZ ^t PLZ others	VEE VCC VEE VCC open	VCC VEE VCC VEE pulse	ig. 19 Waveforms show lose to Fig. 19 1) HC : V _M = 50% V ₁

			t _r ; t _f					
FAMILY	AMPLITUDE	VM	f _{max} ; PULSE WIDTH	OTHER				
74HC	Vcc	50%	< 2 ns	6 ns				
74HCT	3.0 V	1.3 V	< 2 ns	6 ns				

Definitions for Figs 21 and 22:

- C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
- R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.
- pulse generator.

 t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

BCD UP/DOWN COUNTER

FEATURES

- Output capability: standard
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4510 are high-speed Si-gate CMOS devices and are pin compatible with the "4510" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4510 are edge-triggered synchronous up/down BCD counters with a clock input (CP), an up/down count control input (UP/\overline{DN}) , an active LOW count enable input (\overline{CE}) , an asynchronous active HIGH parallel load input (PL), four parallel inputs (Do to D3), four parallel outputs (Q₀ to Q₃), an active LOW terminal count output (TC), and an overriding asynchronous master reset input (MR).

Information on D_0 to D_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. With PL LOW, the counter changes on the LOW-to-HIGH transition of CP if $\overline{\text{CE}}$ is LOW. UP/DN determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, $\overline{\text{TC}}$ is LOW when Q_0 and Q_3 are HIGH and \overline{CE} is LOW. When counting down, \overline{TC} is LOW when Q_0 to Q_3 and \overline{CE} are LOW. A HIGH on MR resets the counter (Q_0 to Q_3 = = LOW) independent of all other input conditions.

Logic equation for terminal count:

$$\overline{TC} = \overline{\overline{CE}} \cdot \left\{ (UP/\overline{DN}) \cdot Q_0 \cdot Q_3 + \cdots + (\overline{UP/\overline{DN}}) \cdot \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \right\}$$

SYMBOL	DADAMETED	CONDITIONS	TYF	UNIT		
STWIBOL	PARAMETER	CONDITIONS	нс	нст	UNIT	
^t PHL [/] ^t PLH	propagation delay CP to Q _n	C _L = 15 pF V _{CC} = 5 V	21	23	ns	
fmax	maximum clock frequency	ACC = 2 A	57	58	MHz	
CI	input capacitance	WWOOLED!	3.5	3.5	pF	
C _{PD} power dissipation capacitance per packa		notes 1 and 2	50	53	pF	

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

f; = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF

VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

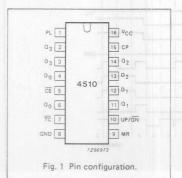
2. For HC the condition is $V_I = GND$ to V_{CC} For HCT the condition is VI = GND to VCC - 1.5 V

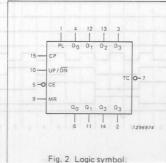
PACKAGE OUTLINES

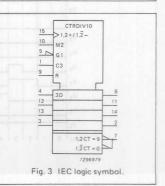
16-lead DIL; plastic (SOT38Z). 16-lead mini-pack; plastic (SO16; SOT109A).

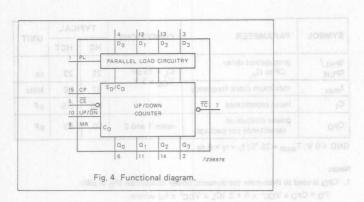
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PL	parallel load input (active HIGH)
4, 12, 13, 3	D ₀ to D ₃	parallel inputs
5	CE	count enable input (active LOW)
6, 11, 14, 2	Q ₀ to Q ₃	parallel outputs
7	TC	terminal count output (active LOW)
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
10	UP/DN	up/down control input
15	СР	clock input (LOW-to-HIGH, edge-triggered)
16	Vcc	positive supply voltage









FUNCTION TABLE

MR	PL	UP/DN	CE	СР	MODE
L	Н	X	X	X 2317	parallel load
L	L	X	Н	X	no change
L	L	L LA	enritis a	OPI Timeler	count down
L	L	Н	L	1	count up
Н	X	X	X	X	reset

H = HIGH voltage level AOLTOMUS CMA 3MAM

L = LOW voltage level

(HE)H evidas) sugiCE

X = don't care

↑ = LOW-to-HIGH clock transition

UP/DN

D₁
D₂
D₃

Q₁ Q₂ Q₃

BCD UP/DOWN COUNTER

EATURES

bishasis :yandaqa fuguu #

GENERAL DESCRIPTION

ne and are pin age of the companies of the companies and are pin another with the "ACTO" of the ACTO" at the omplies of the companies with the "ACTO" of the omplies with JEDEC standard on TA. The TAHC/HCTABTO are adgratingered clock input (CP), an up/down count count enable input (CE), an asynchronous court enable input (CE), as a synchronous crew HIGH parallel load input (PL), and are learnied inputs (DQ to Dg), four are parallel inputs (DQ to Dg), an active are also upper EQ to Dg), an active are are output EQ to Dg), and are active are provided to the count output TAMC and are counter than the count output TAMC and are counter than the count output TAMC and are

uncertainty asymptonous, master reset input (MRI).

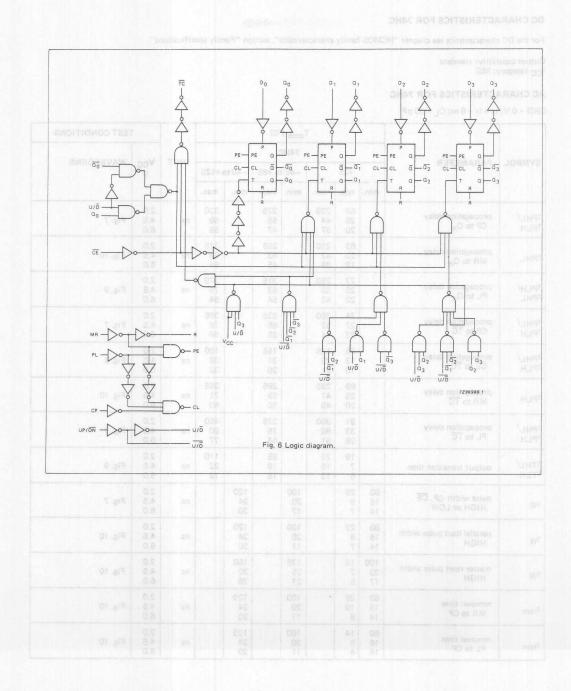
The counter while PL is HIGH, independent the counter while PL is HIGH, independent of all orbits input gendloons except the of all orbits input gendloons except the HIGH transition of OP if CE is LOW.

The counter changes in the LOW-to-HIGH transition of OP if CE is LOW.

TOUR! HIGH for counting up LOW for counting up LOW for bounting up. TC is sounting up. TC is

7296978.1

Fig. 5 Timing diagram.



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

	4 1 4 1		T		Tamb	°C)			7		TEST CONDITIONS	
SYMBOL	51 - 31 - 31 - 31 - 31 - 31 - 31 - 31 -	20	Ц	39	74H	С	4 34		UNIT		WANTEGRAG	
SAMBOL	PARAMETER	+25			-40	to +85	-40 t	-40 to +125		VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.	1-0(Å	
^t PHL/	propagation delay CP to Q _n	٥	69 25 20	220 44 37		275 55 47	7.4	330 66 56	ns	2.0 4.5 6.0	Fig. 7	
[‡] PHL	propagation delay MR to Q _n		63 23 18	210 42 36		265 53 45	<u></u>	315 63 54	ns	2.0 4.5 6.0	Fig. 10	
^t PLH/ ^t PHL	propagation delay PL to Q _n	Å	77 28 22	250 50 43	T.	315 63 54	Å	375 75 64	ns	2.0 4.5 6.0	Fig. 9	
t _{PHL} /	propagation delay CP to TC	店	74 27 22	260 52 44	1111 2011 2011 2011	325 65 55	976 501	395 78 66	ns	2.0 4.5 6.0	Fig. 7	
t _{PHL} /	propagation delay CE to TC	o I	36 13 10	125 25 21	01	155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8	
^t PLH	propagation delay MR to TC		69 25 20	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	Fig. 10	
^t PHL/ ^t PLH	propagation delay PL to TC		91 33 26	300 60 51	alped	375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 9	
^t THL/ ^t TLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 9	
t₩	pulse width CP, CE HIGH or LOW	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
t _W	parallel load pulse width HIGH	80 16 14	22 8 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10	
t _W	master reset pulse width HIGH	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 10	
^t rem	removal time MR to CP	80 16 14	28 10 8	•	100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10	
t _{rem}	removal time PL to CP	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10	

							Tamb (°C)			390	3= 10	TEST COND	ITIONS
SYMBOL	CHOO TEST			74HC								V	WAVEFORMS	
	PARAMET			+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
	WAVEFOR			min.	typ.	max.	min.	max.	min.	max.		Aa	FEMARAS	JOEMYS
t _{su}	set-up time UP/DN to			100 20 17	30 11 9	.xsn	125 25 21	,xem	150 30 26	aim	ns	2.0 4.5 6.0	Fig. 8	Visit
t _{su}	set-up time CE to CP	4.6	an	100 20 17	19 7 6	E.	125 25 21	12	150 30 26		ns	2.0 4.5 6.0	Fig. 8	1H43
t _{su}	set-up time D _n to PL	4.5	.sn	100 20 17	17 6 5	81	125 25 21	83	150 30 26		ns	2.0 4.5 6.0	Fig. 11	7H8; /H78;
^t h	hold time CE to CP	4.5	En-	5 5 5	0 0 0	0	5 5 5	18	5 5 5		ns	2.0 4.5 6.0	Fig. 8	/6H6/ 6FH 6H36/
t _h	hold time D _n to PL	4.6	80	3 3 3	-6 -2 -2	63	3 3 3	Gi	3 18		ns	2.0 4.5 6.0	Fig. 11	HJ97
^t h	hold time UP/DN to	CP CP	an	0 0	-19 -7 -6	63	0 0 0	88	0 0		ns	2.0 4.5 6.0	Fig. 8) 1993 1997 1997
f _{max}	maximum of frequency		an	6.0 30 35	17 52 62		4.8 24 28	- 61	4.0 20 24	18	MHz	2.0 4.5 6.0	Fig. 7	HJT?

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (Δ ICC) for a unit load of 1 is given in the family specifications. To determine Δ ICC per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT							
D _n CE	0.75 1.00							
UP/DN CP	1.00							
MR	1.50							

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_f = t_f = 6 \text{ ns; } C_L = 50 \text{ pF}$

284	VGC WAVEFOR					T _{amb} (°C)				TEST CONDITIONS			
			e125	02.03-	+85	74HC	т	+25				WAVE COME		
SYMBOL	PARAMETER		max.	+25	, KEN	-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS		
			min.	typ.	max.	min.	max.	min.	max.			smit qu-tee		
^t PHL/ ^t PLH	propagation delay CP to Q _n			27	50	13	63	6	75	ns	4.5	Fig. 7		
^t PHL	propagation delay MR to Ω _n			25	42	25	53	3	63	ns	4.5	Fig. 10		
^t PLH [/]	propagation delay PL to Q _n	an I		28	53	25	66	57	80	ns	4.5	Fig. 9		
t _{PHL} /	propagation delay CP to TC			29	58		73	0	87	ns	4.5	Fig. 7		
t _{PHL} /	propagation delay CE to TC	871		17	31		39	0	47	ns	4.5	Fig. 8		
^t PLH	propagation delay MR to TC	ns		31	50	1	63	2-2-	75	ns	4.5	Fig. 10		
^t PHL [/] ^t PLH	propagation delay	an		35	68	1 8	85	-19	102	ns	4.5	Fig. 10		
t _{THL} /	output transition ti	me		7	15	8.4	19	-6	22	ns	4.5	Fig. 9		
tW	pulse width CP, CE HIGH or LOW	37110	16	9		20		24	35	ns	4.5	Fig. 7		
tw	parallel load pulse v HIGH	width	16	6		20		24		ns.	4.5	Fig. 10		
tw	master reset pulse v HIGH	vidth	20	4	noizaez	25	taracter	30	SMOS	ns 1930s	4.5	Fig. 10		
^t rem	removal time MR to CP		23	13		29		35		ns	4.5	Fig. 10		
^t rem	removal time	egs yümi olad əldə	17	10	aid to	21	nu a tol soi timu	26	urrent i	ns due	4.5	Fig. 10 be to sule of		
t _{su}	set-up time UP/DN to CP		20	12		25		30		ns	4.5	Fig. 8 // 10		
t _{su}	set-up time CE to CP		20	6		25		30		ns	4.5	Fig. 8		
t _{su}	set-up time D _n to PL		20	6		25		30		ns	4.5	Fig. 11		
t _h	hold time CE to CP		5	0		5		5		ns	4.5	Fig. 8		
th	hold time D _n to PL		5	0		5		5		ns	4.5	Fig. 11		
^t h	hold time UP/DN to CP		0	-5		0		0		ns	4.5	Fig. 8		
f _{max}	maximum clock pu	lse	30	53		24		20		MHz	4.5	Fig. 7		

AC WAVEFORMS

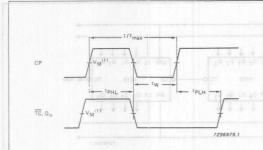


Fig. 7 Waveforms showing the clock (CP) to output (Q_n) and terminal count (\overline{TC}) propagation delays, the clock pulse width and the maximum clock pulse frequency.

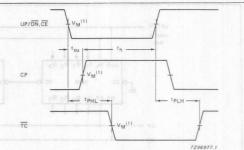


Fig. 8. Waveforms showing the set-up and hold times from count enable ($\overline{\text{CE}}$) and up/down (UP/ $\overline{\text{DN}}$) control inputs to the clock pulse (CP), the propagation delays from UP/ $\overline{\text{DN}}$, $\overline{\text{CE}}$ to $\overline{\text{TC}}$.

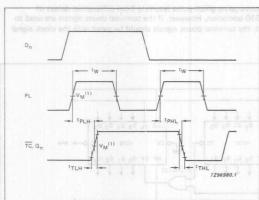


Fig. 9 Waveforms showing the preset enable pulse width, preset enable to output delays and output transition times.

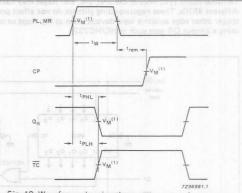


Fig. 10 Waveforms showing the master reset pulse, master reset to terminal count and \mathbf{Q}_{n} delay and master reset to clock removal time.

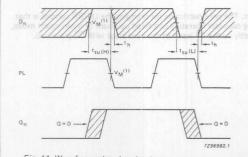
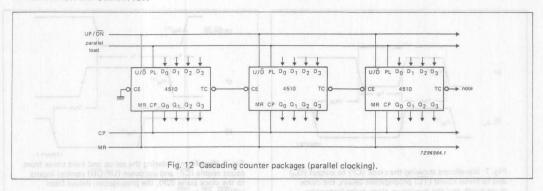


Fig. 11 Waveforms showing the data set-up and hold times to parallel load (PL).

Note to AC waveforms

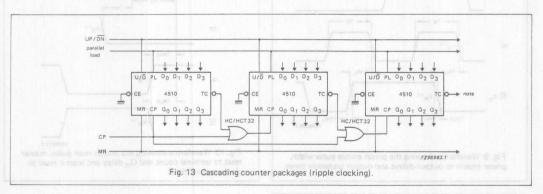
(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION



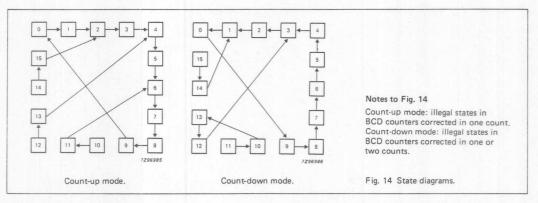
Note to Fig. 12

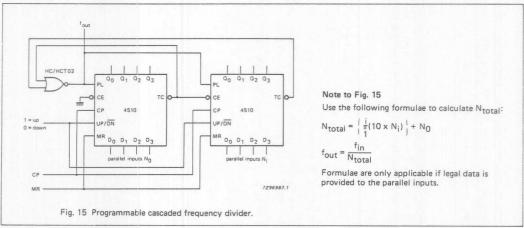
Terminal count (TC) lines at the 2nd, 3rd, etc. stages may have a negative-going glitch pulse resulting from differential delays of different 4510s. These negative-going glitches do not affect proper 4510 operation. However, if the terminal count signals are used to trigger other edge sensitive logic devices, such as flip-flops or counters, the terminal count signals should be gated with the clock signal using a 2-input OR gate such as HC/HCT32.



Note to Fig. 13

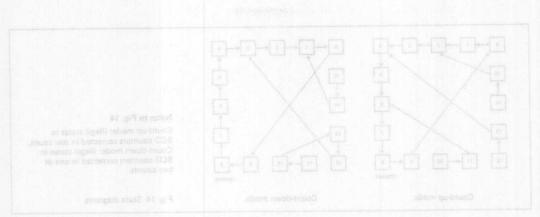
Ripple clocking mode: the UP/\overline{DN} control can be changed at any count. The only restriction on changing the UP/\overline{DN} control is that the clock input to the first counting stage must be HIGH. For cascading counters operating in a fixed up-count or down-count mode, the OR gates are not required between stages and \overline{TC} is connected directly to the CP input of the next stage with \overline{CE} grounded.

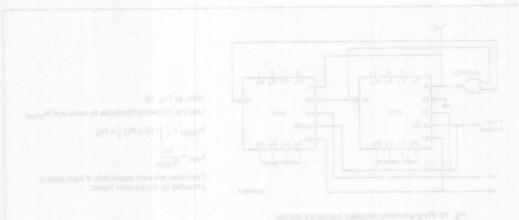




	paralle	l inputs	count-up	count-down		
D ₃	D ₂	D ₁	D ₀	n	n	
0	0	0	0	9	*	
0	0	0	1	8	1	
0	0	1	0	7	2	
0	0	1	1	6	3	
0	1	0	0	5	4	
0	1	0	1	4	5	
0	1	1	0	3	6	
0	1	1	1	2	7	
1	0	0	0	1	8	
1	0	0	1		9	

^{*} no count; fout is HIGH





HBIH ti suo! cinuos an "

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER

FEATURES

- Latch storage of BCD inputs
- Blanking input
- Lamp test input
- Driving common cathode LED displays
- Guaranteed 10 mA drive capability per output
- Output capability: non-standard
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4511 are high-speed Si-gate CMOS devices and are pin compatible with "4511" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

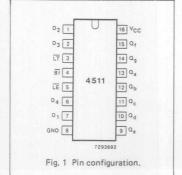
The 74HC/HCT4511 are BCD to 7-segment latch/decoder/drivers with four address inputs (D₁ to D₄), an active LOW latch enable input (\overline{LE}), an active LOW ripple blanking input ($\overline{B1}$), an active LOW lamp test input (\overline{LT}), and seven active HIGH segment outputs (Q_a to Q_q).

When \overline{LE} is LOW, the state of the segment outputs $(Q_a \text{ to } Q_g)$ is determined by the data on D_1 to D_4 .

When $\overline{\text{LE}}$ goes HIGH, the last data present on D₁ to D₄ are stored in the latches and the segment outputs remain stable. When $\overline{\text{LT}}$ is LOW, all the segment outputs are HIGH independent of all other input conditions. With $\overline{\text{LT}}$ HIGH, a LOW on $\overline{\text{BI}}$ forces all segment outputs LOW. The inputs $\overline{\text{LT}}$ and $\overline{\text{BI}}$ do not affect the latch

APPLICATIONS

- Driving LED displays
- Driving incandescent displays
- Driving fluorescent displays
- Driving LCD displays
- Driving gas discharge displays



SYMBOL PA			TYF		
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
tPHL/ tPLH	propagation delay D _D to Q _n LE to Q _n BI to Q _n LT to Q _n	C _L = 15 pF V _{CC} = 5 V	24 23 19 12	24 24 20 13	ns ns ns
CI	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per latch	notes 1 and 2	64	64	pF

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD ×
$$VCC^2$$
 × f_i + Σ (CL × VCC^2 × f_o) where:

FD - CPD x VCC x 11 + 2 (CL x VCC x 16) When

fo = output frequency in MHz VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V_{\parallel} = GND to VCC For HCT the condition is V_{\parallel} = GND to VCC - 1.5 V

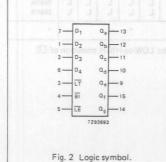
PACKAGE OUTLINES

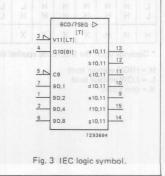
16-lead DIL; plastic (SOT38Z).

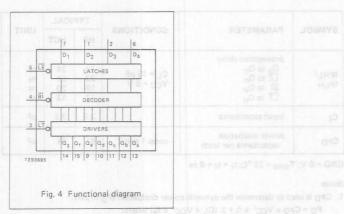
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3 4 14	UT J	lamp test input (active LOW)
4 - E H	BI	ripple blanking input (active LOW)
5	LE	latch enable input (active LOW)
7, 1, 2, 6	D ₁ to D ₄	BCD address inputs
8 8 H	GND	ground (0 V)
13, 12, 11, 10, 9, 15, 14	Q _a to Q _g	segments outputs
16	Vcc	positive supply voltage







FUNCTION TABLE

		1	NPUT	rs					01	UTPU	TS			DISPLAY
LE	BI	LT	D ₄	D ₃	D ₂	D ₁	Qa	Qb	Qc	Q_d	Qe	Qf	Qg	TOMAS
X	X	L	X	X	X	X	Н	Н	Н	Н	Has	Н	Но	8 2 30 8
X	L	Н	X	X	X	×	L	L	P 18	E	Los	L	L	blank
	H H H	HHHH		L L	L H	L H L OH O	H L H	H H H	H H L H	H H H	H H H	H L	L H H	0 1230 M 2 3.00 MA
	H H H	H H H	L (1)	ннн	L H H	L H L	L H L H	H L L	H H H	L H H L	LHL	HHHL	H H L	4 5 6 7
	H H H	TITI	TITI		L H H	LHLH	H H L	H H L	HHLL	HLLL	HLUL	HHLL	H	8 9 blank blank
L L L	H H H	H H H H	H H H	H H H	LLHH	L H L H	L L L	L L L	L L L	L L L	L L L	L L L	L L L	blank blank blank blank
Н	Н	Н	X	X	X	×				* 0	-10	7	a	*

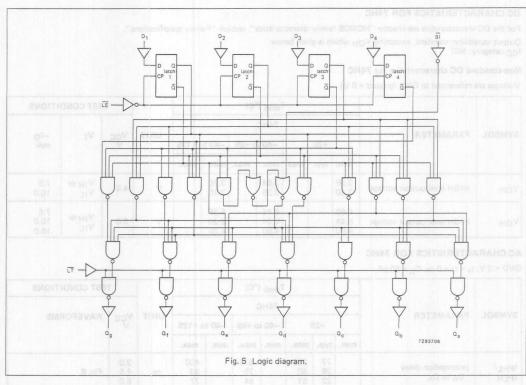
* Depends upon the BCD-code applied during the LOW-to-HIGH transition of LE.

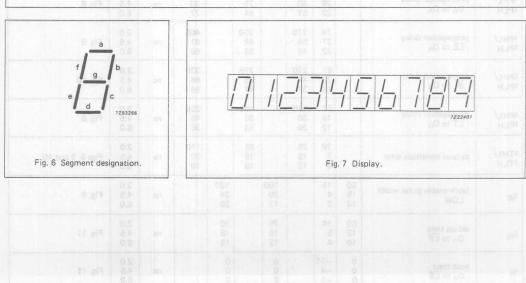
H = HIGH voltage level

L = LOW voltage level

X = don't care







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Output capability: standard, excepting VOH which is given below ICC category: MSI

Non-standard DC characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER				r _{amb} (°C)		TEST CONDITIONS				
		74HC										
		+25			-40 to +85		-40 to +125		UNIT	VCC	VI	−lo mA
		min.	typ.	max.	min.	max.	min.	max.				
Vон	HIGH level output voltage	3.98 3.60		Ì	3.84 3.35	71	3.70 3.10	9	v	4.5	VIH or	7.5 10.0
Vон	HIGH level output voltage	5.60 5.48 4.80			5.45 5.34 4.50		5.35 5.20 4.20		V	6.0	VIH or VIL	7.5 10.0 15.0

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	U				Tamb	(°C)	U.				TEST CONDITIONS
OVMON	, i	74HC								. 5	7
SYMBOL	PARAMETER		+2	5	-40 to +85			-40 to +125		VCC	WAVEFORMS
	entert de	min.	typ.	max.	min.	max.	min.	max.			
tPHL/	propagation delay Dn to Qn		77 28	300 60	gic dia	375 75	F	450 90	ns	2.0	Fig. 8
T LIT	311 -5 -11		22	51		64		77		6.0	
tPHL/ tPLH	propagation delay LE to Q _n		74 27 22	270 54 46		330 68 58		405 81 69	ns	2.0 4.5 6.0	Fig. 9
tPHL/ tPLH	propagation delay BI to Q _n		61 22 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 10
tPHL/ tPLH	propagation delay LT to Q _n		41 15 12	150 30 26	111	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
tTHL/ tTLH	output transition time	7. 91	19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8, 9 and 10
tw	latch enable pulse width LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t _{su}	set-up ti <u>me</u> D _n to LE	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 11
^t h	hold time D _n to LE	0 0 0	-11 -4 -3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard, excepting $V_{\mbox{OH}}$ which is given below $I_{\mbox{CC}}$ category: MSI

Non-standard DC characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

		T _{amb} (°C)								TEST CONDITIONS		
SYMBOL	PARAMETER				74HC	Т	LIBUT	1		1-		
		+ 25			-40 to +85		-40 to +125		UNIT	VCC	VI	mA
		min.	typ.	max.	min.	max.	min.	max.				
Vон	HIGH level output voltage	3.98 3.60	3		3.84 3.35		3.70 3.10	3) rugni Bysleb W	er V primyo	4.5	VIH or VIL	7.5

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

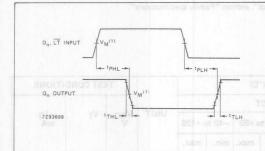
INPUT	UNIT LOAD COEFFICIENT
LT, LE	1.50 0.30

AC CHARACTERISTICS FOR 74HCT

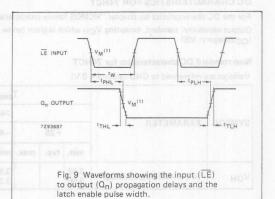
 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

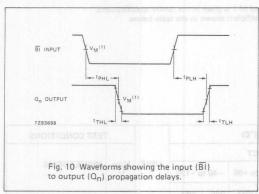
					T_{amb}	(°C)					TEST CONDITIONS
SYMBOL	PARAMETER				74H	СТ	UNIT				
STIVIBOL	PARAMETER	elvsWi di ascri	+2	5	-40 to +85			-40 to +125		VCC	
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/ tPLH	propagation delay D _n to Ω _n	libni a	28	60	M IT	75		90	ns	4.5	Fig. 8
t _{PHL} /	propagation delay LE to Ω _n		27	54	90	68		81	ns	4.5	Fig. 9
^t PHL/ ^t PLH	p <u>ro</u> pagation delay BI to Q _n		23	44		55		66	ns	4.5	Fig. 10
^t PHL/	p <u>ro</u> pagation delay LT to Q _n		16	30		38		45	ns	4.5	Fig. 8
t _{THL} /	output transition time		7	15		19		22	ns	4.5	Figs 8, 9 and 10
tw	latch enable pulse width LOW	16	5		20		24		ns	4.5	Fig. 9
t _{su}	set-up ti <u>me</u> D _n to LE	12	5		15		18		ns	4.5	Fig. 11
-h	hold time D _n to LE	0	-4		0		0		ns	4.5	Fig. 11

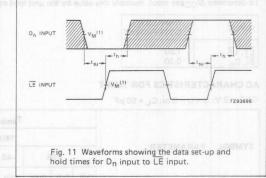
AC WAVEFORMS



 \underline{Fig} . 8 Waveforms showing the input (D_n, LT) to output (Q_n) propagation delays and the output transition times.







Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

Note to Fig. 11

The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION DIAGRAMS

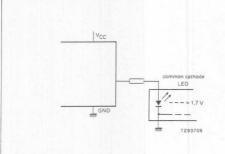


Fig. 12 Connection to common cathode LED display readout.

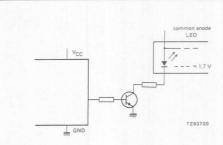
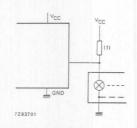


Fig. 13 Connection to common anode LED display readout.



(1) A filament pre-warm resistor to reduce thermal shock and to increase effective cold resistance of the filament is recommended.

Fig. 14 Connection to incandescent display readout.

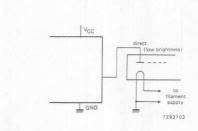


Fig. 15 Connection to fluorescent display readout.

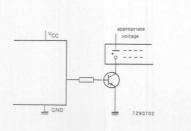


Fig. 16 Connection to gas discharge display readout.

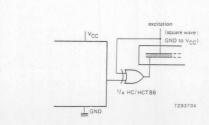
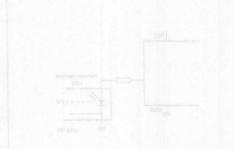
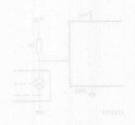


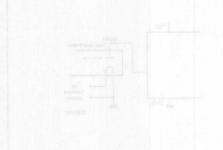
Fig. 17 Connection to LCD display readout. (Direct DC drive is not recommended as it can shorten the life of LCD displays).

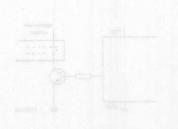


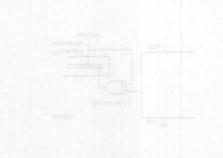












4-TO-16 LINE DECODER/DEMULTIPLEXER WITH INPUT LATCHES

FEATURES

- Non-inverting outputs in the large of t
- Output capability: standard and bA
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4514 are high-speed Si-gate CMOS devices and are pin compatible with "4514" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4514 are 4-to-16 line decoders/demultiplexers having four binary weighted address inputs (A₀ to A₃), with latches, a latch enable input (LE), and an active LOW enable input (E). The 16 outputs (Q₀ to Q₁₅) are mutually exclusive active HIGH. When LE is HIGH. the selected output is determined by the data on An. When LE goes LOW, the last data present at An are stored in the latches and the outputs remain stable. When E is LOW, the selected output, determined by the contents of the latch, is HIGH. At E HIGH, all outputs are LOW. The enable input (E) does not affect the state of the latch.

When the "4514" is used as a demultiplexer, $\overline{\mathsf{E}}$ is the data input and Ao to A3 are the address inputs.

	212145752	CONDITIONS	TYF	UNIT	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
^t PHL [/]	propagation delay An to Qn	C _L = 15 pF V _{CC} = 5 V	23	26	ns
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	44	45	pF

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

 $PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$ where:

fi = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is VI = GND to VCC

For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 V$

PACKAGE OUTLINES

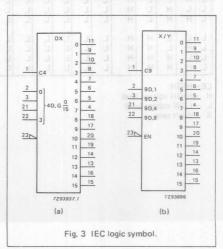
24-lead DIL; plastic (SOT101A). 24-lead mini-pack; plastic (SO24; SOT137A).

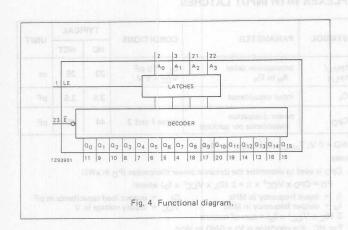
PIN DESCRIPTION DE SCRIPTION DESCRIPTION D

PIN NO.	SYMBOL	NAME AND FUNCTION			
1	JLE J J J	latch enable input (active HIGH)	1	14	
2, 3, 21, 22	A ₀ to A ₃	address inputs			
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	Q ₀ to Q ₁₅	multiplexer outputs (active HIGH)			
12	GND	ground (0 V)			
23	E	enable input (active LOW)			
24	Vcc	positive supply voltage			









APPLICATIONS

- Hexadecimal/BCD decoding

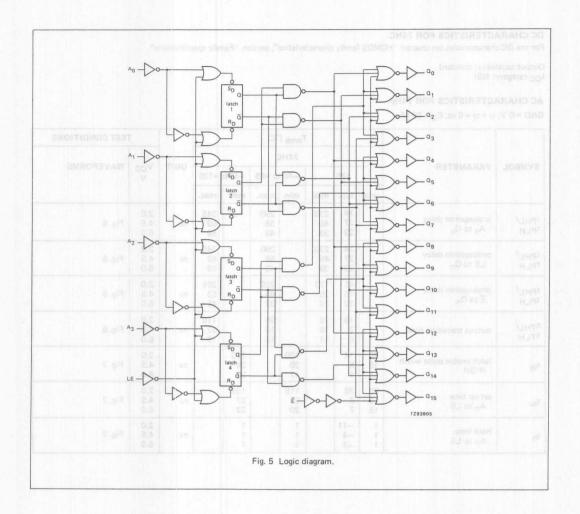
FUNCTION TABLE

	1	NPU	TS							(AII	HTC	OUT	PUT	S	bag	245		34	Hi) H a
Ē	A ₀	A ₁	A ₂	А3	α ₀	01	02	03	04	Q ₅	α ₆	07	08	Qg	Q ₁₀	011	012	Q ₁₃	Q ₁₄	Q ₁₅
Н	X	X	×	Хио	Lov	L	L	Lia	L	L	Ljo	L	L	L	L	L	L	L	L	L
L L L	L H L H	L H H	L L L	L set	H) 1	H L L	LHL	L L H	L L L		L L				L L L	L				L
LLLL	L H L	L H H	HHHH	L L L	L L L L	L L L	L L L	L L L	H L L	L H L	L H L	L			L L L		L L L		L L L	L L L L
LLLL	L H L	L H H	L L L	H H H	Estle L L L	LVIII L L	L L L	L L L	L L L	L L L	L L L	L20 L L	HLLL	L H L	L L H L	L L H	L L L		L L L	L L L
LLLL	L H L	L H H	H H H	H H H	LLLL	L L L		L L L	L L L		L L L	LLLL	L L L		L L L		H	LHLL	L H L	L L L

LE = HIGH

H = HIGH voltage levelL = LOW voltage level

X = don't care



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	10-<<	TH			T _{amb} (°C)		C	4		TEST CONDITIONS	
OVER DOL	30-<<				74H	С			LINUT	5-1	WAVEFORMS	
SYMBOL	PARAMETER	+25			-40	to +85	-40 t	0+125	UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay		74 27 22	230 46 39	Y	290 58 49	108	345 69 59	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} /	propagation delay LE to Q _n		74 27 22	230 46 39	0	290 58 49	1000	345 69 59	ns	2.0 4.5 6.0	Fig. 6	
tphl/	propagation delay E to Q _n	Ħ	41 15 12	175 35 30	0	220 44 37	- 5 m	265 53 45	ns	2.0 4.5 6.0	Fig. 6	
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16	_5_	110 22 19	ns	2.0 4.5 6.0	Fig. 6	
tw	latch enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
t _{su}	set-up time An to LE	90 18 15	25 9 7	(- •<	115 23 20		135 27 23	d	ns	2.0 4.5 6.0	Fig. 7	
^t h	hold time A _n to LE	1 1 1	-11 -4 -3		1 1 1		1 1 1		ns	2.0 4.5 6.0	Fig. 7	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
An	0.65
LE	1.40
Ē	1.00

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	(1,5) and the set-up and hold on hold times are shown as po				T _{amb} (°C)		iziknevi z	ustuo sa	t time an	TEST CONDITIONS
	PARAMETER		ed ye	m sus	74HC	Т			UNIT		WAVEFORMS
SYMBOL			+25		-40 to +85		-40 to +125		Olviii	VCC	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			smoltway SA of sto
tPHL/	propagation delay A _n to Q _n	s india icrable	30	55		69		83	ns 2 at	4.5	Fig. 6
t _{PHL} /	propagation delay LE to Ω _n		29	50		63		75	ns	4.5	Fig. 6
t _{PHL} / t _{PLH}	propagation delay E to On		17	40		50		60	ns	4.5	Fig. 6
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t _W	latch enable pulse width HIGH	16	4		20		24		ns	4.5	Fig. 7
t _{su}	set-up time A _n to LE	18	9		23		27		ns	4.5	Fig. 7
th	hold time A _n to LE	3	-3		3		3		ns	4.5	Fig. 7

AC WAVEFORMS

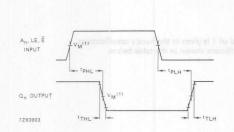


Fig. 6 Waveforms showing the input (A_n, LE, \overline{E}) to output (Q_n) propagation delays and the output transition times.

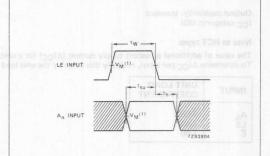


Fig. 7 Waveforms showing the minimum pulse width of the latch enable input (LE) and the set-up and hold times for LE to A_n . Set-up and hold times are shown as positive values but may be specified as negative values.

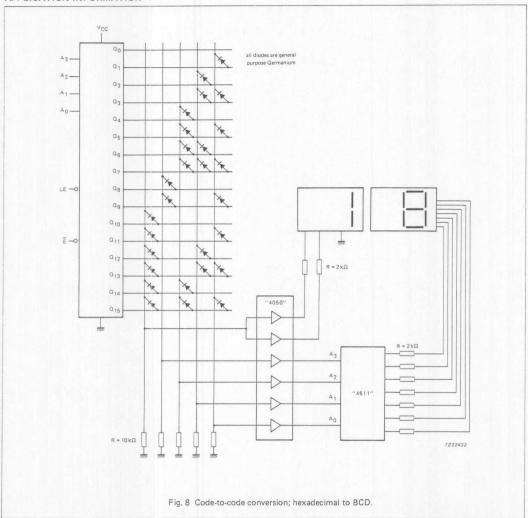
Note to AC waveforms

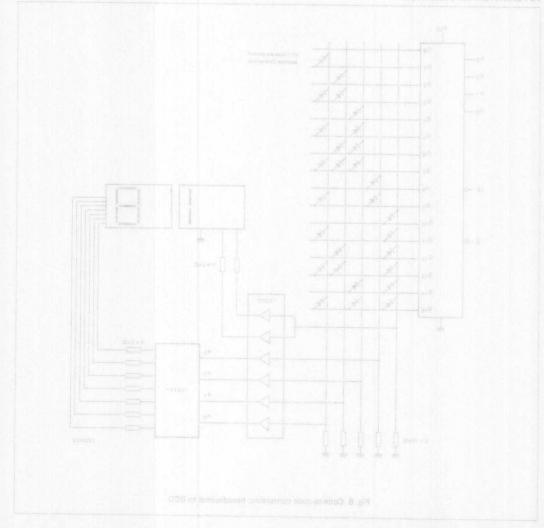
(1) HC : $V_M = 50\%$; $V_1 = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_1 = GND$ to 3 V.

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION INFORMATION





4-TO-16 LINE DECODER/DEMULTIPLEXER WITH INPUT LATCHES; INVERTING

FFATURES

- Inverting outputs
- Output capability: standard
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4515 are high-speed Si-gate CMOS devices and are pin compatible with "4515" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4515 are 4-to-16 line decoders/demultiplexers having four binary weighted address inputs (A_Q to A₃) with latches, a latch enable input (LE), and an active LOW enable input ($\overline{\mathbb{E}}$). The 16 inverting outputs ($\overline{\mathbb{Q}}$) to $\overline{\mathbb{Q}}_{15}$) are mutually exclusive active LOW. When LE is HIGH, the selected output is determined by the data on A_n. When LE goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When $\overline{\mathbb{E}}$ is LOW, the selected output, determined by the contents of the latch, is LOW. When $\overline{\mathbb{E}}$ is HIGH, all outputs are HIGH. The enable input ($\overline{\mathbb{E}}$) does not affect the state of the latch.

When the "4515" is used as a demultiplexer, \overline{E} is the data input and A_0 to A_3 are the address inputs.

01/14001	DADAMETER	CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNII	
tPHL/	propagation delay A_n to \overline{Q}_n	C _L = 15 pF V _{CC} = 5 V	25	26	ns	
CI	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	44	46	pF	

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

Notes

- 1. CPD is used to determine the dynamic power dissipation (PD in μ W):
 - $PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$ where:

 - f_0 = output frequency in MHz
 - $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

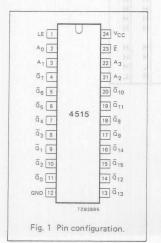
PACKAGE OUTLINES

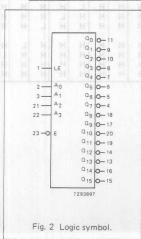
24-lead DIL; plastic (SOT101A).

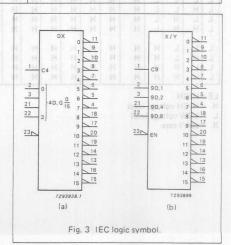
24-lead mini-pack; plastic (SO24; SOT137A).

PIN DESCRIPTION

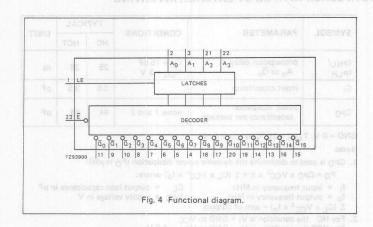
PIN NO.	SYMBOL	NAME AND FUNCTION	Z	x	Н
1.	LE	latch enable input (active HIGH)			
2, 3, 21, 22	A ₀ to A ₃	address inputs			
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19,	ā₀ to ā₁₅	multiplexer outputs (active LOW)			
14, 13, 16, 15	CNID				
12	GND	ground (0 V)			
23	E	enable input (active LOW)			
24	Vcc	positive supply voltage			







VCC = supply voltage in V



APPLICATIONS

- Digital mutliplexing project
- Hexadecimal/BCD decoding

FUNCTION TABLE

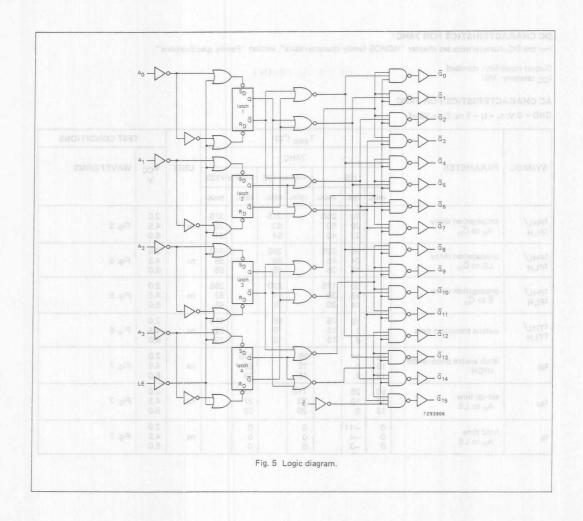
	1	NPU'	TS									OUT	PUT	S						
Ē	A ₀	A ₁	A ₂	A3	\bar{a}_0	₫1	$\bar{\mathbf{Q}}_2$	₫3	<u>a</u> 4	₫5	₫6	₫7	₫8	₫9	₫10	<u>Q</u> 11	₫12	₫13	₫14	₫15
Н	X	X	X	X	H	Н	HA	Н	Н	Н	Н	Н	Н	Н	H	н	Н	н	Н	Н
	LHLH	L H H	LLLWO	L L L L evist	LHHH	H	HHLH	HHHL	HHHH	H H H	HHHH	HHHHH	HHHH	HHHH	H H H	HHHH	H H H H	HHH	ннн	HHHH
	LHLH	L H H	HHHH		HHHH	HHH	H H H	H H H	L H H	H H H	HHLH	HHHL	H H H	H H H H H	HHHH	HHHH	H H H	ннн	ннн	H H H
	L H L	L H H	L L L	H H H	HHHH	H H H	H H H	H H H	H H H	HHHH	H H H	H H H	L H H	H H H	H H L	H H H L	H H H	пппп	H H H	HHHH
LLL	LHLH	L H H	H H H	H H H	1111	H H H	1111	HHHH	H H H	HHHH	HHHH	HHHH	HHHH	HHHH	HHHH	HHH	LHH	HTHH	HHLH	HHHL

LE = HIGH

H = HIGH voltage level

L = LOW voltage level

X = don't care



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	0-4-6				T _{amb} (°C)	L	CH	4		TEST CONDITIONS	
01/11001	5_4_				74H	С		7		J-14	WAVEFORMS	
SYMBOL	PARAMETER	+25			-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} /	propagation delay A_n to \overline{Q}_n		80 29 23	250 50 43		315 63 54	0.4	375 75 64	ns	2.0 4.5 6.0	Fig. 6	
^t PHL [/]	propagation delay LE to $\overline{\Omega}_{n}$		66 24 19	225 45 38	CI.	280 56 48	10 08 E	340 68 58	ns	2.0 4.5 6.0	Fig. 6	
tPHL/	propagation delay E to $\overline{\Omega}_n$		50 18 14	175 35 30	a	220 44 37	1 89	265 53 45	ns	2.0 4.5 6.0	Fig. 6	
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6	
tw	latch enable pulse width HIGH	75 15 13	14 5 4		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 7	
t _{su}	set-up time An to LE	90 18 15	28 10 8	-•<	115 23 20		135 27 23	d	ns	2.0 4.5 6.0	Fig. 7	
^t h	hold time A _n to LE	0 0	-11 -4 -3		0 0		0 0		ns	2.0 4.5 6.0	Fig. 7	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

Note to HCT types

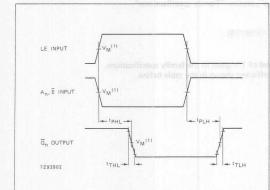
The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
An	0.65
E	1.00

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \ V; t_{\Gamma} = t_{f} = 6 \ ns; C_{L} = 50 \ pF$

			A country	-	Tamb (°C)			A) tuani	TEST CONDITIONS		
mes for	PARAMETER	1) Their			74HC	Т		itlanen	rugius s		WAVEFORMS	
SYMBOL		ecties	+25	out may	-40	to +85	-40 to	o +125	UNIT	VCC		
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/	propagation delay A_n to \overline{Q}_n		30	55		69		83	ns	4.5	Fig. 6	
t _{PHL} / cy is	propagation delay LE to $\overline{\Omega}_{n}$	indias stables	29	50	rt i	63		75	ns	4.5	Fig. 6	
t _{PHL} /	propagation delay \overline{E} to \overline{Q}_n		18	40		50		60	ns	4.5	Fig. 6	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 6	
tw	latch enable pulse width HIGH	16	3		20		24		ns	4.5	Fig. 7	
t _{su}	set-up time A _n to LE	18	9		23		27		ns	4.5	Fig. 7	
^t h	hold time A _n to LE	3	-2		3		3		ns	4.5	Fig. 7	



11

Fig. 6 Waveforms showing the input $(A_n,\, LE,\, \overline E)$ to output $(\overline Q_n)$ propagation delays and the output transition times.

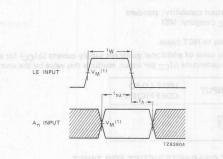


Fig. 7 Waveforms showing the minimum pulse width of the latch enable input (LE) and the set-up and hold times for LE to A_n . Set-up and hold times are shown as positive values but may be specified as negative values.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V. Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

BINARY UP/DOWN COUNTER

FEATURES

- Output capability: standard
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4516 are high-speed Si-gate CMOS devices and are pin compatible with the "4516" of the "40008" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4516 are edge-triggered synchronous up/down 4-bit binary counters with a clock input (CP), an up/down count control input (UP/ \overline{DN}), an active LOW count enable input (\overline{CE}), an asynchronous active HIGH parallel load input (PL), four parallel inputs (D0 to D3), four parallel outputs (Q0 to Q3), an active LOW terminal count output (\overline{TC}), and an overriding asynchronous master reset input (MR).

Information on D_0 to D_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. When PL and \overline{CE} are LOW, the counter changes on the LOW-to-HIGH transition of CP. UP/DN determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, \overline{TC} is LOW when Q_0 to Q_3 are HIGH and \overline{CE} is LOW. When counting down, \overline{TC} is LOW when Q_0 to Q_3 and \overline{CE} are LOW. A HIGH on MR resets the counter (Q_0 to Q_3 = = LOW) independent of all other input conditions.

Logic equation for terminal count:

$$\begin{split} \overline{\mathsf{TC}} &= \overline{\overline{\mathsf{CE}}} \; \cdot \; \left\{ \; \left(\mathsf{UP}/\overline{\mathsf{DN}} \right) \; . \; \mathsf{\Omega}_0 \; . \; \mathsf{\Omega}_1 \; . \; \mathsf{\Omega}_2 \; . \; \mathsf{\Omega}_3 \; + \right. \\ & \left. \; + \; \left(\overline{\mathsf{UP}/\overline{\mathsf{DN}}} \right) \; . \; \overline{\mathsf{Q}}_0 \; . \; \overline{\mathsf{Q}}_1 \; . \; \overline{\mathsf{Q}}_2 \; . \; \overline{\mathsf{Q}}_3 \; \right\} \end{split}$$

SYMBOL		CONDITIONS	TYF	LIBUT	
	PARAMETER	CONDITIONS	нс	нст	UNIT
tPHL/	propagation delay CP to Q _n	C _L = 15 pF - V _{CC} = 5 V	19	19	ns
f _{max}	maximum clock frequency	- vcc - 3 v	45	57	MHz
CI	input capacitance	Visidateu	3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	59	61	pF

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

$$\Sigma$$
 (C_L x V_{CC}² x f₀) = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

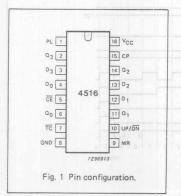
PACKAGE OUTLINES

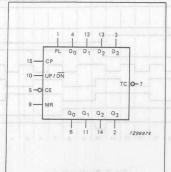
16-lead DIL; plastic (SOT38Z).

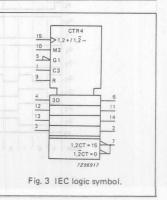
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PL	parallel load input (active HIGH)
4, 12, 13, 3	Do to D3	parallel inputs
5	CE	count enable input (active LOW)
6, 11, 14, 2	Q ₀ to Q ₃	parallel outputs
7	TC	terminal count output (active LOW)
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
10	UP/DN	up/down control input
15	CP	clock input (LOW-to-HIGH, edge-triggered)
16	Vcc	positive supply voltage







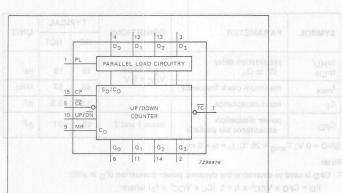


Fig. 4 Functional diagram.

FUNCTION TABLE

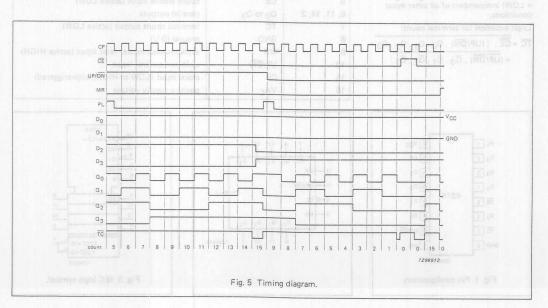
MR	PL	UP/DN	CE	CP and	MODE
L	Н	X	X	X 02	parallel load
L	L	X	(601H0679	X	no change
L	L	L	L	1	count down
L	L	Н	L	1	count up
Н	X	X	X	X	reset

H = HIGH voltage level

L = LOW voltage level minor) rugni

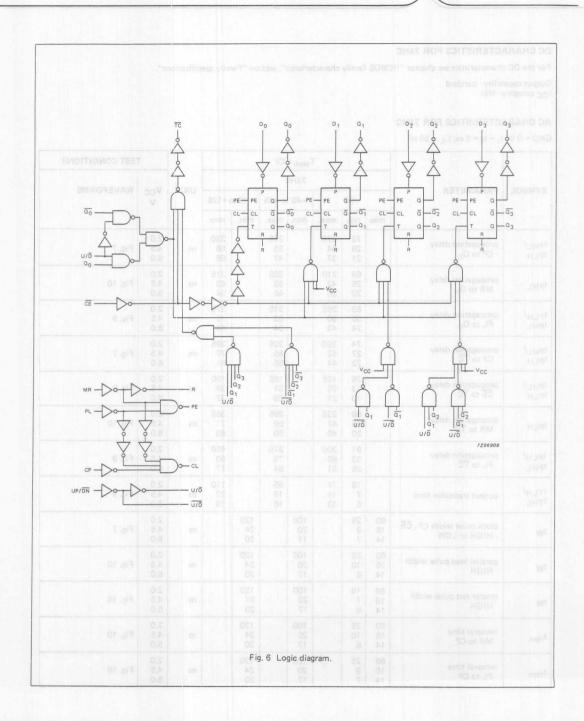
X = dont't care

↑ = LOW-to-HIGH clock transition



fi = input frequency in Mila

to = ourput free



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

	4 1 4		2	4	Tamb ((°C)	7				TEST CONDITIONS	
OVMDOL			T.	Î	74H	С			T	WAVEFORMS		
SYMBOL	PARAMETER	- 91	+25	31	-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS	
	0 10 00 0	min.	typ.	max.	min.	max.	min.	max.			-07	
tPHL/	propagation delay CP to Q _n	-0	72 26 21	220 44 37		275 55 47	100	330 66 56	ns	2.0 4.5 6.0	Fig. 7	
tPHL	propagation delay MR to Ω _n		69 25 20	210 42 36		265 53 45	4	315 63 54	ns	2.0 4.5 6.0	Fig. 10	
tpLH/	propagation delay PL to Q _n		83 30 24	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 9	
^t PHL [/]	propagation delay CP to TC	Δl	74 27 22	260 52 44	Č.	325 65 55	(395 78 66	ns	2.0 4.5 6.0	Fig. 7	
^t PHL [/]	propagation delay CE to TC	T	36 13 10	125 25 21		155 31 26	26) 26	190 38 32	ns	2.0 4.5 6.0	Fig. 8	
^t PLH	propagation delay MR to TC) (S	69 25 20	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	Fig. 10	
t _{PLH} /	propagation delay PL to TC		91 33 26	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 9	
tTLH/ tTHL	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 9	
tw	clock pulse width CP, CE HIGH or LOW	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
tw	parallel load pulse width HIGH	80 16 14	28 10 8		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10	
t _W	master rest pulse width HIGH	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10	
[†] rem	removal time MR to CP	80 16 14	28 10 8		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10	
^t rem	removal time PL to CP	80 16 14	25 9 7	.(1)6/10	100 20 17	el 91	120 24 20		ns	2.0 4.5 6.0	Fig. 10	

AC CHARACTERISTICS FOR 74HC (Cont'd)

	TEST CONDIT		1			T _{amb} (°C)					TEST CONDIT	IONS
SYMBOL	PARAMETER					74H	CITE 1			UNIT	Van	WAVEFORMS	
3111102				+25		-40	to +85	-40 t	o +125	ONT	V _{CC}		JOSMY
		V	min.	typ.	max.	min.	max.	min.	max.				
t _{su}	set-up time UP/DN to CP	E.4 21	100 20 17	30 11 9	1914 - N	125 25 21	18	150 30 26	2	ns	2.0 4.5 6.0	Fig. 8	/JHS
t _{su}	set-up time CE to CP	ts 4.5	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8	JHS
t _{su}	set-up time D _n to PL	5.4 s	100 20 17	17 6 5		125 25 21		150 30 26	E .	ns	2.0 4.5 6.0	Fig. 11	PHIL PHIL PHIL
^t h	hold time CE to CP	4.5	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8	PLB PHU PLB
^t h	hold time D _n to PL	a 4.5	3 3	-6 -2 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 11	HTd
t _h	hold time UP/DN to CP	2,4 ar	0 0 0	-19 -7 -6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 8	JH9 TLH
f _{max}	maximum clock frequency	< pulse	6.0 30 35	16 49 58	20	4.8 24 28	20	4.0 20 24	2 01	MHz	2.0 4.5 6.0	Fig. 7	· W

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D _n	0.75
PL, CE	1.00
UP/DN	1.00
CP	1.25
MR	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

					Tamb	°C)					TEST CONDITIONS
	UNIT VCC WAVEFORM	20			74HC	т				1	YMBOL PARAMETE
SYMBOL	PARAMETER V		+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS
	0.0	min.	typ.	max.	min.	max.	min.	max.			
tPHL/	propagation delay CP to Q _n		28	50		63		75	ns	4.5	Fig. 7
^t PHL	propagation delay MR to Q _n		24	42	0	53		63	ns	4.5	Fig. 10
tPLH/	propagation delay PL to Q _n		32	53	a	66		80	ns	4.5	Fig. 9
tPHL/	propagation delay CP to TC		29	58		73		87	ns	4.5	Fig. 7
tPHL/ tPLH	propagation delay CE to TC		18	31		39		47	ns	4.5	Fig. 8
^t PLH	propagation delay MR to TC		31	50		63	1	75	ns	4.5	Fig. 10 Mod
tPLH/	propagation delay PL to TC		34	68		85	9	102	ns	4.5	Fig. 9
t _{TLH} /	output transition time		7	15		19		22	ns	4.5	Fig. 9
tW	clock pulse width CP, CE HIGH or LOW	16	9	20	20	24	24	030 450 03 450 03 450	ns	4.5	Fig. 7
tw	parallel load pulse width HIGH	16	8		20		24		ns	4.5	Fig. 10
tw	master rest pulse width HIGH	20	5	noises	25	zinetosn	30	nst 201	ns	4.5	Fig. 10
^t rem	removal time MR to CP	23	14		29		35		ns	4.5	Fig. 10
^t rem	removal time PL to CP	17	10	iio zi T l	21	tinue	26	EA1 mar	ns	4.5	Fig. 10 Seque Told of all
t _{su}	set-up time World eld UP/DN to CP	20	11	ide snai	25	baol 1li	30	value by	ns	4.5	Fig. 8
t _{su}	set-up time CE to CP	20	9		25		30		ns	4.5	Fig. 8
t _{su}	set-up time D _n to PL	20	9		25		30		ns	4.5	Fig. 11 50.1 55.2
^t h	hold time CE to CP	10	9		13		15		ns	4.5	Fig. 8 Dar P
^t h	hold time D _n to PL	5	-6		5		5		ns	4.5	Fig. 11
^t h	hold time UP/DN to CP	0	-5		0		0		ns	4.5	Fig. 8
f _{max}	maximum clock pulse frequency	30	52		24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

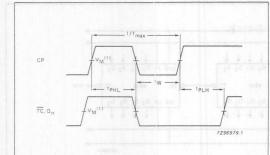


Fig. 7 Waveforms showing the clock (CP) to output (Q_n) and terminal count $(\overline{\mathsf{TC}})$ propagation delays, the clock pulse width and the maximum clock pulse frequency.

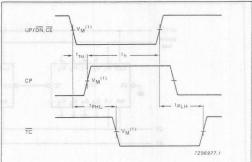


Fig. 8 Waveforms showing the set-up and hold times form count enable ($\overline{\text{CE}}$) and up/down (UP/ $\overline{\text{DN}}$) control inputs to the clock pulse (CP), the propagation delays from UP/ $\overline{\text{DN}}$, $\overline{\text{CE}}$ to $\overline{\text{TC}}$.

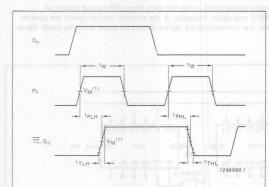


Fig. 9 Waveforms showing the preset enable pulse width, preset enable to output delays and output transition times.

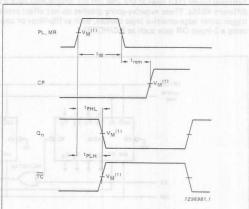


Fig. 10 Waveforms showing the master reset pulse, master reset to terminal count and \mathbf{Q}_n delay and master reset to clock removal time.

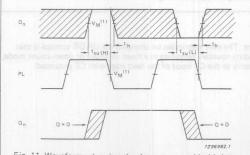
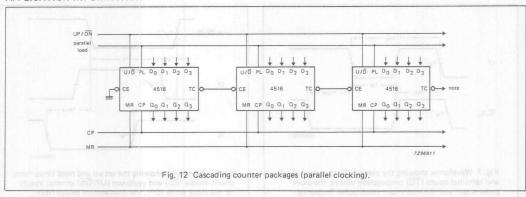


Fig. 11 Waveforms showing the data set-up and hold times to parallel load (PL).

Note to AC waveforms

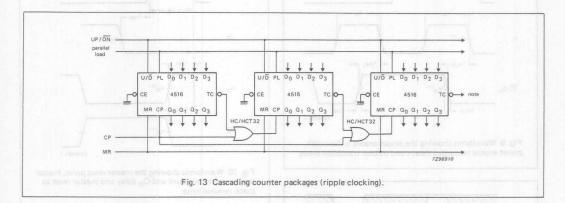
(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION



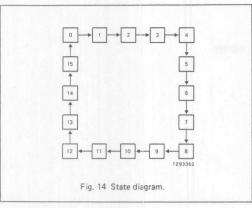
Note to Fig. 12

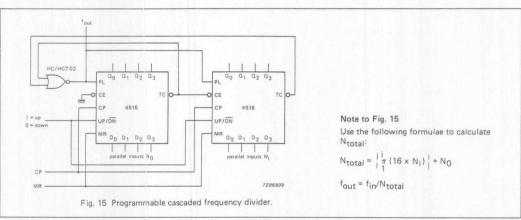
Terminal count (TC) lines at the 2nd 3rd etc. Stages may have a negative-going glitch pulse resulting from differential delays of different 4516s. These negative-going glitches do not affect proper 4516 operation. However, if the terminal count signals are used to trigger other edge-sensitive logic devices, such as flip-flops or counters, the terminal count signals should be gated with the clock signal using a 2-input OR gate such as HC/HCT32.



Note to Fig. 13

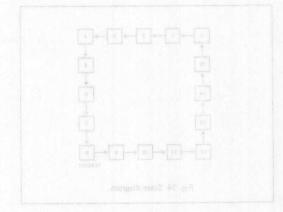
Ripple clocking mode: the UP/\overline{DN} control can be changed at any count. The only restriction on changing the UP/\overline{DN} control is that the clock input to the first counting stage must be "HIGH". For cascading counters operating in a fixed up-count or down-count mode, the OR gates are not required between stages and \overline{TC} is connected directly to the CP input of the next stage with \overline{CE} grounded.

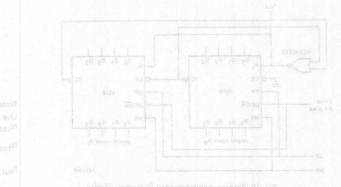




	paralle	l inputs	count-up	count-down	
D ₃	D ₂	D ₁	D ₀	n	n
0	0	0	0	15	
0	0	0	1	14	1
0	0	1	0	13	2
0	0	1	1	12	3
0	1	0	0	11	4
0	1	0	1	10	5
0	1	1	0	9	6
0	1	1	1	8	7
1	0	0	0	7	8
1	0	0	1	6	9
1	0	1	0	5	10
1	0	1	1	4	11
1	1	0	0	3	12
1	1	0	1	2	13
1	1	1	0	1	14
1	1	1	1		15

^{*} no count; fout is HIGH.





no count four is HIGH.

DUAL SYNCHRONOUS BCD COUNTER

FEATURES

- Output capability: standard
- · Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4518 are high-speed Si-gate CMOS devices and are pin compatible with the "4518" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4518 are dual 4-bit internally synchronous BCD counters with an active HIGH clock input (nCP_0) and an active LOW clock input (nCP_1), buffered outputs from all four bit positions (nQ_0 to nQ_3) and an active HIGH overriding asynchronous master reset input (nMR).

The counter advances on either the LOW-to-HIGH transition of nCP0 if nCP1 is HIGH or the HIGH-to-LOW transition of nCP1 if nCP0 is LOW. Either nCP0 or nCP1 may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on nMR resets the counter (nQ0 to nQ3 = LOW) independent of nCP0 and nCP1.

APPLICATIONS

- Multistage synchronous counting
- Multistage asynchronous counting
- Frequency dividers

01/14001			TYP	LIBUT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
tPHL/ tPLH	propagation delay nCP0, nCP1 to nQn		20	24	ns
^t PHL 1	propagation delay nMR to nQn	C _L = 15 pF V _{CC} = 5 V	13	14	ns
fmax	maximum clock frequency		61	55	MHz
CI DIN = h	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per counter	notes 1 and 2	29	27	pF

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD
$$\times$$
 VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

fi = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF

rency in MHz VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V $_{\rm I}$ = GND to V_{CC} For HCT the condition is V $_{\rm I}$ = GND to V_{CC} $_{\rm I}$ - 1.5 V

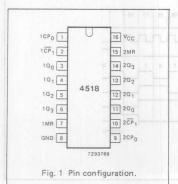
PACKAGE OUTLINES

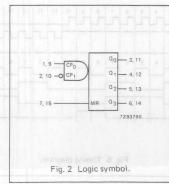
16-lead DIL; plastic (SOT38Z).

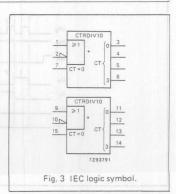
16-lead mini-pack; plastic (SO16; SOT109A).

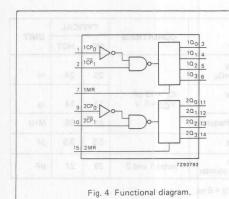
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1,9	1CP ₀ , 2CP ₀	clock inputs (LOW-to-HIGH, edge-triggered)
2, 10	1CP ₁ , 2CP ₁	clock inputs (HIGH-to-LOW, edge-triggered)
3, 4, 5, 6	1Q ₀ to 1Q ₃	data outputs
7, 15	1MR, 2MR	asynchronous master reset inputs (active HIGH)
8	GND	ground (0 V)
11, 12, 13, 14	2Q ₀ to 2Q ₃	data outputs
16	Vcc	positive supply voltage









FUNCTION TABLE

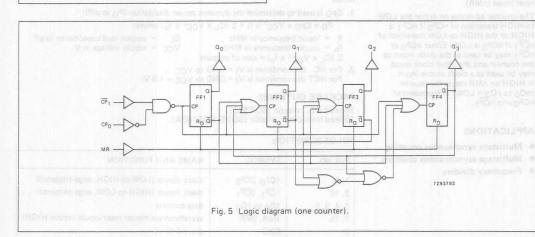
nCP ₀	nCP ₁	MR	MODE
1	Н	L	counter advances
L	1	L	counter advances
1	X	L	no change
X	†	L	no change
1	HE .	L	no change
Н	1	L	no change
X	X	H	Q_0 to $Q_3 = LOW$

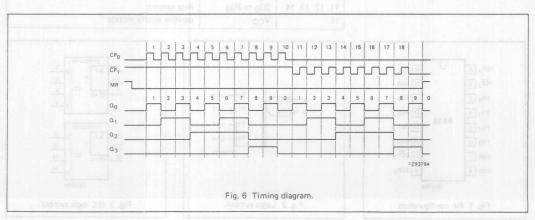
H = HIGH voltage level

X = don't care

↑ = LOW-to-HIGH clock transition

↓ = HIGH-to-LOW clock transition





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_1 = 50$ pF

					T _{amb}	(°C)				TEST CONDITIONS		
SYMBOL		74HC								DAGUT BLOIRS	TURUT TURKIT	
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			1.50	RIVID
tPHL/ tPLH	propagation delay nCP ₀ , nCP ₁ to nQ _n		66 24 19	210 42 36		265 53 45		315 63 59	ns	2.0 4.5 6.0	Fig. 9	
tPHL 2010	propagation delay nMR to nΩ _n		44 16 13	150 30 26	(9°) d	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8	to he do
tTHL/	output transition time	125	19 7 6	75 15 13	For 0	95 19 16	-25	110 22 19	ns	2.0 9 4.5 6.0	Fig. 9	TOSMAS
tw	clock pulse width HIGH or LOW	80 16 14	25 9 7	Ann J	100 20 17	ent 3	120 24 20	28	ns	2.0 4.5 6.0	Fig. 8 4000	(5.74) (3.44)
tw	master reset pulse width	120 24 20	39 14 11		150 30 26		180 36 31	Cr.	ns	2.0 4.5 6.0	Fig. 8	JHR
^t rem	removal time nMR to nCP ₀ , nCP ₁	0 0	-22 -8 -6	DE.	0 0 0		0 0 0	T 05	ns	2.0 4.5 6.0	Fig. 8	HUTT
t _{su}	set-up time nCP ₁ to nCP ₀ ; nCP ₀ to nCP ₁	80 16 14	22 8 6	30	100 20 17	25	120 24 20	20. 11	ns 115	2.0 4.5 6.0	Fig. 7	W.
f _{max}	maximum clock pulse frequency nCP ₀ , nCP ₁	6.0 30 35	18 55 66	G	4.8 24 28	0	4.0 20 24	- 0	MHz	2.0 4.5 6.0	Fig. 8	med

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

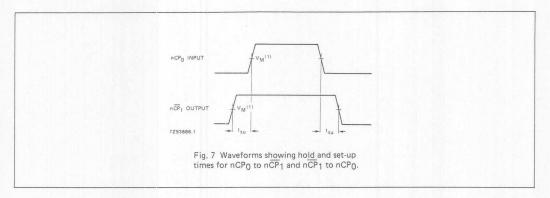
INPUT	UNIT LOAD COEFFICIENT
nCP ₀ , nCP ₁	0.80
nMR	1.50

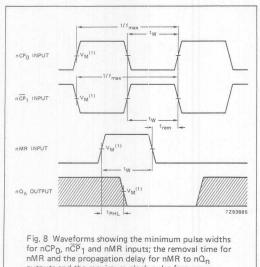
AC CHARACTERISTICS FOR 74HCT

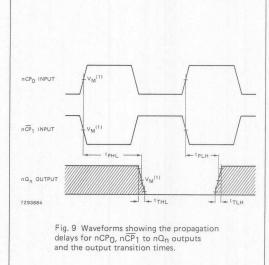
 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	ns 4.6 Rig.8	70.00			T_{amb}	(°C)				TEST CONDITIONS			
CVMPOL		74HCT											
SYMBOL	PARAMETER 2	+25		5	-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS		
	0.0	min.	typ.	max.	min.	max.	min.	max.					
tPHL/ tPLH	propagation delay nCP0, nCP1 to nQn		28	53		66		80	ns	4.5	Fig. 9	VV ^d	
[†] PHL	propagation delay nMR to nQ _n		17	35	0	44		53	ns	4.5	Fig. 8	990	
tTHL/ tTLH	output transition time		7	15		19	2	22	ns	4.5	Fig. 9		
tw	clock pulse width HIGH or LOW	20	11	ő	25	0	30	i= 0	ns	4.5	Fig. 8	031617	
tw	master reset pulse width HIGH	20	11	24	25	20	30	8 8	ns	4.5	Fig. 8	ns,	
^t rem	removal time nMR to nCP ₀ , nCP ₁	0	-11	20	0	4.8	0	81 0.8	ns	4.5	Fig. 8	xam	
t _{su}	set-up time nCP ₁ to nCP ₀ ; nCP ₀ to nCP ₁	16	5		20		24		ns	4.5	Fig. 7		
f _{max}	maximum clock pulse frequency nCP ₀ , nCP ₁	25	50		20		17		MHz	4.5	Fig. 8		

AC WAVEFORMS







Note to Fig. 8 and Fig. 9

Conditions:

 $n\overline{CP}_1$ =HIGH while nCP0 is triggered on a LOW-to-HIGH transition and nCP0 = LOW , while nCP1 is triggered on a HIGH-to-LOW transition.

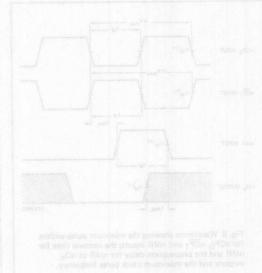
outputs and the maximum clock pulse frequency.

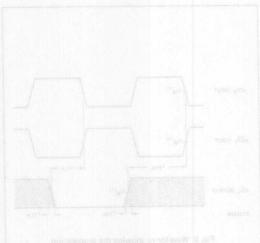
Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

AC WAVEPORMS







Note to Fig. 8 and Fig. 9

enoilibre

CP1 = MICH while rCP0 is traggered on a LOW-to-Hick rensition and nCP0 = LOW, while nCP1 is pregered on HICHTO-LOW transition.

> Note to AC waveforms (1) HC: VM = 50%: V/ = 6ND to Vc. HCT: VM = 1.3 V; V/ = 6ND to 3 V

DUAL 4-BIT SYNCHRONOUS BINARY COUNTER

FEATURES

Output capability: standard

• ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4520 are high-speed Si-gate CMOS devices and are pin compatible with the "4520" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4520 are dual 4-bit internally synchronous binary counters with an active HIGH clock input (nCPo) and an active LOW clock input (nCP1), buffered outputs from all four bit positions (nQ₀ to nQ₃) and an active GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns HIGH overriding asynchronous master reset input (nMR).

The counter advances on either the LOWto-HIGH transition of nCP₀ if nCP₁ is HIGH or the HIGH-to-LOW transition of nCP₁ if nCP₀ is LOW. Either nCP₀ or nCP₁ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on nMR resets the counter $(nQ_0 \text{ to } nQ_3 = LOW) \text{ independent of } nCP_0 \text{ and } n\overline{CP}_1.$

APPLICATIONS

- Multistage synchronous counting
- Multistage asynchronous counting
- Frequency dividers

SYMBOL P.	DADAMETED	CONDITIONS	TYF	LINUT	
SAMBOL	PARAMETER	CONDITIONS	НС	нст	ns ns MHz
^t PHL/ ^t PLH	propagation delay nCP0, nCP1 to nQn	I-CL	24	24	ns
^t PHL	propagation delay nMR to nQn	C _L = 15 pF V _{CC} = 5 V	13	13	ns
f _{max}	maximum clock frequency		68	64	MHz
Cı	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per counter	notes 1 and 2	29	24	pF

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x VCC^2 x f_i + Σ (CL x VCC^2 x f_o) where:

CL = output load capacitance in pF VCC = supply voltage in V f; = input frequency in MHz

fo = output frequency in MHz

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$ 2. For HC the condition is VI = GND to VCC

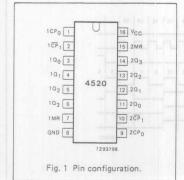
For HCT the condition is $V_1 = GND$ to $V_{CC} - 1.5 V$

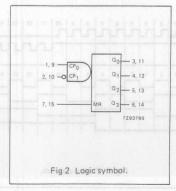
PACKAGE OUTLINES

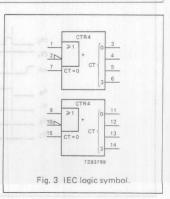
16-lead DIL; plastic (SOT38Z). 16-lead mini-pack; plastic (SO16; SOT109A).

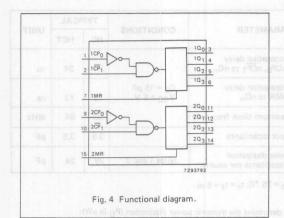
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1CP ₀ , 2CP ₀	clock inputs (LOW-to-HIGH, edge-triggered)
2, 10	1CP ₁ , 2CP ₁	clock inputs (HIGH-to-LOW, edge-triggered)
3, 4, 5, 6	1Q ₀ to 1Q ₃	data outputs
7, 15	1MR, 2MR	asynchronous master reset inputs (active HIGH)
8	GND	ground (0 V)
11, 12, 13, 14	2Q ₀ to 2Q ₃	data outputs
16	Vcc	positive supply voltage









FUNCTION TABLE

nCP ₀	nCP ₁	MR	MODE
1 4	Н	L	counter advances
L	1	L	counter advances
1	X	L	no change
X	1	L	no change
1	L	L	no change
H	1	L	no change
X	X	H	Q_0 to $Q_3 = LOW$

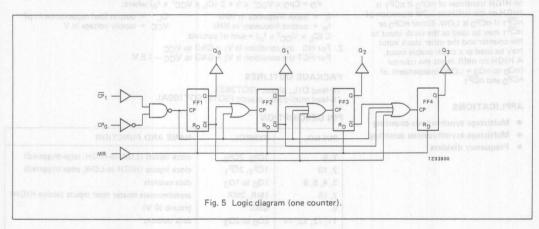
H = HIGH voltage levels on visited and

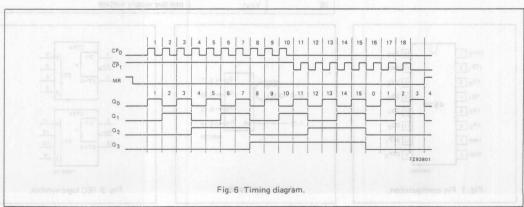
L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH clock transition

↓ = HIGH-to-LOW clock transition





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

		acts o	i nwo	degrapio	T _{amb}	(°C)	n ata A	rd-eulev i		TEST CONDITIONS		
SYMBOL					74H	С						
	PARAMETER	+25		-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.			0.80	n oson
tPHL/ tPLH	propagation delay nCP0 to nQ _n		77 28 22	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 8	PMG
tPHL/ tPLH	propagation delay nCP ₁ to nQ _n		77 28 22	240 48 41	(A) (1)	300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 8	
[†] PHL 2N	propagation delay nMR to nQ _Π		44 16 13	150 30 26	Тона	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9	JOSWY
tTHL/ tTLH	output transition time	.2000	19 7 6	75 15 13	ITH . IN	95 19 16	877 - CSA	110 22 19	ns	2.0 4.5 6.0	Fig. 8	
t _W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	HJ9
tW	master reset pulse width	120 24 20	39 14 11		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 7	HJS
^t rem	removal time nMR to nCP ₀ ; nCP ₁	0	-28 -10 -8		0 0 0		0 0		ns ga	2.0 4.5 6.0	Fig. 7	UHT HJT
^t su	set-up time nCP ₁ to nCP ₀ ; nCP ₀ to nCP ₁	80 16 14	14 5 4	8	100 20 17	5	120 24 20	20	ns	2.0 4.5 6.0	Fig. 8	VV
f _{max}	maximum clock pulse frequency	6.0 30 35	19 58 69		4.8 24 28		4.0 20 24	20	MHz	2.0 4.5 6.0	Fig. 7	W

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

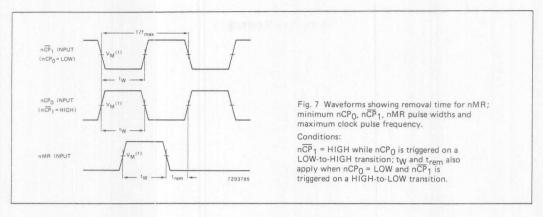
INPUT MAGE	COEFFICIENT
nCP ₀ , nCP ₁	0.80
nMR	1.50

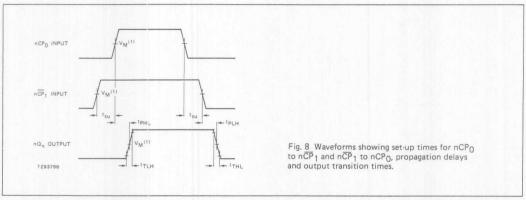
AC CHARACTERISTICS FOR 74HCT

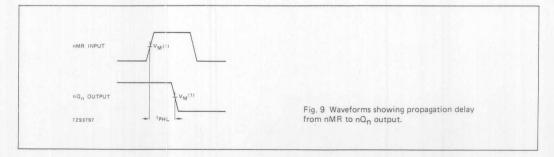
GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

	0.8	Fe			Tamb	(°C)		TEST CONDITIONS				
	2,0 ns 4.5 Eig.9	12			74H	СТ		yslab	noisepagarq No.or. Blan			
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		is neiti	metr ruqtuo	
tPHL/ tPLH	propagation delay nCP ₀ to nQ _n		28	53	0	66	2	80	ns	4.5	Fig. 8	W
tPHL/	propagation delay		25	53	0	66	8	80	ns	4.5	Fig. 8	
^t PHL	propagation delay nMR to nΩ _n		16	35		44	1	53	ns	4.5	Fig. 9	
tTHL/ tTLH	output transition time		7	15		19	8	22 0	ns	4.5	Fig. 8	men
tw	clock pulse width HIGH or LOW	20	10	- CO - S	25	20	30	80 1	ns	4.5	Fig. 7	DS.
tw	master reset pulse width HIGH	20	12	6 20	25	4.0	30	6.0 a	ns	4.5	Fig. 7	XBIO
trem	removal time nMR to nCP0; nCP1	0	-8	2	0	BS 1	0	8 80	ns	4.5	Fig. 7	
t _{su}	set-up time nCP1 to nCP0; nCP0 to nCP1	16	6		20		24		ns	4.5	Fig. 8	
fmax	maximum clock pulse frequency	30	58		24		20		MHz	4.5	Fig. 7	

AC WAVEFORMS



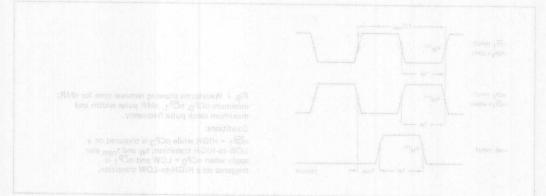


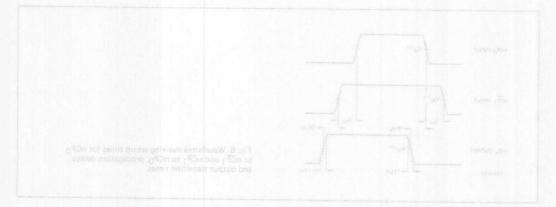


Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

AC WAVEFORMS







Note to AC waveforms (1) HC: $V_{M} = 50\%$, $V_{I} = 600$ to V_{CC} HCT: $V_{M} = 1.3 \text{ V}$, $V_{I} = 600$ to 3 V

DUAL RETRIGGERABLE PRECISION MONOSTABLE MULTIVIBRATOR

- Separate reset inputs
- Triggering from leading or trailing edge
- · Output capability: standard
- Icc category: MSI
- Power-on reset on-chip

GENERAL DESCRIPTION

The 74HC/HCT4538 are high-speed Si-gate CMOS devices and are pin compatible with "4538" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4538 are dual retriggerable-resettable monostable multivibrators. Each multivibrator has an active LOW trigger/retrigger input $(n\overline{A}_0)$, an active HIGH trigger/retrigger input (nA₁), an overriding active LOW direct reset input (nRD), an output (nQ) and its complement $(n\overline{Q})$, and two pins (nC_{TC}) and nRCTC) for connecting the external timing components C+ and R+. Typical pulse width variation over temperature range is ± 0.2%.

The "4538" may be triggered by either the positive or the negative edges of the input pulse. The duration and accuracy of the output pulse are determined by the external timing components Ct and Rt. The output pulse width (T) is equal to 0.7 x Rt x Ct. The linear design techniques guarantee precise control of the output pulse width.

A LOW level at nRD terminates the output pulse immediately.

Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times.

01/44001	FUNCTION TABLE	CONDITIONS	TYP	LINUT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
tPHL/	propagation delay $n\overline{A}_0$, nA_1 to nQ , $n\overline{Q}$	C _L = 15 pF V _{CC} = 5 V	27	30	ns
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per multivibrator	notes 1 and 2	136	138	pF

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_1 + \Sigma (C_L \times V_{CC}^2 \times f_0) + + 0.48 \times C_{EXT} \times V_{CC}^2 \times f_0 + D \times 0.8 \times V_{CC}$$
 where:

f; = input frequency in MHz = output load capacitance in pF = supply voltage in V fo = output frequency in MHz $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$ D

= duty factor in % CEXT = timing capacitance in pF

2. For HC the condition is V_1 = GND to V_{CC} For HCT the condition is V_1 = GND to V_{CC} – 1.5 V

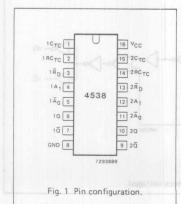
PACKAGE OUTLINES

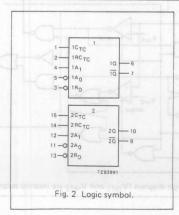
16-lead DIL; plastic (SOT38Z).

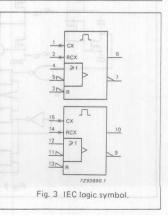
16-lead mini-pack; plastic (SO16; SOT109A).

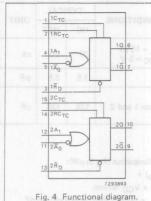
PIN DESCRIPTION

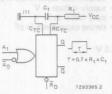
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	1CTC, 2CTC	external capacitor connections
2, 14	1RCTC,2RCTC	external resistor/capacitor connections
3, 13	$1\overline{R}_D, 2\overline{R}_D$	direct reset inputs (active LOW)
4, 12	1A ₁ , 2A ₁	trigger inputs (LOW-to-HIGH, edge-triggered)
5, 11	1Ā0, 2Ā0	trigger inputs (HIGH-to-LOW, edge-triggered
6, 10	10, 20	pulse outputs
7, 9	10, 20	complementary pulse outputs
8	GND	ground (0 V)
16	Vcc	positive supply voltage











(1) Connect C_{TC} (pins 1 and 15) to GND (pin 8).

Fig. 5 Connection of the external timing components \mathbf{R}_{t} and \mathbf{C}_{t} .

FUNCTION TABLE

	INPUTS	PARAS	OUTF	PUTS
nĀ0	nA ₁	$n\overline{R}_D$	nQ	nQ
Į Da 3	Drigo IA	Н	1	
Н	1	Н	1	T
X	X	From:	L	Н

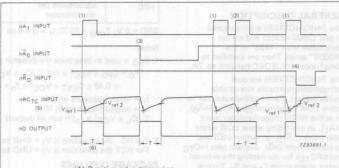
= HIGH voltage level

= LOW voltage level = don't care

= LOW-to-HIGH transition = HIGH-to-LOW transition

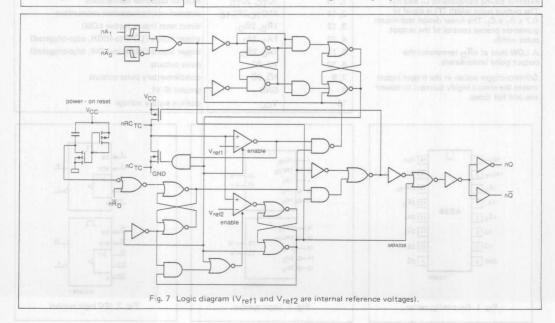
= one HIGH level output pulse
= one LOW level output pulse

= one LOW level output pulse



- (1) Positive edge triggering.
- (2) Positive edge retriggering (pulse lengthening).
- (3) Negative edge triggering.
- (4) Reset (pulse shortening).
- (5) V_{ref1} and V_{ref2} are internal reference voltages. (6) $T = 0.7 \times R_t \times C_t$ (see also Fig. 5).

Fig. 6 Timing diagram.



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". To or become an analysis and a second of the DC characteristics are chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

					Tamb (°C)					TEST CONDITIONS
CC OF GND;		10.0	1	0.	74H0	3.0			31	enup a	EN INDUCTIONS
SYMBOL	PARAMETER		+25		-40 1	o +85	-40 to	+125	UNIT	VCC	OTHER
		min.	typ.	max.	min.	max.	min.	max.	s beivied s	ed ylne	cote This measurement can:
^t PLH	propagation delay nÃ ₀ , nA ₁ to nQ		85 31 25	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig. 8 _{13TOARAHO} OK
^t PHL	propagation delay nĀ ₀ , nA ₁ to nQ̄		83 30 24	265 53 45	apida	330 66 56	SI Yausa	400 80 68	ns	2.0 4.5 6.0	Fig. 8 validação juntu
^t PHL	propagation delay	oi eds	80 29 23	265 53 45	baol s	330 66 56	f lool/	400 80 68	ns la ylaqu	2.0 4.5 6.0	Fig. 8 Says 10H of sto
^t PLH	propagation delay	2013	83 30 24	265 53 45	138003	340 68 58	MIN AP	400 80 68	ns	2.0 4.5 6.0	Fig. 8 INU TUPNI
tTHL/	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 8 aa.0 (An. QAr
t _W	nĀ ₀ pulse width LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
tw	nA ₁ pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
tw	nR _D pulse width	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t _W	nQ, nQ pulse width HIGH or LOW	0.63	0.70	0.77	0.602	0.798	0.595	0.805	ms	5.0	Fig. 8; $R_t = 10 \text{ k}\Omega$; $C_t = 0.1 \mu\text{F}$
^t rem	removal time \overline{R}_D to $n\overline{A}_0$, nA_1	35 7 6	6 2 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 8
t _{rt}	retrigger time nĀ ₀ , nA ₁	- - -	455+X 80+X 55+X		=		-		ns	2.0 4.5 6.0	Fig. 8 X = C _{EXT} /(4.5 × V _{CC})
REXT	external timing resistor	10 2		1000 1000					kΩ	2.0 5.0	
C _{EXT}	external timing capacitor				no lim	its			pF	5.0	

NON-STANDARD DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V) most political recommendation of the second sec

					T _{amb} (°C)				bai	TEST CONDITIONS			
SYMBOL	DADAMETED				74H0		UNIT		V/	OTHER				
	PARAMETER	+25			-40	to +85	-40 t	o +125	ONEN I	V _{CC}	VIV	OTHER		
		min.	typ.	max.	min.	max.	min.	max.	300	- 10		- 1. V V - CON		
SHOP	TOMOS TOST				7 1 de	51					2.0			
±II	input leakage current nRC _{EXT}			0.5	инс	5.0		10.0	μΑ	6.0	or GND	V _{CC} or GND; note 1		

Note

1. This measurement can only be carried out after a trigger pulse is applied.

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

						UNIT LOAD	INPUT
					2.0 4.5 6.0	0.50 0.65	nĀo, nA1 nRD
	19						
	X+68h X+68 X+88						

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

					T _{amb} (°	(C)					TEST CONDITIONS
OV44DO1	BARAMETER.				74HC	Т				109	
SYMBOL	PARAMETER		+25		-40 t	o +85	-40 to	+125	UNIT	VCC	OTHER
	and a	min.	typ.	max.	min.	max.	min.	max.		204	
^t PLH	propagation delay nĀ ₀ , nA ₁ to nQ		35	60	- 20	75		90	ns	4.5	Fig. 8
^t PHL	propagation delay nA ₀ , nA ₁ to nQ		35	60		75		90	ns	4.5	Fig. 8
^t PHL	propagation delay nRD to nQ		35	60	6.75	75	-	90	ns	4.5	Fig. 8
^t PLH	propagation delay nR _D to nΩ	1	35	60		75	I A	90	ns	4.5	Fig. 8
t _{THL} / t _{TLH}	output transition time		7	15		19		21	ns	4.5	Fig. 8
t _W	nĀ ₀ pulse width LOW	20	11		25		30		ns	4.5	Fig. 8
tw	nA ₁ pulse width HIGH	16	5	7	20	177	24		ns	4.5	Fig. 8
tw	nRD pulse width	20	11		25		30		ns	4.5	Fig. 8
tw	nQ, nQ pulse width HIGH or LOW	0.63	0.70	0.77	0.602	0.798	0.595	0.805	ms	5.0	Fig. 8; R _t = 10 kΩ; C _t = 0.1 μ F
^t rem	removal time RD to nA0, nA1	7	2	rigger ti	9	si eni i	11	n , An	ns	4.5	Fig. 8
t _{rt}	retrigger time	-	80+X		-		-		ns	4.5	Fig. 8 X = C _{EXT} /(4.5 x V _{CC})
REXT	external timing resistor	2		1000					kΩ	5.0	ore to AC waveforms HC: V _M = 50%; V ₁ =
CEXT	external timing capacitor				no limi	ts			pF	5.0	HOL: AM - ITS ALAL

NON-STANDARD DC CHARACTERISTICS FOR 74HCT

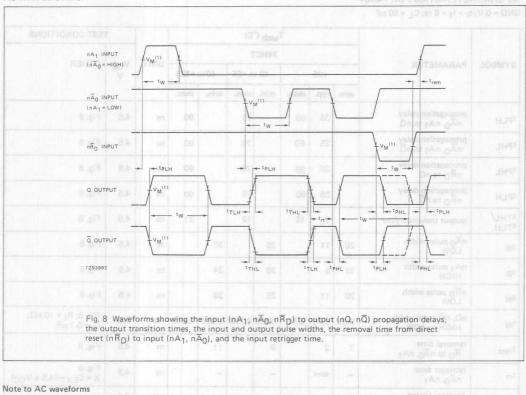
Voltages are referenced to GND (ground = 0 V)

					T _{amb} (°C)					TEST CO	ONDITIONS
SYMBOL	PARAMETER				74HC	Т			UNIT	V	V.	OTHER
STIMBUL	PARAMETER			-40	to +85	-40 to +125		ONTI	V _{CC}	V _I	OTHER	
		min.	typ.	max.	min.	max.	min.	max.				
±II	input leakage current nRCEXT			0.5		5.0		10.0	μА	5.5	2.0 or GND	V _{CC} or GND; note 1

Note

1. This measurement can only be carried out after a trigger pulse is applied.





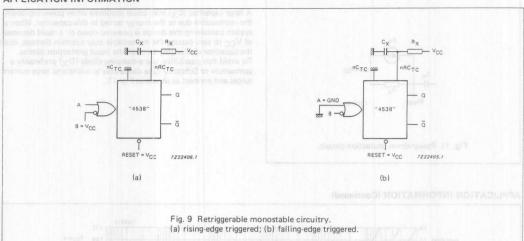
Note to AC waveforms
(1) HC: $V_M = 50\%$; $V_I = GND$ to V_{CC} .

HCT: $V_M = 1.3$ V; $V_I = GND$ to 3 V.

NON-STANDARD DC CHARACTERISTICS FOR TAHCT

			+125								

APPLICATION INFORMATION



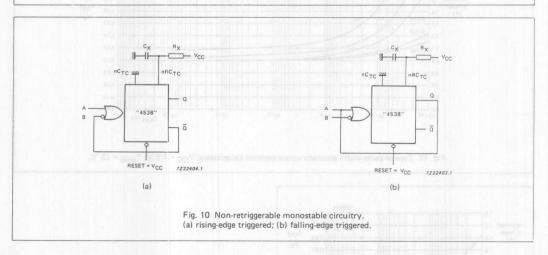
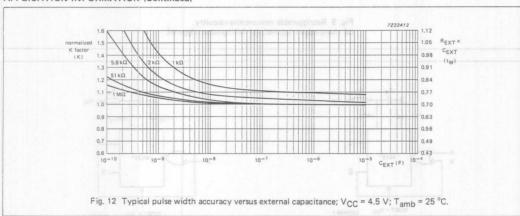


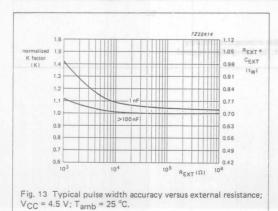
Fig. 11 Power-down protection circuit.

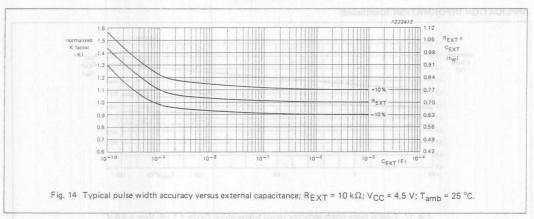
Power-down considerations WOTTAMED THE WOTTAMENTA

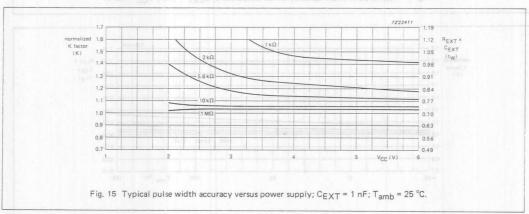
A large capacitor (C_X) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may substain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_X) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Fig. 11.

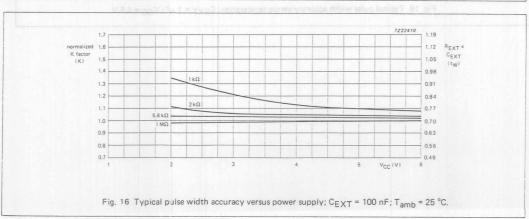
APPLICATION INFORMATION (Continued)













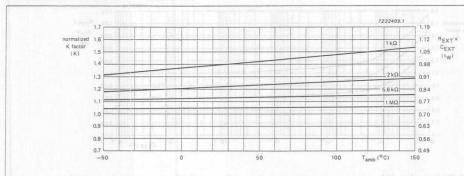


Fig. 17 Typical pulse width accuracy versus temperature; C_{EXT} = 1 nF; V_{CC} = 4.5 V.

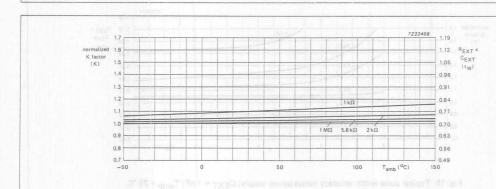


Fig. 18 Typical pulse width accuracy versus temperature; C_{EXT} = 1 μF ; V_{CC} = 4.5 V_{cc}

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER FOR LCDs

FEATURES

- Latch storage of BCD inputs
- Blanking inputs
- Output capability: non-standard
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4543 are high-speed Si-gate CMOS devices and are pin compatible with "4543" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4543 are BCD to 7-segment latch/decoder/drivers for liquid crystal displays. They have four address inputs (D₀ to D₃), an active HIGH latch disable input (LD), an active PD = CPD \times VCC² \times f₁ + Σ (CL \times VCC² \times f₀) where: HIGH blanking input (BI), an active HIGH phase input (PH) and seven buffered segment outputs (Q_a to Q_q).

The "4543" provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder driver. The "4543" can invert the logic levels of the output combination. The phase (PH), blanking (BI) and latch disable (LD) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the "4543" are directly connected to the segments of the liquid crystal.

		CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	ONT	
t _{PHL} /	propagation delay D_n to Ω_n LD to Ω_n BI to Ω_n	C _L = 15 pF V _{CC} = 5 V	29 32 20	33 31 28	ns ns ns	
Cl	input capacitance	عراره إعراقي	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	42	42	pF	

$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

- 1. CPD is used to determine the dynamic power dissipation (PD in μ W):

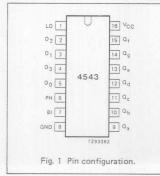
 - $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

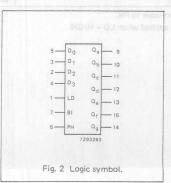
PACKAGE OUTLINES

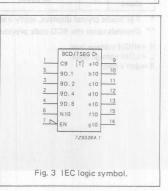
- 16-lead DIL; plastic (SOT38Z).
- 16-lead mini-pack; plastic (SO16; SOT109A).

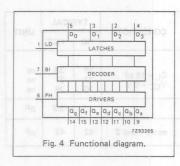
PIN DESCRIPTION

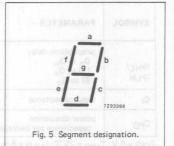
PIN NO.	SYMBOL	NAME AND FUNCTION	
1 5 3	LD	latch disable input (active HIGH)	H
5, 3, 2, 4	D ₀ to D ₃	address (data) inputs	
6	PH	phase input (active HIGH)	
7	BI	blanking input (active HIGH)	
8	GND	ground (0 V)	
9, 10, 11, 12 13, 15, 14	Q _a to Q _g	segment outputs	
16	Vcc	positive supply voltage	











APPLICATIONS

- Driving LCD displays
- Driving fluorescent displays
- Driving incandescent displays
- Driving gas discharge displays

FUNCTION TABLE

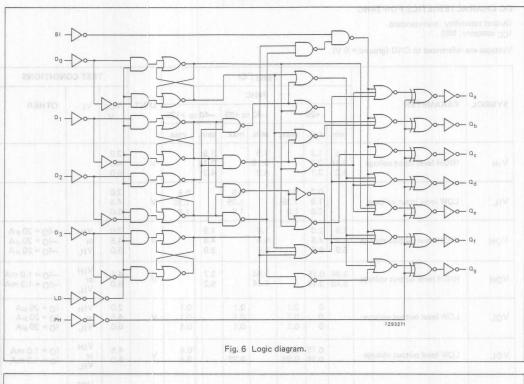
			UDILIT	0		3000	DISP								address inputs (Do to Dg), an active
		11	NPUT:	5 :818	KDA PO	1 × 50	DA K	That is	U	UTPU	15	94-1	DA .	DISPL	HGH blanking input (BI), an active
LD	ВІ	PH*	D ₃	D ₂	D ₁	D ₀	Qa	Qb	Q_c	Q_{d}	Qe	Qf	Q_g		HIGH phase input (PH) and seven
X	Н	L	X	X	X	X	E d	L	L	Lo	X LOC	VLX.	LOT	blank	The "4543" provides the function or a
HHHH		L L L	L L L	L L L	LHH	H	HLHH	H H H	HHLH	H L H	H L H	H L L L	L H H	0 1 2 3	Folit storage latch and an 8-4-2/1 BCD had 7-agment decoder driver. The "45-41" can invent the logic levels of the output combination. The phase (PH), blanking. (B1) and latch disable (LD) inputs an
HHHH		L L L		HHHH	L H H	H L H	L H H	H L L	HHHH	L H H L	L L H L	HHHL	HHHL	4 5 6 7	uad to reverse the function table phase, black the display and store a SCD code, espectively. For liquid crystal displays a square-wave a applied to RH and the alegarical
HHHH	L L L	L L L	H H H	E LONG	H H	L L H	H	H H L	H H L	H	H L L	H H L	H H L	8 9 blank blank	common back-plane of the display. The oursuit of the "AFAS" are directly consecred to the segments of the liquid cystal.
ннн			H H H H	H H H H	L	L H L		L L L		L H	L L L	LLLL	S . C . L . L . L . L	blank blank blank blank	
L	L	L H	X	X as at	X	X			. g6	** se of a		MI.	8, 16,	as	

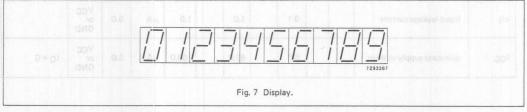
- For liquid crystal displays, apply a square-wave to PH.
- ** Depends upon the BCD-code previously applied when LD = HIGH.

H = HIGH voltage level

L = LOW voltage level

X = don't care





RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134). For RATINGS see chapter "HCMOS family characteristics", section "Family specifications", standard outputs.

DC CHARACTERISTICS FOR 74HC

Output capability: non-standard I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

		-			Tamb (,C)				Т	EST CO	NDITIONS
		-			74H	С		Loc	TIMUT	Vcc		OTHER
SYMBOL	PARAMETER	+25		H	-40 to +85		-40 to +125		UNIT	VCC	VI	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
VIH	HIGH level input voltage	1.5 3.15 4.2	1.2 2.4 3.1		1.5 3.15 4.2	«О	1.5 3.15 4.2		v	2.0 4.5 6.0		-14
VIL	LOW level input voltage		0.7 1.8 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
Vон	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	-«	v	2.0 4.5 6.0	VIH or VIL	-10 = 20 μA -10 = 20 μA -10 = 20 μA
Vон	HIGH level output voltage	3.98 5.48	0.15 0.16		3.84 5.34		3.7 5.2	-<	V	4.5 6.0	VIH or VIL	-IO = 1.0 m. -IO = 1.3 m.
VoL	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	VIH or VIL	IO = 20 μA IO = 20 μA IO = 20 μA
VOL	LOW level output voltage		0.15 0.16	0.26	Logic	0.33		0.4	V	4.5 6.0	VIH or VIL	IO = 1.0 mA IO = 1.3 mA
±II	input leakage current		100 E	0.1		1.0		1.0	μΑ	6.0	VCC or GND	
Icc	quiescent supply current			8.0		80.0		160.0	μА	6.0	VCC or GND	I _O = 0

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

					T _{amb} (°C)		(V D	bring	TEST CONDITIONS			
SYMBOL	PARAMETER				74H	C.			UNIT	.,			
STIVIBUL	PARAMETER		+25			-40 to +85		-40 to +125		VCC	WAVEFORMS	TIVIS	
	O V DOV TIVI	min.	typ.	max.	min.	max.	min.	max.		813			
tPHL/	propagation delay D _n to Q _n	xsm	91 33 26	340 68 58	.nim	425 85 72	.qyr	510 102 87	ns	2.0 4.5 6.0	Fig. 12		
tPHL/	propagation delay LD to Ω _n		102 37 30	370 74 63	0.9	465 93 79	8.1	555 111 94	ns	2.0 4.5 6.0	Fig. 13	-H)V	
^t PHL/ ^t PLH	propagation delay BI to Ω _n	/ 8.0	66 24 19	265 53 45		330 66 56	1.2.1	400 80 68	ns	2.0 4.5 6.0	Fig. 14	11/	
t _{PHL} /	propagation delay PH to Q _n		55 20 16	200 40 34	4.6	250 50 43	6.0	300 60 51	ns	2.0 4.5 6.0	lavel HOTH	HOV	
t _{THL} /	output transition time		63 23 18	250 50 43	A8.i	315 63 54	1,32	375 75 64	ns	2.0 4.5 6.0	Figs 12, 13 and 1	4	
An OS =	LD pulse width HIGH or LOW	35 7 6	11 4 3	4.4	45 9 8		55 11 9		ns epical or	2.0 4.5 6.0	Fig. 13		
Am 0.1 =	set-up time D _n to LD	60 12 10	8 3 2	.33	75 15 13	85.	90 18 15		ns estilo	2.0 4.5 6.0	Fig. 15	Jo.	
^t h	hold time D _n to LD	30 6 5	3 1 1	0.	40 8 7	b	45 9 8		ns	2.0 4.5 6.0	Fig. 15	pl:	

DC CHARACTERISTICS FOR 74HCT

Output capability: non-standard

ICC category: MSI

Voltages are referenced to GND (ground = 0 V)

	BNIT Ved WAVEFOR			7	r _{amb} (°C)				TEST CONDITIONS			
	V	+128	or 0b	- 25+	74HC	Т	-25		UNIT	\(\)	\/.	OTHER	
SYMBOL	PARAMETER	. KISIYI	+25	25 –4		to +85	-40 to +125		UNIT	VCC	VI	OTHER	
	2.0 Pig 12	min.	typ.	max.	min.	max.	min.	max.			ourgago		
VIH	HIGH level input voltage	2.0	1.6	1 2 - 1	2.0	370	2.0		V	4.5 to 5.5	oliepedo	10 /19443	
VIL	LOW level input voltage	100	1.2	0.8		0.8	36 36	0.8	V	4.5 to 5.5	olispage	10 /TM41	
Vон	HIGH level output voltage	4.4	4.5	1 08	4.4	200	4.4		٧	4.5	VIH or VIL	$-10 = 20 \mu A$	
VOH Al bos	HIGH level output voltage	3.98	4.32	16	3.84	280	3.7		V	4.5	VIH or VIL	-IO = 1.0 mA	
VoL	LOW level output voltage	96	0	0.1	31	0.1		0.1	V	4.5	VIH or VIL	10 = 20 μΑ	
VOL	LOW level output voltage		0.15	0.26	0.00	0.33		0.4	V	4.5	VIH or VIL	I _O = 1.0 mA	
±II	input leakage current		8	0.1	01	1.0		1.0	μА	5.5	V _{CC} or GND	ori go	
Icc	quiescent supply current			8.0		80.0		160.0	μА	5.5	VCC or GND	10 = 0	
ΔI _{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μΑ	4.5 to 5.5	V _{CC} -2.1 V	other inputs at V _{CC} or GND; I _O = 0	

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given here. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D ₀ , D ₁ , D ₂	1.00
D ₃	0.50
BI	0.50
LD	1.50
PH	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

					T _{amb} (°C)				TEST CONDITIONS		
					74HC	eno.	.,	75-24				
SYMBOL	PARAMETER	+25			-40 to +85 -40 t			+125	UNIT	V _{CC}	WAVEFORMS	
	CD-CO-	min.	typ.	max.	min.	max.	min.	max.	note I			
t _{PHL} /	propagation delay D _n to Q _n		38	80		100		120	ns	4.5	Fig. 12	
tPHL/	propagation delay	9 Cos four	36	68		85	(00)	102	ns	4.5	Fig. 13	
tPHL/	propagation delay BI to Q _n		32	66		83		99	ns	4.5	Fig. 14	
t _{PHL} /	propagation delay PH to Q _n		24	66		83		99	ns	4.5		
tTHL/	output transition time	Cres	23	50		63		75	ns	4.5	Figs 12, 13 and 14	
tw	LD pulse width HIGH or LOW	10	4		13		15	gteett	ns	4.5	Fig. 13	
t _{su}	set-up time D _n to LD	12	4		15		18	mortgal	ns	4.5	Fig. 15	
^t h	hold time D _n to LD	8	2		10		12		ns	4.5	Fig. 15	

APPLICATION DIAGRAMS

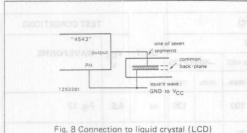
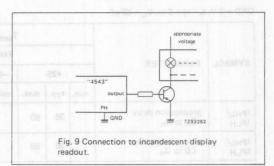
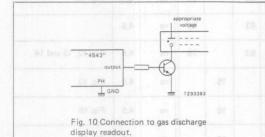
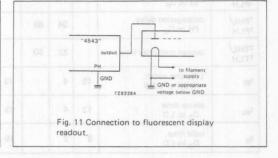


Fig. 8 Connection to liquid crystal (LCD) display readout.







AC WAVEFORMS

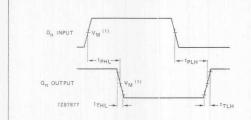


Fig. 12 Waveforms showing the address input (D_n) to output (Q_n) propagation delays and the output transition times.

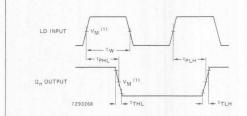


Fig. 13 Waveforms showing the latch disable input (LD) to output ($\Omega_{\rm D}$) propagation delays and the output transition times.

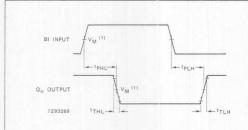


Fig. 14 Waveforms showing the blanking (B1) to output (Ω_n) propagation delays and the output transition times.

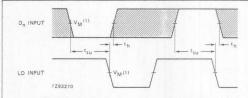


Fig. 15 Waveforms showing the address ($D_{\rm n}$) to latch disable (LD) input set-up and hold times.

Note to Fig. 15

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_1 = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_1 = GND$ to 3 V.

AC WAVEFORMS

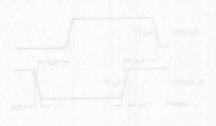


Fig. 12 Waveforms showing the address input (D_n) to output (D_n) propagation delays and the output transition times.



rig. 13 Waveforms showing the latch disable input (LD) to output (Q_n) propagation delays and the output transition times.

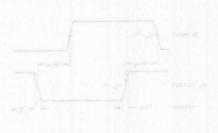


Fig. 14. Waveforms showing the blanking (B1) to output (Q_{ij}) propagation delays and the output transition times.

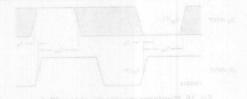


Fig. 15 Waveforms showing the address (D to latch disable (LD) input set-up and hold times.

More to Flg. 15

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC = VM = 50%; V₁ = 6ND to V_{CC}.

74HC/HCT5555

FEATURES

- Positive and negative edge triggered
- Retriggerable or non-retriggerable
- Programmable delay minimum: 100 ns maximum: depends on input frequency and division ratio
- Divide-by range of 2 to 2²⁴
- Direct reset terminates output pulse
- Very low power consumption in triggered start mode
- · 3 oscillator operating modes:
 - RC oscillator
 - Crystal oscillator
 - External oscillator
- Device is unaffected by variations in temperature and V_{CC} when using an external oscillator
- · Automatic power-ON reset
- Schmitt trigger action on both trigger inputs
- · Direct drive for a power transistor
- Low power consumption in active mode with respect to TTL type timers
- High precision due to digital timing
- · Output capability: 20 mA
- I_{cc} category: MSI.

APPLICATIONS

- Motor control
- · Attic fan timers
- · Delay circuits
- · Automotive applications
- Precision timing
- · Domestic appliances.

GENERAL DESCRIPTION

The 74HC/HCT5555 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT5555 are precision programmable delay timers which consist of:

- · 24-stage binary counter
- integrated oscillator (using external timing components)

- retriggerable/non-retriggerable monostable
- · automatic power-ON reset
- · output control logic
- · oscillator control logic
- overriding assynchronous master reset (MR).

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns.

SYMBOL	PARAMETER	CONDITIONS	01.	UNIT	
t _{PHL} /t _{PLH}	propagation delay A, \overline{B} to Q/\overline{Q} MR to Q/\overline{Q} RS to Q/\overline{Q}	C _L = 15 pF V _{CC} = 5 V	24 19 26	19 20	
Cı	input capacitance		3.5	3.5	pF
СРО	power dissipation capacitance per buffer	notes 1 and 2	23	36	pF

Notes

 C_{PD} is used to determine the dynamic power dissipation (P_{D} in μW):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz

f_o = output frequency in MHz

 $\Sigma(C_1 \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

For HC the condition is $V_1 = GND$ to V_{CC}

For HCT the condition is $V_1 = GND$ to $V_{CC} - 1.5 V$.

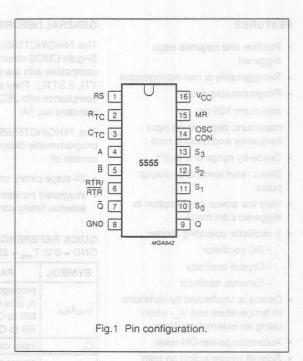
ORDERING INFORMATION

EXTENDED TYPE		PAC	CKAGE	
NUMBER	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT5555N	16	DIL	plastic	SOT38Z
74HC/HCT5555D	16	SO16	plastic	SOT109A

74HC/HCT5555

PINNING

SYMBOL	PIN	DESCRIPTION
RS	NCTIEN	clock input/oscillator pin
R _{TC}	2	external resistor connection
C _{TC}	3	external capacitor connection
A	4	trigger input (positive-edge triggered)
B	5	trigger input (negative-edge triggered)
RTR/RTR	6	retriggerable/non-retriggerable input (active HIGH/active LOW)
Q	7	pulse output (active LOW)
GND	8	ground (0 V)
Q	9	pulse output (active HIGH)
S ₀ - S ₃	10, 11, 12, 13	programmable input
OSC CON	14	oscillator control
MR an	15 24	master reset input (active HIGH)
V _{cc}	16	positive supply voltage



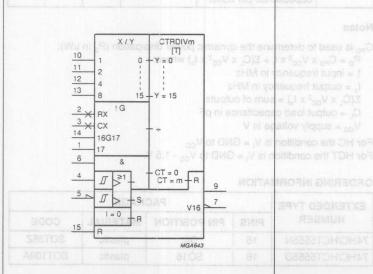
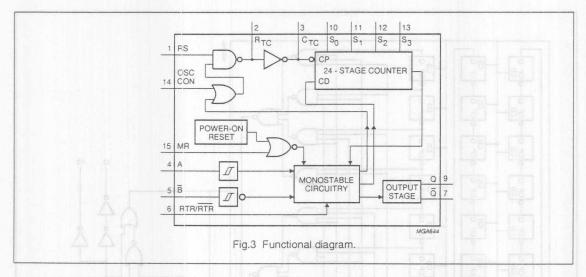


Fig.2 IEC logic diagram.

74HC/HCT5555



FUNCTIONAL DESCRIPTION

The oscillator configuration allows the design of RC or crystal oscillator circuits. The device can operate from an external clock signal applied to the RS input (R $_{TC}$ and C $_{TC}$ must not be connected). The oscillator frequency is determined by the external timing components (R $_{T}$ and C $_{T}$), within the frequency range 1 Hz to 4 MHz (32 kHz to 20 MHz with crystal oscillator).

In the HCT version the MR input is TTL compatible but the RS input has CMOS input switching levels. The RS input can be driven by TTL input levels if RS is tied to V_{CC} via a pull-up resistor.

The counter divides the frequency to obtain a long pulse duration. The 24-stage is digitally programmed via the select inputs (S_0 to S_3). Pin S_3 can also be used to select the test mode, which is a convenient way of functionally testing the counter.

The "5555" is triggered on either the positive-edge, negative-edge or both.

 Trigger pulse applied to input A for positive-edge triggering

- Trigger pulse applied input B for negative-edge triggering
- Trigger pulse applied to inputs A and B (tied together) for both positive-edge and negative triggering.

The Schmitt trigger action in the trigger inputs, transforms slowly changing input signals into sharply defined jitter-free output signals and provides the circuit with excellent noise immunity.

The OSC CON input is used to select the oscillator mode, either continuously running (OSC CON = HIGH) or triggered start mode (OSC CON = LOW). The continuously running mode is selected where a start-up delay is an undesirable feature and the triggered start mode is selected where very low power consumption is the primary concern.

The start of the programmed time delay occurs when output Q goes HIGH (in the triggered start mode, the previously disabled oscillator will start-up). After the programmed time delay, the flip-flop stages are reset

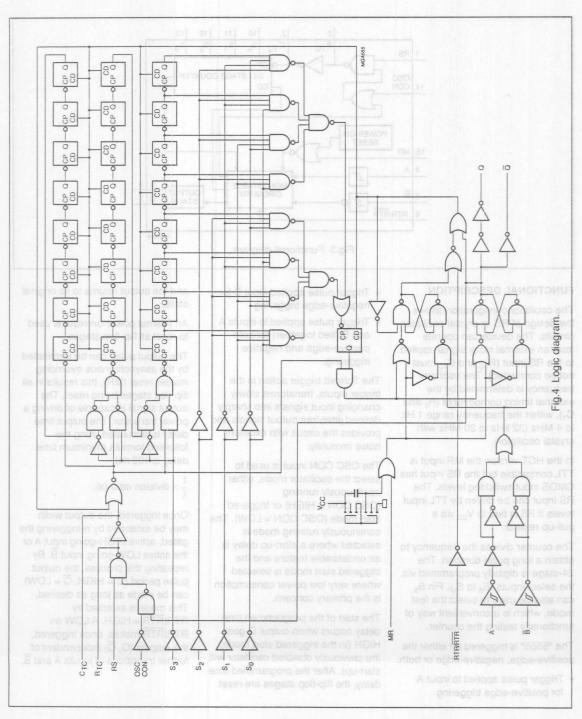
and the output returns to its original state.

An internal power-on reset is used to reset all flip-flop stages.

The output pulse can be terminated by the assynchronous overriding master reset (MR), this results in all flip-flop stages being reset. The output signal is capable of driving a power transistor. The output time delay is calculated using the following formula (minimum time delay is 100 ns):

 $\frac{1}{f_i}$ × division ratio (s).

Once triggered, the output width may be extended by retriggering the gated, active HIGH-going input A or the active LOW-going input \overline{B} . By repeating this process, the output pulse period ($Q = HIGH, \overline{Q} = LOW$) can be made as long as desired. This mode is selected by RTR/ $\overline{RTR} = HIGH$. A LOW on RTR/ \overline{RTR} makes, once triggered, the outputs (Q, \overline{Q}) independent of further transitions of inputs A and \overline{B} .



ntiw remit vale 74HC/HCT5555

TEST MODE

Set S_3 to a logic LOW level, this will divide the 24 stage counter into three, parallel clocking, 8-stage counters. Set S_0 , S_1 and S_2 to a logic HIGH level, this programs the counter to divide-by 2^8 (256). Apply a trigger pulse and clock in 255 pulses, this sets all flip-flop stages to a logic HIGH level. Set S_3 to a logic HIGH level, this causes the counter to divide-by 2^{24} . Clock one more pulse into the RS input, this causes a logic 0 to ripple through the counter and output Q/\overline{Q} goes from HIGH-to-LOW level. This method of testing the delay counter is faster than clocking in 2^{24} (16 777 216) clock pulses.

FUNCTION TABLE

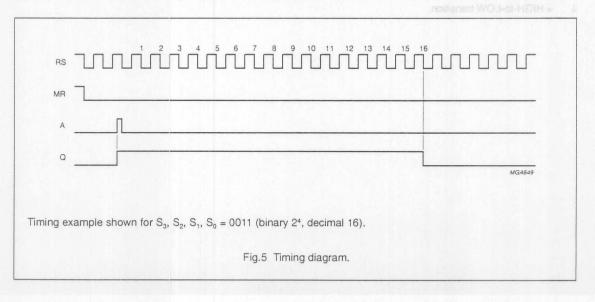
	INPUTS		OUT	PUTS		
MR	A 100	B	Q	Q		
Н	220 X	X		Н		
L	1	X	one HIGH level output pulse	one LOW level output pulse		
L	X 262 144	818	one HIGH level output pulse	one LOW level		

Notes

- H = HIGH voltage level
 - = LOW voltage level
- X = don't care
- = LOW-to-HIGH transition

DELAY TIME SELECTION

	SELECT	INPUTS		OUTPUT Q/Q (FRE	QUENCY DIVIDING)
S ₃	S ₂	S ₁	S _o	BINARY	DECIMAL
d output	in the gounter an	Description of the contract of	es allogic	ulse into the RS input, thits tue	de-by 214, Clock one mor 2
alz Fry al) -2 til 8 (iniooio	TUELTE IAS OF THAT	nestH con	22 133110 0011301 8111 .1074	4 Out-childlift most about 4
L	L	Н	L	23	8
L	L	Н	Н	24	16 BLEAT MOITON
L	»Higgin	L	L	25 0711014	32
L	Н	L	Н	26	64
L	Н	Н	L	27	128
L	Н	Н	Н	28	256
epi in	tratio .	auto tuatro			
H	A Lamo L	gyel Halist and	L	217	131 072
Hisland	Judiuo L	esting factor	Н	218	262 144
Н	L	Н	L	219	524 288
Н	L	Н	Н	220	1 048 576
Н	Н	L	L	2 ²¹	2 097 152
Н	Н	L	Н	222	4 194 304
Н	Н	Н	L	223	8 388 608
Н	Н	Н	Н	224	16 777 216



diw jemit vale 74HC/HCT5555

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: parallel outputs, bus driver; serial output, standard I_{CC} category: MSI.

DC CHARACTERISTICS FOR 74HC

	OSC CON Is	d.a			T _{amb} (°	C) _ N			-		TI	EST	CONDITION
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	0 +125	UNIT		V _{cc}		OTUED
	OSC CON 16-3	MIN	TYP	MAX	MIN	MAX	MIN	MAX	-		(V)	Vı	OTHER
V _{OH}	HIGH level output voltage Q and Q outputs	1.9 4.4 5.9	2 4.5 6.0	-	1.9 4.4 5.9	-	1.9 4.4 5.9	= 0	V V	1.9	2.0 4.5 6.0	out out epsi	Ι _ο = -20 μΑ
V _{OH}	HIGH level output voltage Q and Q outputs	3.98 5.48	4.32 5.81		3.84 5.34	-	3.7 5.2	-	V	5.9	4.5 6.0		$I_o = -6.0 \text{ mA}$ $I_o = -7.8 \text{ mA}$
V _{OH}	HIGH level output voltage Q and Q outputs	3.3 4.8	V V	==	3 4.5	= 1	2.7 4.2	- 8 - 0	V	4.4 5.9	4.5 6.0		$I_o = -20 \text{ mA}$ $I_o = -20 \text{ mA}$
VoL	LOW level output voltage Q and Q outputs	<u>ā</u> ,5	0 0	0.1 0.1 0.1	3.7 5.2 2.2	0.1 0.1 0.1	3.	0.1 0.1 0.1	V V	3.98	2.0 4.5 6.0	out age	Ι _ο = 20 μΑ
Vol	LOW level output voltage Q and Q outputs	4.5	0.15 0.15	0.26 0.26	- 8 - 8	0.33 0.33	1-1-9	0.40 0.40	V		4.5	rsi W	l _o = 6.0 mA l _o = 7.8 mA
V _{OL} OS	LOW level output voltage Q and Q outputs	(2,0 (4,5)	∆/ ∆/	0.9	-	1.14	-	1.34	V		4.5 6.0	age	I _o = 20 mA I _o = 25 mA
V _{IH}	HIGH level input voltage RS input	1.7 3.6 4.8		0.4	1.7 3.6 4.8	= 5.0	1.7 3.6 4.8	9.70	V V		2 4.5 6.0	rei W	OJ Juo Vot
V _{IL}	LOW level input voltage RS input	-	- - -	0.3 0.9 1.2	- - -	0.3 0.9 1.2	-	0.3 0.9 1.2	V V		2.0 4.5 6.0	huc	luo

74HC/HCT5555

					Tamb (°	C)					TEST CON	DITION
SYMBOL	PARAMETER	390	+25	TLANDOE.	-40 1	to +85	-40 1	to +125	UNIT	V _{cc}	DE EDITETIONS	BINIOU BAIT
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	VAID SI	(V)	ye par _i Vel out	OTHER
ИОПТО	иоо тезт	3.98 5.48	-	_	3.84 5.34	_ _(O°)	3.7 5.2	_	V	4.5 6.0	RS = GND; OSC CON = V _{CC}	$l_0 = -2.6 \text{ mA}$ $l_0 = -3.3 \text{ mA}$
нанто	HIGH level	3.98 5.48	- X/	FF 03 0	3.84 5.34	H OY U	3.7 5.2	81 P NEA	V	4.5 6.0	RS = V _{CC} ; OSC CON = GND; untriggered	$l_o = -0.65$ mA $l_o = -0.85$ mA
V _{OH} S-	voltage R _{TC} output	1.9 4.4 5.9	2.0 4.5 6	= (1.9 4.4 5.9		1.9 4.4 5.9	 S	V V V	2.0 4.5 6.0	RS = V _{CC} ; OSC CON = V _{CC}	l _o = -20 μA
	6.0 6= 4.5 ₆ = 6.0 ₆ =	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9	- 4 	1.9 4.4 5.9	- 1	V V V	2 4.5 6.0	RS = V _{CC} ; OSC CON = GND; untriggered	$I_0 = -20 \mu\text{A}$
V _{OH} 02	HIGH level output voltage C _{TC} output	3.98 5.48	V V V	.0	3.84 5.34	1.0 1.0 1.0	3.7 5.2	0.1 0.1 0.1	V	4.5 6.0	RS = V _{IH} ; OSC CON = V _{IH}	$l_o = -3.2 \text{ mA}$ $l_o = -4.2 \text{ mA}$
Am 0.8 Am 8.7	LOW level	-	V 0 V 0	0.26 0.26	= 8	0.33 0.33	-	0.4	V	4.5 6	RS = V _{CC} ; OSC CON = V _{CC}	$I_0 = 2.6 \text{ mA}$ $I_0 = 3.3 \text{ mA}$
V _{OL}	voltage R _{TC} output	-	0 4	0.1 0.1 0.1	- b	0.1 0.1 0.1	-	0.1 0.1 0.1	V V	2.0 4.5 6	RS = V _{CC} ; OSC CON = V _{CC}	Ι _ο = 20 μΑ
V _{OL}	LOW level output voltage C _{TC} output	_	V V V	0.26 0.26	1.1 2.8 4.4	0.33 0.33	3.6	0.4	V	4.5 6.0	RS = V _{IL} ; OSC CON = V _{IL} ; untriggered	l _o = 3.2 mA l _o = 4.2 mA

74HC/HCT5555

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_t = 6 ns; C_1 = 50 pf.$

FORMS	BVAW 30V	THAL		01 04-	T _{amb} (°C	;)				TEST	CONDITION
SYMBOL	PARAMETER		+25	MIM	-40 1	0 +85	-40 to	+125	UNIT	V _{cc}	WAVEFORMS
	2.0 4.5 Fig.8:	MIN	TYP	MAX	MIN	MAX	MIN	MAX	2	(V)	WAVEFORMS
	propagation	-sHM	77	240 8		300		360	nss	2.0	puperi
tpLH/tpHL	delay A, B to	SHM	28	48	-	60	-	72	ns	4.5	Fig.6
b eine	Q, Q	THIS	22	41 00	-	51	-	61	ns	6.0	i Shala
	propagation	-ci-th/	61	185	-	230		280	ns	2.0	Treque
t _{PLH} /t _{PHL}	delay MR to Q,	-	22	37		46	-	56	ns	4.5	Fig.7
TLN THE	Q	-	18	31	-	39	-	48	ns	6.0	9
	propagation	-	83	250	-	315	_	375	ns	2.0	DOA on of ce
t _{PLH} /t _{PHL}	delay RS to Q,	_	30	50	_	63	_	75	ns	4.5	Fig.8; note 1
'PLH' 'PHL	Q	v5 act v	24	43	Tovous	54	_	64	ns	6.0	119.0, 110.0
Delted (iended, it me timi	19 90 V	19	75	1evew	95	rigger I	110	ns	2.0	voted the cin
b /b	output	1	1			19	1 - 1	22	ns	4.5	Fig.6
t _{THL} /t _{TLH}	transition time	dan resp	7 6	15	emains	16	ualuo e	19	EDOT HE TITLE	AL DERIVE SIDES	rig.o
		-	Ь	13	-	16	-	19	ns	6.0	re RS clock into
	trigger pulse	rithw b	17	ger synt	nol on a	pulse	ratuo e	it io no	danima	ed. The t	ne stage selec
	width	70		-	90	-	105	-	ns	2.0	tine RS clocks
t _w	A = HIGH	14	6	-	18	-	21	-	ns	4.5	Fig.6
	_	12	5	-	15	-	18	-	ns	6.0	
	B = LOW										
	master reset	70	19	-	90		105	-	ns	2.0	
t _w	pulse width	14	7	-	18	-	21	-	ns	4.5	Fig.7
	HIGH	12	6	-	15		18	-	ns	6.0	
THE PART	clock pulse	80	25	-	100	-	120	-	ns	2.0	
t _w	width RS:	16	9	_	20	_	24	-	ns	4.5	Fig.8
**	HIGH or LOW	14	7	_	17	-	20	-	ns	6.0	
	minimum										
	output pulse	_	275	_	_	-	_	_	ns	2.0	
tw	width	_	100	_	_	-	_	_	ns	4.5	Fig.6; note 1
·W	Q = HIGH,	-	80		_	_	_	_	ns	6.0	1 19.0, 11010 1
	$\overline{Q} = LOW$		00						113	0.0	
		-	0	-	-	_	-	_	ns	2.0	
t _{rt}	retrigger time		0	_	_	_		_	ns	4.5	Fig.10; note 2
Ч	A, B	_	0		_	_	_		ns	6.0	1 19.10, 11016 2
		-	0			-		-	113	0.0	
0	external timing	5	-	1000	-	-	-	-	kΩ	2.0	5:- 40
R _{EXT}	resistor	1	-	1000	-	-	-	-	kΩ	5.0	Fig.13
						-		-			
C_{EXT}	external timing	50	no limi	ite					pF	2.0	Fig.13
CEXT	capacitor	50	110 11111						pF	5.0	1 lg. 13
THE T		120	39	-	150	_	180	-	ns	2.0	
t _{rem}	removal time	24	14	_	30	-	36	_	ns	4.5	Fig.7
10/11	MR to A, B	20	11	1	26	_	31	_	ns	6.0	

SYMBOL					T _{amb} (°C	3a 0a	TEST CONDITION				
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{cc}	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX		(V)	WAVEFORMS
f _{max}	maximum clock pulse frequency	2 10 12	5.9 18 21	MIM	1.8 8 10	Min	1.3 6.6 8	TYP_	MHz MHz MHz	2.0 4.5 6.0	Fig.8; note 3
f _{max}	maximum clock pulse frequency	6 30 35	24.8 75 89		4.8 24 28		4 20 24	28 - 22 - 61 -	MHz MHz MHz	2.0 4.5 6.0	Fig.9; note 4

Notes to the AC Characteristics

- 1. One stage selected.
- 2. It is possible to retrigger directly after the trigger pulse, however the pulse will only be extended, if the time period exceeds the clock input cycle time divided by 2.
- One stage selected. The termination of the output pulse remains synchronized with respect to the falling edge of the RS clock input.
- 4. One stage selected. The termination of the output pulse is no longer synchronized with respect to the falling edge of the RS clock input.

74HC/HCT5555

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specification".

Output capability: non-standard; bus driver with extended specification on V_{OH} and V_{OU} I_{OC} category: MSI.

Alti 6/2-	= al NGO OGO	0.0			T _{amb} (°C	;)				TE	ST C	NOITION
SYMBOL	PARAMETER	+25			-40 t	to +85	-0 to	+125	UNIT	V _{cc}	.,	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	3.98	(V)	V,	OTHER
V _{OH}	HIGH level output voltage Q and Q outputs	4.4	4.5	-	4.4	- 4.	4.4	4.5	V	4.5	ollagu Dilagu	Ι _ο = -20 μΑ
V _{OH}	HIGH level output voltage Q and Q outputs	3.98	4.32		3.84	= 4.	3.7	4.5	V	4.5		$I_o = -6 \text{ mA}$
V _{OH}	HIGH level output voltage Q and Q outputs	3.3	- _V		3	= A8.	2.7	-	V _{a.E}	4.5	HOI uput upatto	$I_0 = -20 \text{ mA}$
V _{OL}	LOW level output voltage Q and Q outputs	45-	0 V	0.1	- 8	0.1	83.0	0.1	v –	4.5	l WC	Ι _ο = 20 μΑ
V _{OL}	LOW level output voltage Q and Q outputs	4.5	0.15	0.26	-	0.33	- r.x	0.40	V	4.5	a wc	I _o = 6 mA
V _{OL}	LOW level output voltage Q and Q outputs	4.5	- V	0.9	- 8	1.14	3.26	1.34	V	4.5	oltage Aput	l _o = 20 mA

74HC/HCT5555

					T _{amb} (°	C)				CHAS	TEST CON	IDITION	
SYMBOL	PARAMETER	nily spe	+25	section	-40 1	-40 to +85		-0 to +125		V _{cc}	cteristics see	or the DO chara	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	v revitt	(V)	non-standard	OTHER	
иогла	TEST COI	3.98	_	-	3.84	(0°)	3.7	-	V	4.5	RS = GND; OSC CON = V _{CC}	l _o = -2.6 mA	
	y soV 1	IMU	125	of 0-	85	- 01 04	-		ES+		RS = V _{CC} ;	SYMBOL PA	
	HIGH level	3.98	XAM	-MM	3.84	141	3.7	ANA	V	4.5	OSC CON = GND; untriggered	$I_0 = -0.65 \text{ mA}$	
V _{OH} Au US-=	voltage R _{TC} output	4.4	4.5	A.	4.4	-	4.4	-	4.5 V	4.5	RS = V _{CC} ; OSC CON = V _{CC}	I _o = -20 μA	
Am ∂⊷ ⊭	4.5	4.4	4.5	- T.	4.4	- 2	4.4	_	V	4.5	RS = V _{CC} ; OSC CON = GND; untriggered	Ι _ο = -20 μΑ	
AIV _{OH}	HIGH level output voltage C _{TC} output	3.98	-	_ ₹.	3.84	-	3.7	-	V	4.5	RS = V _{IH} ; OSC CON = V _{IH}	$I_0 = -3.2 \text{ mA}$	
Au OS =	LOW level	- v	- 1.0	0.26	_	0.33	-	0.4	v o	4.5	RS = V _{CC} ; OSC CON = V _{CC}	I _o = 2.6 mA	
V _{OL}	voltage R _{TC} output	- v	0 0.40	0.1	3	0.1	-	0.1	V 0.15	4.5	RS = V _{CC} ; OSC CON = V _{CC}	Ι _ο = 20 μΑ	
V _{OL}	LOW level output voltage C _{TC} output	- V	- 1.34	0.26	4 -	0.33	-	0.4	V	4.5	RS = V _{IL} ; OSC CON = V _{IL} ; untriggered	l _o = 3.2 mA	

Notes to HCT DC Characteristics

- 1. The RS input has CMOS input switching levels.
- 2. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in Table 1.

74HC/HCT5555

UNIT LOAD COEFFICIENT

SMBOSBVAN	INPUT			40			UNIT LOAD COEFFICIENT		
	MR	XAX HBM	XAM	NIM	XAM	SAL	0.35		
El villa	A				nane		0.69	natxa	
	B						0.50	resist	140
Fig.13	RTR/RTR		atim	on			0.35	nente	Cent
	OSC CON								
Fig.7	S ₀ - S ₂	- as	11 -12	30	-	l bi	0.65	of Flat	inan
	S ₃						0.40	alex BOT	

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$.

	4.5 Frig.9	MHZ		os j	amb (°C	()			30	TEST	CONDITION
SYMBOL	PARAMETER		+25		-40 t	0 +85	-40 to	+125	UNIT	V _{cc}	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	eristics	(V)	WAVEFORMS
t _{PLH} /t _{PHL}	propagation delay A, B to Q, Q	n ec yk	28	48	ew <u>r</u> wo	60	trigger d by 2.	72	ns	4.5	Fig.6
t _{PHL} /t _{PLH}	propagation delay MR to Q,	eer diw	24	41	remain	51	quo er	62	ns	4.5	Fig.7
t _{PHL} /t _{PLH}	propagation delay RS to Q,	-	32	54	-	68	-	81	ns	4.5	Fig.8; note 1
t_{THL}/t_{TLH}	output transition time	-	7	15	-	19	-	22	ns	4.5	Fig.6
t _w	trigger pulse width A = HIGH B = LOW	21	12	-	26	-	32	-	ns	4.5	Fig.6
t _w	master reset pulse width HIGH	14	5	-	18	-	21	-	ns	4.5	Fig.7
t _w	clock pulse width RS; HIGH or LOW	16	9	-	20	-	24	-	ns	4.5	Fig.8
t _w	minimum output pulse width Q = HIGH, \overline{Q} = LOW	-	100	-		-	-	-	ns	4.5	Fig.6
t _{rt}	retrigger time A, B	-	0	-	-	-	-	-	ns	4.5	Fig.10; note 2

74HC/HCT5555

	PARAMETER			- 1	amb (°C)				TEST CONDITION		
SYMBOL		+25			-40 to +85		-40 to +125		UNIT	V _{cc}		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	8M	(V)	WAVEFORMS	
R _{EXT}	external timing resistor	a.o ₁	-	1000	_	-	-		kΩ A	4.5	Fig.13	
C _{EXT}	external timing capacitor	50		no limits					pF	4.5	Fig.13	
t _{rem}	removal time MR to A, B	24	14	-	30	-	36	-	ns -	4.5	Fig.7	
f _{max}	maximum clock pulse frequency	10	18	-	8	-	6.6	-	MHz	4.5	Fig.8; note 3	
f _{max}	maximum clock pulse frequency	30	75	-	24	naT	20	-	MHz	4.5	Fig.9; note 4	

Notes to HCT AC characteristics

- 1. One stage selected.
- 2. It is possible to retrigger directly after the trigger pulse, however the pulse will only be extended, if the time period exceeds the clock input cycle time divided by 2.
- 3. One stage selected. The termination of the output pulse remains synchronized with respect to the falling edge of the RS clock input.
- 4. One stage selected. The termination of the output pulse is no longer synchronized with respect to the falling edge of the RS clock input.

74HC/HCT5555



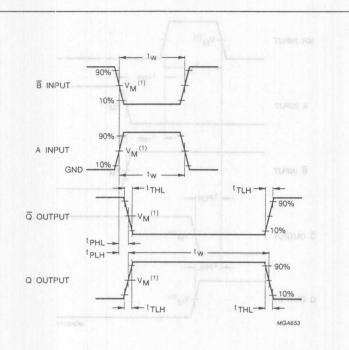
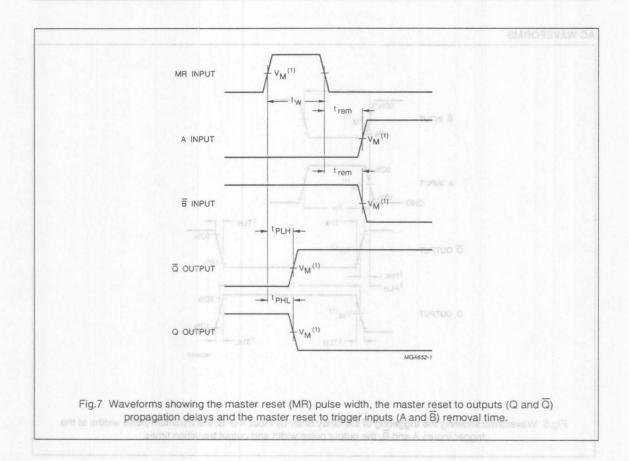
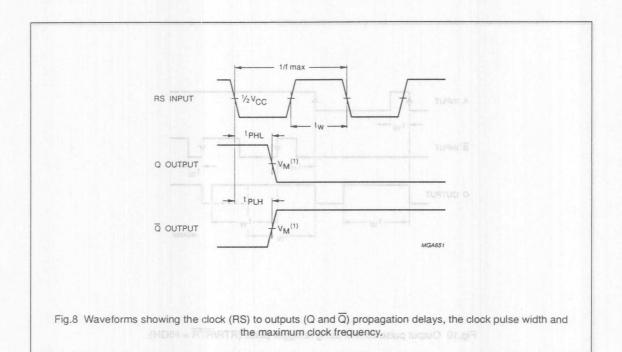


Fig.6 Waveforms showing the triggering of the delay timer by input A or \overline{B} , the minimum pulse widths of the trigger inputs A and \overline{B} , the output pulse width and output transition times.





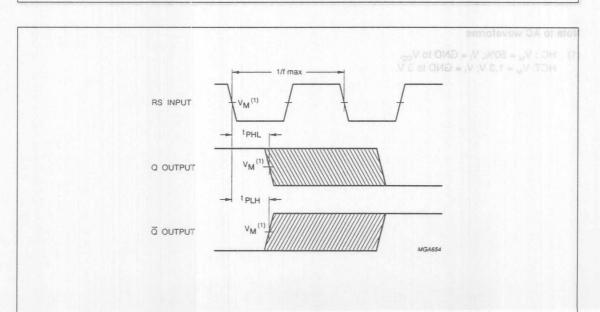
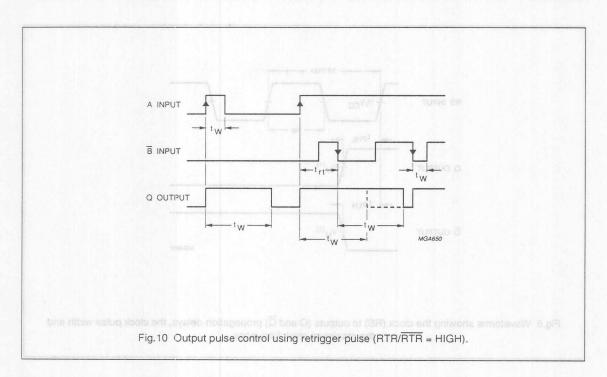


Fig.9 Waveforms showing the clock (RS) to outputs (Q and \overline{Q}) propagation delays, the clock pulse width and the maximum clock frequency (Output waveforms are not synchronized with respect to the RS waveform).



Note to AC waveforms

(1) HC: $V_M = 50\%$; $V_I = GND \text{ to } V_{CC}$. HCT: $V_M = 1.3 \text{ V}$; $V_I = GND \text{ to } 3 \text{ V}$.

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APPLICATION INFORMATION

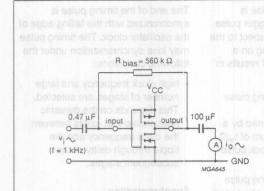


Fig.11 Test set-up for measuring forward transconductance $g_{is} = di_o/dv_i$ at v_o is constant (see Fig.12) and MR = LOW.

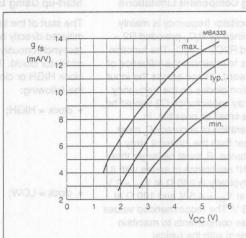
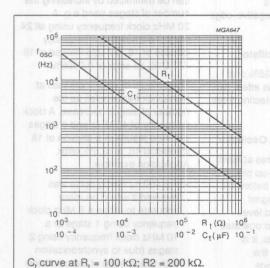
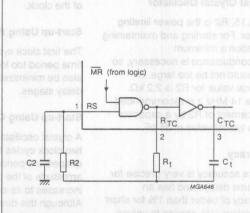


Fig.12 Typical forward transconductance g_{ts} as a function of the supply voltage at V_{CC} at $T_{amb} = 25$ °C.



 R_t curve at C_t = 1 nF; R2 = 2 x R_t . RC oscillator frequency as a function of R_t and C_t at V_{CC} = 2 to 6 V; T_{amb} = 25 °C.

Fig. 13 Application information.



Typical formula for oscillator frequency:

$$f_{\rm osc} = \frac{1}{2.5 \times R_t \times C_t}$$

Fig.14 Example of an RC oscillator.

74HC/HCT5555

Timing Component Limitations

The oscillator frequency is mainly determined by R₁C₁, provided R2 ≈ 2R, and R2C2 << R,C,. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C, must be larger than the inherent stray capacitance. R, must be larger than the "ON" resistance in series with it, which typically is 280 Ω at $V_{cc} = 2 \text{ V}$, 130 Ω at V_{CC} = 4.5 V and 100 Ω at $V_{cc} = 6 \text{ V}$. The recommended values for these components to maintain agreement with the typical oscillation formula are:

 $C_t > 50$ pF, up to any practical value, $10 \text{ k}\Omega < R_t < 1 \text{ M}\Omega$.

In order to avoid start-up problems, R, $\gg 1 \text{ k}\Omega$.

Typical Crystal Oscillator

In Fig.15, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 k Ω . Above 14 MHz it is recommended replacement of R2 by a capacitor with a typical value of 35 pF.

Accuracy

Device accuracy is very precise for long time delays and has an accuracy of better than 1% for short time delays (1% applies to values ≥400 ns). Tolerances are dependent on the external components used, either RC network or crystal oscillator.

Start-up Using External Clock

The start of the timing pulse is initiated directly by the trigger pulse (assynchronously with respect to the oscillator clock). Triggering on a clock HIGH or clock LOW results in the following:

- clock = HIGH; the timing pulse may be lengthened by a maximum of t_w/2 (t_w = clock pulse width)
- clock = LOW; the timing pulse may be shortened by a maximum of t_w/2 (t_w = clock pulse width).

This effect can be minimized by selecting more delay stages. When using only one or two delay stages, it is recommended to use an external time base that is synchronized with the negative-edge of the clock.

Start-up Using RC Oscillator

The first clock cycle is ≈35% of a time period too long. This effect can also be minimized by selecting more delay stages.

Start-up Using Crystal Oscillator

A crystal oscillator requires at least two clock cycles to start-up plus an unspecified period (ms) before the amplitude of the clock signal increases to its expected level.

Although this device also operates at lower clock amplitudes, it is recommended to select the continuously running mode (OSC CON = HIGH) to prevent start-up delays.

Termination of the Timing Pulse

The end of the timing pulse is synchronized with the falling edge of the oscillator clock. The timing pulse may lose synchronization under the following conditions:

 high clock frequency and large number of stages are selected.
 This depends on the dynamic relationship that exists between the clock frequency and the ripple through delay of the subsequent stages.

Synchronization

When frequencies higher than those specified in the Table 'Synchronization limits' are used, the termination of timing pulse will lose synchronization with the falling edge of the oscillator. The unsynchronized timing pulse introduces errors, which can be minimized by increasing the number of stages used e.g. A 20 MHz clock frequency using all 24 stages will result in a frequency division of 16 777 225 instead of 16 777 216, an error of 0.0005%.

The amount of error increases at high clock frequencies as the number of stages decrease. A clock frequency of 40 MHz and 4 stages selected results in a division of 18 instead of 16, a 12.5% error. Application example:

 If a 400 ns timing pulse was required it would be more accurate to utilize a 5 MHz clock frequency using 1 stage or a 10 MHz clock frequency using 2 stages (due to synchronization with falling edge of the oscillator) than a 40 MHz clock frequency and 4 stages (synchronization is lost).

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Minimum Output Pulse Width

The minimum output pulse width is determined by the minimum clock pulse width, plus the maximum propagation delay of A, \overline{B} to Q. The rising edge of Q is dominated by the A, \overline{B} to Q propagation delay, while the falling edge of Q is dominated by RS to Q propagation delay. These propagation delays are not equal.

The RS to Q propagation delay is some what longer, resulting in inaccurate outputs for extremely short pulses. The propagation delays are listed in the section 'AC Characteristics'. With these numbers it is possible to calculate the maximum deviation (an example is shown in Fig.16). Figure 16 is valid for an external clock where the

trigger is synchronized to the falling edge of the clock only. The graph shows that the minimum programmed pulse width of 100 ns is:

- · minimum of 4% too long
- · typically 7% too long
- · maximum of 10% too long.

SYNCHRONIZATION LIMITS

NUMBER OF STAGES SELECTED	CLOCK FREQUENCY (TYPICAL)
1	18 MHz
2	14 MHz
3	11 MHz
4	9.6 MHz
5	8.3 MHz
6	7.3 MHz
7	6.6 MHz
8	6 MHz
17	3.2 MHz
18	3.0 MHz
19	2.9 MHz
20	2.8 MHz
21	2.7 MHz
22	2.6 MHz
23	2.5 MHz
24	2.4 MHz

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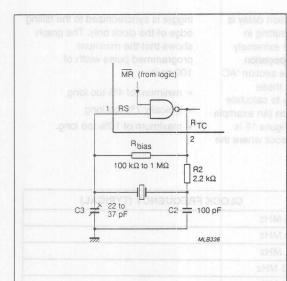


Fig.15 External components configuration for a crystal oscillator.

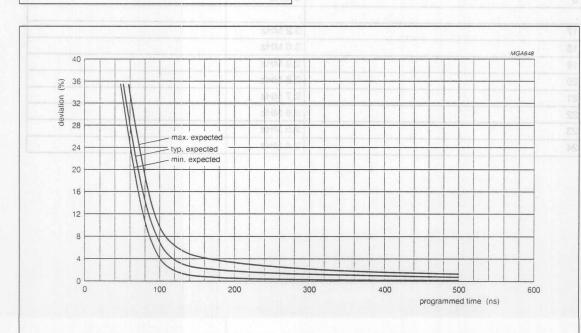


Fig.16 Graphic representation of short time delay accuracy; one stage selected; $V_{\rm CC}$ = 4.5 V.

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FEATURES

- · 8-pin space saving package
- Programmable 3-stage ripple counter
- Suitable for over-tone crystal application up to 50 MHz (V_{CC} = 5 V ± 10%)
- · 3-state output buffer
- · Two internal capacitors
- Recommended operating range for use with third overtone crystals 3 to 6 V
- Oscillator stop function (MR)
- Output capability: bus driver → (15 LSTTL)
- I_{cc} category: MSI.

APPLICATIONS

- Control counters
- Timers
- Frequency dividers
- · Time-delay circuits
- CIO (Compact Integrated Oscillator)
- Third-overtone crystal operation.

applied. On-chip capacitors minimize external component count for third overtone crystal applications.

The oscillator may be replaced by an external clock signal at input X1. In this event the other oscillator pin (X2) must be floating. The counter advances on the negative-going transition of X1. A LOW level on MR resets the

counter, stops the oscillator and sets the output buffer in the 3-state condition. $\overline{\rm MR}$ can be left floating since an internal pull-up resistor will make the $\overline{\rm MR}$ inactive. In the HCT version, the $\overline{\rm MR}$ input and the two mode select pins S1 and S2 are TTL compatible, but the X1 input has CMOS input switching levels and may be driven by a TTL output using a pull-up resistor connected to V_{CC}.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25 \, ^{\circ}\text{C}$; $t_r = t_f = 6 \, \text{ns}$.

OVMBOL	DADAMETER	CONDITIONS	Т	YP.	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
t _{PHL} /t _{PLH}	propagation delay X1 to OUT (S1 = S2 = LOW)	C _L = 15 pF V _{CC} = 5 V	17	17	ns
f _{max}	maximum clock frequency	SX 2	90	90	MHz
Cı	input capacitance except X1 and X2	CHLARM	3.5	3.5	pF
		÷1; notes 1 and 2	54	54	pF
_	power dissipation	÷2; notes 1 and 2	42	42	pF
C _{PD}	capacitance per package	÷4; notes 1 and 2	36	36	pF
	paskago	÷8; notes 1 and 2	33	33	pF

GENERAL DESCRIPTION

The HC/HCT6323A are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The HC/HCT6323A are oscillators designed for quartz crystal combined with a programmable 3-state counter, a 3-state output buffer and an overriding asynchronous master reset (MR). With the two select inputs S1 and S2 the counter can be switched in the divide-by-1, 2, 4 or 8 mode. If left floating the clock is divided by 8. The oscillator is designed to operate either in the fundamental or third overtone mode depending on the crystal and external components

Notes

 C_{PD} is used to determine the dynamic power dissipation (P $_{D}$ in $\mu W):$

 $P_D = (C_{PD} \times V_{CC}^2 \times f_i) + (C_L + V_{CC}^2 \times f_o) + (I_{pull-up} \times V_{CC})$ where:

 f_i = input frequency in MHz.

f_o = output frequency in MHz.

V_{CC} = supply voltage in V.

C_L = output load capacitance in pF.

I_{pull-up} = pull-up currents in μA.

For HC and HCT an external clock is applied to X1 with:

 $t_i = t_i \le 6$ ns, V_i is GND to V_{CC} , $\overline{MR} = HIGH$

 $I_{pull-up}$ is the summation of $-I_1$ (μ A) of S1 and S2 inputs at the LOW state.

ORDERING INFORMATION

EXTENDED TYPE	g.3 Fun	PAC	CKAGE	
NUMBER	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT6323AD	8	SO	plastic	SOT96

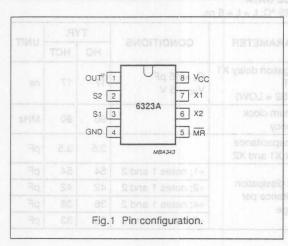
74HC/HCT6323A

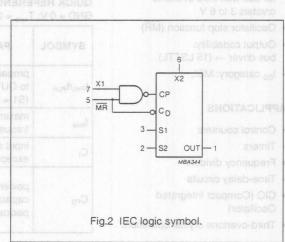
PINNING

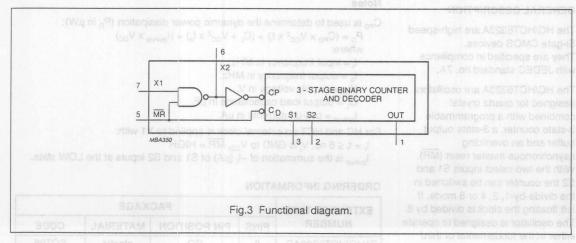
SYMBOL	PIN	DESCRIPTION
OUT	u-liq	counter output
S1 - S2	3, 2	mode select inputs for divide by 1, 2, 4 or 8
GND	4	ground (0 V)
MR ons aleve	5	master reset (active LOW)
X2	6	oscillator pin
X1 0 0 0 0 0 0	7	clock input/oscillator pin
V _{cc}	8	positive supply

FUNCTION TABLE

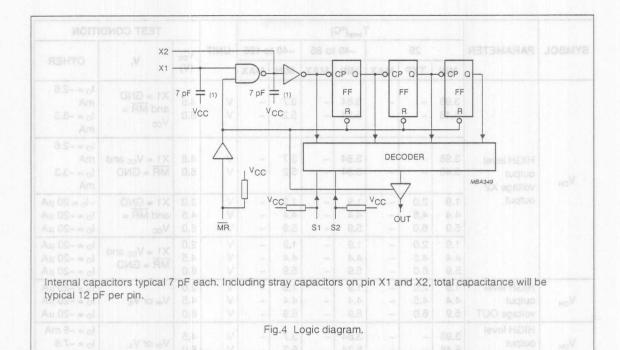
INPUT	package 2	OUTPUTS
applic 12 ms.	S2 908	- ald OUT
The os Ollator ma	0	f _i ^{TSUNDOO}
an extronal clock	ine cryster	f _i /2
In this event the	0	f _i /4
eogewhs setrum	1	f _i /8







74HC/HCT6323A



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family Characteristics", section "Family Specifications".

Output capability: non-standard; bus driver (except for X2)

Icc category: MSI.

Voltages are referenced to GND (ground = 0 V).

DC CHARACTERISTICS FOR 74HC

OF VII. 10 = 20 HA		V C		V	Γ _{amb} (°C	;)		TEST CONDITION				
SYMBOL PARAMETER	25			-40	-40 to 85		-40 to 125		V _{cc}	Javal WO	OTLIER	
	MIN	TYP	MAX	MIN	MAX	MIN	MAX	0	(V)	V _i tuqu	OTHER	
	HIGH level	1.5	1.2	_	1.5	-	1.50		V	2.0	TOO OUR	
VIH	input voltage	3.15	2.4	-	3.15	-	3.15	-	V	4.5	nout leakage	
	MR, X1 input	4.2	3.2	4	4.2	-	4.20	-	V	6.0	1X toenus	
	LOW level	-	0.8	0.5	_	0.5	_	0.5	V	2.0		
VIL	input voltage	-	2.1	1.35	-	1.35	-	1.35	V	4.5	nput pull-up	
d Fig. 12	MR, X1 input	2 0.	2.8	1.80	_	1.8	_	1.8	V	6.0	annent St.	

74HC/HCT6323A

					T _{amb} (°C	;)					TEST COND	ITION
SYMBOL	PARAMETER		25		-40	to 85	-40 1	to 125	UNIT	V _{cc}	sx V,	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX		(V)	TX VI	OTHER
		3.98 5.48	- R		3.84 5.34	-	3.7 5.2	ig V	V	4.5	X1 = GND and MR = Vcc	$I_0 = -2.6$ mA $I_0 = -3.3$ mA
v outp	HIGH level output voltage X2	3.98 5.48	_8300 	080 -7	3.84 5.34	-	3.7 5.2	- -pv ₁	V	4.5 6.0	$\frac{X1}{MR} = V_{CC}$ and $\frac{X1}{MR} = \frac{X1}{MR} = \frac{X1}{MR}$	$I_0 = -2.6$ mA $I_0 = -3.3$ mA
	output	1.9 4.4 5.9	2.0 4.5 6.0	- 00 <u>V</u>	1.9 4.4 5.9	- 18	1.9 4.4 5.9	- I	V V	2.0 4.5 6.0	X1 = GND and MR = V _{CC}	$-I_0 = 20 \mu$ $I_0 = -20 \mu$ $I_0 = -20 \mu$
		1.9 4.4 5.9	2.0 4.5 6.0	- - -	1.9 4.4 5.9	-	1.9 4.4 5.9	- - -	V V	2.0 4.5 6.0	$\frac{X1 = V_{CC} \text{ and }}{MR = GND}$	$l_0 = -20 \mu $ $l_0 = -20 \mu$ $l_0 = -20 \mu$
V _{OH}	HIGH level output voltage OUT	1.9 4.4 5.9	2.0 4.5 6.0	- -	1.9 4.4 5.9	- - -	1.9 4.4 5.9	- - -	V V	2.0 4.5 6.0	V _{IH} or V _{IL}	$l_0 = -20 \mu$ $l_0 = -20 \mu$ $l_0 = -20 \mu$
V _{OH}	HIGH level output voltage OUT	3.98 5.48	-	-	3.84 5.34	igic dia	3.7 5.2	-	V	4.5 6.0	V _{IH} or V _{IL}	$l_0 = -6 \text{ mA}$ $l_0 = -7.8$ mA
V _{OL}	LOW level output voltage X2 output	illy S <u>p</u> i	in "Fair	0.26 0.26	eoitan	0.33	mily C	0.4	V V	4.5 6.0	$\frac{X1}{MR} = V_{CC}$ and	l ₀ = 2.6 m. l ₀ = 3.3 m.
		-	0 0 0	0.1 0.1 0.1	-	0.1 0.1 0.1	-	0.1 0.1 0.1	V V brius	2.0 4.5 6.0	$\frac{X1}{MR} = V_{CC}$ and $\frac{X1}{MR} = V_{CC}$	I _O = 20 μA I _O = 20 μA I _O = 20 μA
V _{OL} MC	LOW level ouput voltage OUT	- - -	0 0 0	0.1 0.1 0.1	- - -	0.1 0.1 0.1		0.1 0.1 0.1	V V V	2.0 4.5 6.0	V _{IH} or V _{IL}	I _O = 20 μA I _O = 20 μA I _O = 20 μA
V _{OL}	LOW level output voltage OUT	- (V)	<u> </u>	0.26 0.26	40 to	0.33 0.33	E MI	0.4	V V 9Y	4.5	V _{IH} or V _{IL}	I _O = 6 mA I _O = 7.8 m/s
±lu	input leakage current X1	- 0.0	-	0.1	20 -	1	2 -	E 1	μА	6.0	$\overline{MR} = V_{CC}$ $S1 = V_{CC}$ $S2 = V_{CC}$	M HIV
-1,	input pull-up current S1, S2 and MR	5	30	100		35 -		35 80	μА	6.0	GND	see Fig.11 and Fig.12
I _{cc}	quiescent supply current	-	-	8	-	80	-	160	μА	6.0	V _{cc} or GND	I _O = 0

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AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_t = 6 \text{ ns}$; $C_1 = 50 \text{ pF}$.

					T _{amb} (°C	C)		DV ast I	nanyal	T	EST C	ONDITION
SYMBOL	PARAMETER		25		-40	to 85	-40 t	to 125	UNIT	Vcc	V, S	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX		(V)	V ₁	OTHER
t _{PHL} /t _{PLH}	propagation delay X1 to OUT divide by 1	- - -	61 22 19	185 37 31	- - -	230 46 39	- T	275 55 47	ns ns ns	2.0 4.5 6.0	Fig.7	S1 = GND S2 = GND
t _{PHL} /t _{PLH}	propagation delay X1 to OUT divide by 2	1389	74 27 23	235 47 40	MAX.	290 58 49	- XAM	350 70 60	ns ns ns	2.0 4.5 6.0	Fig.7	S1 = GND S2 = V _{CC}
t _{PHL} /t _{PLH}	propagation delay X1 to OUT divide by 4		91 33 28	285 57 48	-	355 71 60	-	425 85 72	ns ns ns	2.0 4.5 6.0	Fig.7	S1 = V _{cc} S2 = GND
t _{PHL} /t _{PLH}	propagation delay X1 to OUT divide by 8		105 38 32	335 67 57	_ _ _ _ 8.0	415 83 71	= - 8.0	500 100 85	ns ns ns	2.0 4.5 6.0	Fig.7	S1 = V _{CC} S2 = V _{CC}
t _{PLZ} /t _{PHZ}	3-state output disable time MR to OUT	-	75 15 13	150 30 26		185 37 31	-	225 45 38	ns ns ns	2.0 4.5 6.0	Fig.8	e H
t _{PZL}	3-state output enable time MR to OUT	_	36 13 11	150 30 26		185 37 31	 - -as.r	225 45 38	ns ns ns	2.0 4.5 6.0	Fig.8	X
t _{PZH}	3-state output enable time MR to OUT	-	61 22 19	200 40 34	- 88.1	250 50 43	_50.1	300 60 51	ns ns ns	2.0 4.5 6.0	Fig.8	note 1
t _{THL} /t _{TLH}	output transition time	- - -	14 5 4	60 12 10		75 15 13	- - -	90 19 15	ns ns ns	2.0 4.5 6.0	Fig.7	
t _w	clock pulse width X1, HIGH or LOW	50 10 9	17 6.0 5	<u> </u>	60 12 10	- : : : : : : : : : : : : : : : : : : :	75 15 13		ns ns ns	2.0 4.5 6.0	Fig.7	NO HOV
t _w	master reset pulse width MR; LOW	80 16 14	22 8 7	İ	100 20 17	- - - _{b b}	120 24 20		ns ns ns	2.0 4.5 6.0	Fig.9	
t _{rem}	removal time MR to X1	100 20 17	19 7 6.0	<u> </u>	125 25 21	-	150 30 26	- - - 3 x	ns ns ns	2.0 4.5 6.0	Fig.9	R
f _{max}	maximum clock pulse frequency	10 50 59	17 85 100	<u> </u>	8 40 47	-	6.6 33 39	-	MHz MHz MHz	2.0 4.5 6.0	Fig.7	iv i

Note to the 74HC AC Characteristics

^{1.} t_{PZH} only applicable in the divide-by-1 mode and X1 must be HIGH.

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS Family Characteristics", section "Family Specifications".

Output capability: bus driver (except for X2).

I_{cc} category: MS1.

Voltages are referenced to GND (ground = 0 V).

	8.0 1.01	an		1	T _{amb} (°C	(2)					TEST CO	NDITION
SYMBOL	PARAMETER	en	25	25		-40 to 85		-40 to 125		V _{cc}	nejapan	ong
	4.5 Fig.7 S	MIN	TYP	MAX	MIN	MAX	MIN	MAX		(V)	no vispaq UO oVi x ya	OTHER
ViH	HIGH level input voltage MR, S1 and S2 inputs	2.0	425 85 - 72		2.0	-	2.0	8	V	4.5 to 5.5	ce by 2 pagation ay X1 to Ot de by 4	2.146.7
>>V = V = S	LOW level input voltage MR, S1 and S2 inputs	an - an an	300 100 85 – 225	0.8	33 71 -	0.8	133 17 17 18 18 18	0.8	V	4.5 to 5.5	pagation sy X1 to OL de by 8 (ate output	
V _{tH}	HIGH level input voltage X1 input	3.15 3.85	45 38 - 225 -	-	3.15 3.85	-	3.15 3.85	- 8 - 8	V	4.5 5.5	to OUT	PAN GHS GIS
V _{IL}	LOW level input voltage X1 input	ns –	38 -	1.35	- 18 - 08s	1.35	- a:	1.35 1.65	V	4.5 5.5	emin sign to OUT tuctue state	MR 3-s
1 50	6.0 Fig.8 III 6.0 2.0	3.98	51 _ 18 90	_	3.84		3.7	9 1	V	4.5	X1 = GND and MR = V _{CC}	$I_0 = -2.6 \text{ m/s}$
V _{OH}	HIGH level output	3.98	15	76	3.84	08	3.7	7	V 0	4.5	X1 = V _{CC} and MR = GND	$I_0 = -2.6 \text{ m/s}$
∨ ОН	voltage X2 output	4.4	4.5	13 _	4.4	01	4.4	2	٧	4.5	X1 = GND and MR = V _{CC}	I _O = -20 μA
	4.5 Fig.9 6.0 2.0	4.4	4.5	29 20 150	4.4	17 _	4.4	. e	V 8	4.5	X1 = V _{CC} and MR = GND	I ₀ = -20 mA
V _{OH}	HIGH level output voltage OUT	4.4	4.5	30 26 6.6	4.4	15	4.4	_ 0.	V	4.5	V _{IH} or V _{IL}	l _O = -20 μA
V _{OH}	HIGH level output voltage OUT	3.98	_	39	3.84	71	3.7	00	V	4.5	V _{IH} or V _{IL}	$I_0 = -6 \text{ mA}$

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				1	Tamb (°C	;)			TOH	SV HE	TEST CO	NDITION
SYMBOL	PARAMETER		25		-40	to 85	-401	to 125	UNIT	V _{cc}		271177
	BNOU 1831	MIN	TYP	MAX	MIN	MAX	MIN	MAX		(V)	V _t	OTHER
ОТНЕВ	LOW level output	7_	X/	0.26	M X	0.33	ых	0.4	V	4.5	$X1 = V_{CC}$ and \overline{MR} = V_{CC}	I _O = 2.6 mA
DNO = 12	voltage X2 output	4.	0	0.1	-	0.1	-	0.1	V	4.5	X1 = V _{CC} and MR = V _{CC}	Ι ₀ = 20 μΑ
V _{OL}	LOW level output voltage OUT	4	0	0.1	-	0.1		0.1	V	4.5	V _{IH} or V _{IL}	Ι ₀ = 20 μΑ
Vol 18	LOW level output voltage OUT	<u>-</u>	en en	0.26	-	0.33	-	0.4	V 35	4.5	V _{IH} or V _{IL}	I _O = 6 mA
S1 = Jl±c S2 = Voc	input leakage current	=	an a	0.1	-	1.0		1.0	μА	5.5	MR = V _{CC} ; S1 = V _{CC} ; S2 = V _{CC}	ond Hraymer dep
-1,	input pull-up current S1, S2 and MR	5	25	100	-	23	-	26.	μА	5.5	GND 1 sid	see Fig.11 and Fig.12
I _{cc}	quiescent supply current	.=	an.	8	-	80		160	μА	5.5	V _{cc} or GND	l ₀ = 0
t eton ess ΔI _{cc}	additional quiescent supply current per	4.	100	360		450	-	490	22 μΑ	5.5	V _{cc} or GND	other inputs at Vcc or GND;
	input pin for unit load coefficient is 1	7	en .	19		ar		2)	8		sition time	$l_0 = 0;$ (note 1)

Note to the HCT DC Characteristics

1. The value of additional quiescent supply current (ΔI_{CC}) for unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

UNIT LOAD COEFFICIENT

TUPUT A.S. FIG.7	UNIT LOAD COEFFICIENT
MR, \$1, \$2	frequency 0.40

74HC/HCT6323A

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_t = 6 ns; C_L = 50 pF$

	,V	201			T _{amb} (°C	()			L.	TEST CONDITION			
SYMBOL	PARAMETER		25	AW I II	-40	to 85	-40 t	o 125	UNIT	V _{cc}		OTHER	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX		(V)	V ₁	OTHER	
t _{PHL} /t _{PLH}	propagation delay X1 to OUT divide-by-1	4.5	24	40	-	50	-	60	ns	4.5	Fig.7	S1 = GND S2 = GND	
t _{PHL} /t _{PLH}	propagation delay X1 to OUT divide-by-2	4.5	29	50	-	62	-	75	ns	4.5	Fig.7	S1 = GND S2 = V _{CC}	
Am d	propagation delay X1 OUT to divide-by-4	4.5	35	60	- E	75	- 8	90	ns	4.5	Fig.7	S1 = V _{CC} S2 = GND	
t _{PHL} /t _{PLH}	propagation delay X1 OUT to divide-by-8	5.5	40	70	-	87	-	105	ns	4.5	Fig.7	S1 = V _{CC} S2 = V _{CC}	
t _{PLZ} /t _{PHZ}	3-state output disable time MR to OUT	8.6	21	35	-	43	- 0	52	ns	4.5	Fig.8	n Isi J-	
t _{PZ}	3-state output enable time MR to OUT	8.5	16	30	-	37	-	45	ns	4.5	Fig.8		
t _{PZH}	3-state output enable time MR to OUT	5.5	22 Au	38	-	47	- 0	57	ns	4.5	Fig.8		
t _{THL} /t _{TLH}	output transition time	-	5	12	-	15	-	19	ns	4.5	Fig.7		
t _w	clock pulse width X1, HIGH or LOW	10	6	-	12	-	15	-	ns	4.5	Fig.7	H ent or etc	
t _w	master reset pulse width MR; LOW	16	8	t to by	20	ligt (soli ing unit	24	pply cu this ve	ns	4.5	Fig.9	The value	
t _{rem}	removal time	24	12	-	30	-	36	-	ns	4.5	Fig.9	NIT LOAD	
f _{max}	maximum clock pulse frequency	50	85	_	40	-	33	-	MHz	4.5	Fig.7		

Note to the 74HCT AC Characteristics

^{1.} $t_{\mbox{\scriptsize PZH}}$ only applicable in the divide-by-1 mode and X1 must be HIGH.

74HC/HCT6323A

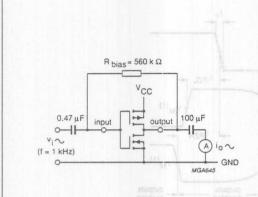


Fig.5 Test set-up for measuring forward transconductance $g_{fs} = di_{o}/dv_{i}$ at v_{o} is constant (see also Fig.6); MR = HIGH.

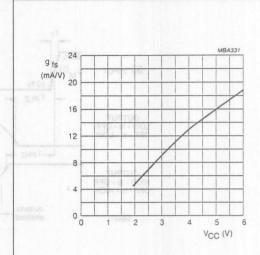


Fig.6 Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at $T_{amb} = 25$ °C.

Fig.8 Waveforms showing the input MR to

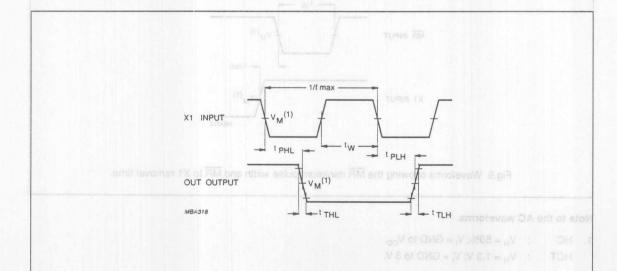


Fig.7 Waveforms showing the clock (X1) to output (OUT) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

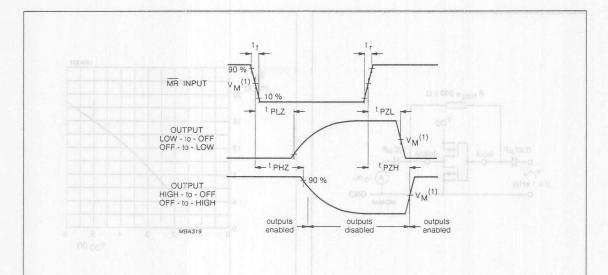
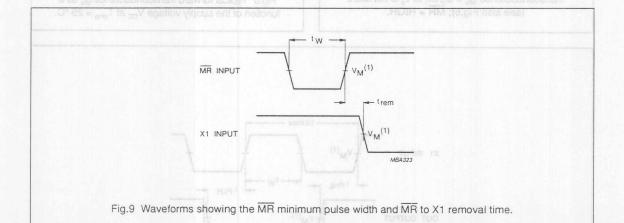


Fig.8 Waveforms showing the input MR to output OUT, 3-state enable and disable times.

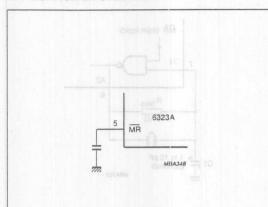


Note to the AC waveforms

1. HC : $V_M = 50\%$; $V_1 = GND$ to V_{CC} . HCT : $V_M = 1.3$ V; $V_1 = GND$ to 3 V.

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APPLICATION INFORMATION



The input pull-up current is used to create a power-on delay time at MR.

Fig.10 Power-on reset.

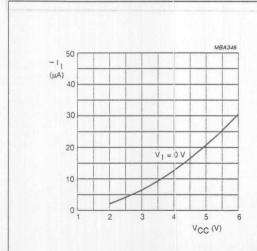


Fig.12 Typical input pull-up current as a function of the supply voltage (V_{cc}).

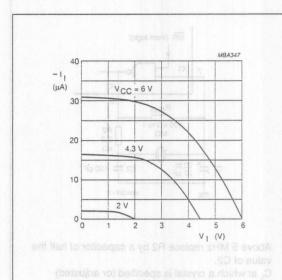


Fig.11 Typical input pull-up current as a function of the input voltage (V_I).

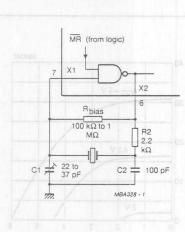
Table 1 Typical application values

f (MHz)	R2 (KΩ)	C1 (pF)	C2 (pF)		
1	4.7	47 to	68		
10	2.2	47 to	68		
25	1	33	33		

Table 2 Typical Application Values

f(MHz)	R _{bias} (ΚΩ)	C1(pF)	100000
50	3.0	4.7	

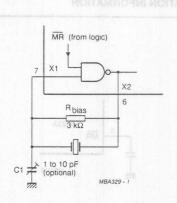
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Above 5 MHz replace R2 by a capacitor of half the value of C2.

 C_L at which a crystal is specified (or adjusted) equals for this application C1 . C2/C1 + C2.

Fig.13 Typical setup for a crystal oscillator operating in the fundamental mode (1 MHz to 25 MHz).



Applicable for third overtone crystals (lower damping resistance at the third harmonic frequency) at typical 50 MHz. For lower frequencies extra load capacitors must be supplied, or increase bias resistor.

Fig.14 Typical set-up for a crystal oscillator operating in the third overtone mode without the use of an inductor.

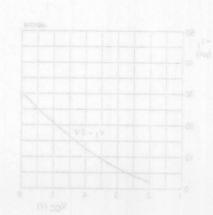


Fig.12 Typical input pull-up current as a function of the supply voltage (V_{cc)}...

74HC/HCT6323A

Typical Crystal Oscillator

In Fig.13, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 K Ω .

The oscillator has been designed to operate over a wide frequency spectrum, for quartz crystals operating in the fundamental mode and in the overtone mode. The circuit is a Pierce type oscillator and requires a minimum of external components. There are two on-chip capacitors, X1 and X2, of approximately 7 pF. Together with the stray and input capacitance the value becomes 12 pF for 8-pin SO packages. These values are convenient and make it possible to run the oscillator in the third overtone without external capacitors applied. If a certain frequency is chosen, the IC parameters, as forward transconductance, and the crystal parameters such as the motional resistances R1 (fundamental), R3 (third overtone) and R5 (fifth overtone), are of paramount importance. Also the values of the external components as R_s (series resistance) and the crystal load capacitances play an important role. Especially in overtone mode oscillations, R. (bias resistance) and the load capacitance values are very important.

Considerations for Fundamental Oscillator:

In the fundamental oscillator mode. the R_b has only the function of biasing the inverter stage, so that it operates as an amplifier with a phase shift of approximately 180°. The value must be high, i.e. $100 \text{ k}\Omega$ up to 10 M Ω . The load capacitors C1 and C2, must have a value that is suitable for the crystal being used. The crystal is designed for a certain frequency having a specific load capacitance. C1 can be used to trim the oscillation frequency. The series resistance reduces the total loop gain. One function of it is therefore to reduce the power dissipation in the crystal. R_s also suppresses overtone oscillations and introduces a phase shift over a broad frequency range. This is of less concern provided R_e is not too high a value.

Note

A combination of a small load capacitor value and a small series resistance, may cause a third overtone oscillation.

Considerations for Third-overtone Oscillator:

In the overtone configuration, series resistance is no longer applied. This is essential otherwise the gain for third overtone can be too small for oscillation. A simple solution to suppress the fundamental oscillation, is to spoil the crystal fundamental activity. By dramatically reducing the value of the bias resistor of the inverting stage, and applying small load capacitors, it is possible to have an insufficient phase in the total loop for fundamental oscillation. However the phase for third overtone is good. It can be explained by the R_b × C_t time constant. During oscillation the crystal with the load capacitors cause a phase shift of 180°. Because R, is parallel with the crystal (no R_s), R_h spoils the phase for fundamental. R_b × C₁ must be of a value, that it is not spoiling the phase for third overtone too much. Because third overtone is a 3 times higher frequency than the fundamental, the R_b × C_l cannot 'maintain' the higher third overtone frequency, which results in a less spoiled overtone phase.

74HC/HCT6323A

Typical Crystal Oscillator

n Fig. 13, R2 is the power limiting resistor. For starting and maintaining scallbuton a minimum ransconductance is necessary, so 72 should not be too large. A practical value for R2 is 2.2 KΩ.

The oscillator has been designed to operate over a wide frequency spectrum, for quartz crystals operating in the fundamental mode and in the overtone mode. The circuit is a Pierce type oscillator and requires a minimum of external capacitors, X1 and X2, of capacitors, X1 and X2, of approximately 7 pF. Together with the stray and input capacitance the value becomes 12 pF for 8-pin SO packages. These values are convenient and make it possible to convenient and make it possible to overtone without external capacitors overtone without external capacitors crystal parameters such as the forward transconductance, and the motional resistances P1 crystal parameters such as the parametrally, P3 (third overtone) and P5 (fifth overtone), are of parametral components as P4 (series resistance) and the crystal load capacitances play an overtone mode oscillations, P6 (bias operations) and the load capacitance values are vary important.

Considerations for Fundamental

In the fundamental oscillator mode, the R_b has only the function of blasing the inverter stage, so that it operates as an amplifier with a phase shift of approximately 180°. The value must be high, i.e. 100 kg. The value must be high, i.e. 100 kg. C1 and C2, must have a value that is suitable for the crystal being used. The crystal is designed for a certain frequency having a specific load frequency having a specific load made oscillation frequency. The series resistance reduces the total loop gain. One function of it is therefore to reduce the power dissipation in ceduce the power dissipation in the crystal. R_c also suppresses a phase shift over a broad frequency range. This is of less concern arounded R_c is not too high a value.

stol

A combination of a small load capacitor value and a small serier resistance, may cause a third overtone oscillation.

Considerations for Third-overtone Oscillator:

In the overtone configuration, series resistance is no longer applied. This is essential otherwise the gain for scallation. A simple solution to oscillation. A simple solution to suppress the fundamental solution to oscillation, is to spoil the crystal poscillation, is to spoil the crystal reducing the value of the bias reducing the value of the bias applying small load capacitors, it is possible to have an insufficient phase in the total loop for the phase for third overtone is good. The phase for third overtone is good, the phase for third overtone the phase of fundamental. By a Comparison the phase shift of 180°. The phase for fundamental By a Comparison the phase for third overtone too much. Secause third overtone too much. The phase for third overtone is a 3 times on a trained overtone is a 3 times on the higher third overtone is a 3 times on the higher third overtone is a 3 times the higher third overtone is a 3 times on the phase in third overtone is a 3 times the maintain' the higher third overtone is a 3 times on the phase in third overtone in a less poiled overtone phase.

Hex non-inverting precision Schmitt-trigger

74HC7014

FEATURES

- · Operating voltage 3 to 6 V
- · Output capability: standard
- · category: SSI

APPLICATIONS

 Wave and pulse shapers for highly noisy environments

DESCRIPTION

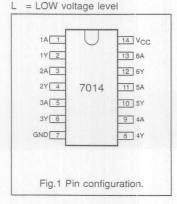
The 74HC7014 is a high-speed Si-gate CMOS device. It is specified in compliance with JEDEC standard no. 7A.

The 74HC7014 provides six precision Schmitt-triggers with non-inverting buffers. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. The precisely defined trigger levels are lying in a window between 0.55 x $V_{\rm CC}$ and 0.65 x $V_{\rm CC}$. This makes the circuit suitable to operate in a highly noisy environment. Input shorts are allowed to –1.5 V and 16 V without disturbing other channels.

FUNCTION TABLE

INPUT	OUTPUT		
nA	nΥ		
L	L		
Н	Н		

H = HIGH voltage level



QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25 \, ^{\circ}\text{C}$; $t_r = t_f = 6 \, \text{ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
V _{T+}	positive going threshold	C _L = 50 pF V _{CC} = 5 V	3.1	V
V _{T-}	negative going threshold	av	2.9	V
C ₁	input capacitance		3.5	pF
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	9	pF
Icc	DC supply current	diagram.	3.0	mA

Notes to the quick reference data

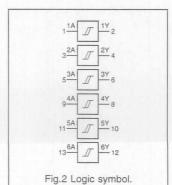
- 1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W): $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacity in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
- 2. For HC the condition is $V_1 = GND$ to V_{CC} .

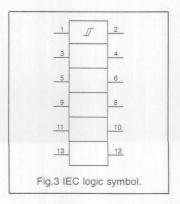
ORDERING INFORMATION

TYPE NUMBER	PACKAGE								
THE NUMBER	PINS	PIN POSITION	MATERIAL	CODE					
74HC7014P	14	DIL	plastic	SOT27					
74HC7014T	14	SO	plastic	SOT108A					

PINNING

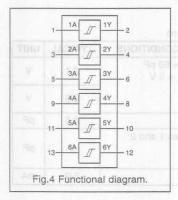
PIN NO.	SYMBOL	NAME AND FUNCTION				
1, 3, 5, 9, 11, 13	1A to 6A	data inputs				
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs				
7	GND	ground (0 V)				
14	V _{cc}	positive supply voltage				

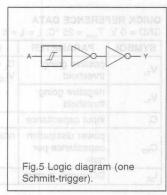




Hex non-inverting precision Schmitt-trigger

74HC7014





Notes to the quick reference data

. $C_{\rm ep}$ is used to determine the cyrramic power dissipation (P_0 in μW): $P_0 = C_{\rm ep} \times V_{\rm ec}^2 \times f_1 + \Sigma \left(C_{\rm i} \times V_{\rm ec} \times f_1\right)$ where: $f_1 = {\rm input}$ frequency in MHz; $C_0 = {\rm cutput}$ load capacity in pF; $f_2 = {\rm cutput}$ frequency in MHz; $V_{\rm ec} = {\rm suppiy}$ voltage in V; $\Sigma \left(C_1 \times V_{\rm ec}^2 \times f_1\right) = {\rm sum}$ of outputs.

REFRING INFORMATION

PINNING
PRI NO. SYMBOL NAME AND FUNCTION
1, 3, 5, 9, 11, 13, 1A to 6A data inputs
2, 4, 6, 8, 10, 12, 1Y to 6Y data outputs
7
GNO ground (0 V)

PEATURES

- Operating voltage 3 to 6 V
- Output capability: standart
 - 122 vropetso

RELICATIONS

Wave and pulse shapers for highly noisy environments

DESCRIPTION

The 74HC7014 is a high-speed Si-gate CMOS device. It is specified in compliance with JEDEC standard in compliance with JEDEC standard

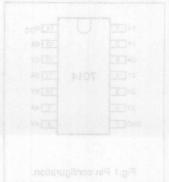
The 74HC7014 provides six procession Schmilt-ritggers with non-inverting buffers. It is capable of transforming slowly changing loput sanghals into strainly defined.

Ifter-free curput signals. The processe of the window between ping in a window between makes the circuit suitable to operate in a highly noisy snytronment throat singuts are allowed to -1.5 V and 16 V winout disturbing other

RINCHON TABLE

= HIGH voltage level





Hex non-inverting precision Schmitt-trigger 74HC7014

DC CHARACTERISTICS FOR 74HC

For the DC output characteristics see chapter "HCMOS family characteristics", section "Family specifications". Except for recommended operating conditions the 7014' has a DC supply voltage from minimum 3 V to maximum 6 V.

Transfer characteristics are given below.

Output capability: standard

Category: SSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

					T _{amb} ((C)				TEST CONDITIONS		
SYMBOL PARAI	PARAMETER	+25				to +85	-40 to +125		UNIT	V _{cc}	V ₁	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		(V)	(V)	OTHER
		-	1.86	1.95	-	1.95	-	1.95		3.00		
	o notiniteb ad priv	vorte	2.94	3.08	.pFl	3.08	-	3.08		4.75		ua Pi
V_{T+}	positive-going	-	3.10	3.25	4	3.25	-	3.25	V	5.00		Figs.6 and 7
	threshold	-	3.25	3.41	-	3.41	-	3.41		5.25		
		-	3.72	3.90	-	3.90	-	3.90		6.00		
		1.65	1.74	_	1.65	_	1.65	-		3.00	an an	BORSVAW
	81	2.62	2.76	A. (art)	2.62	M - [2.62	-		4.75		
V_{T-}	negative-going	2.75	2.90	-	2.75	-	2.75	-	V	5.00		Figs.6 and 7
threshold	threshold	2.89	3.05	W = 50	2.89	() -	2.89			5.25		
		3.30	3.48	-	3.30	-	3.30	-		6.00		
		50	120	-	50	-	50	-	1/	3.00	THE A	
	la contra de la contra del la contra de la contra del la contra del la contra de la contra de la contra del l	100	180	-	100	-	100	-		4.75		TURN As
V _H	hysteresis	120	200	-	120	-	120	-	mV	5.00		Figs.6 and 7
	$(V_{T+} - V_{T-})$	130	210	-	130	-	130	J=11-		5.25		ml .
		160	240	-	160	-	160	-		6.00		
					1197					V _{cc}	David	TUTTHO YA
		-	-	0.1	-	1.0	-	1.0	μА	or		
±I,	input leakage							11171-11		GND		
-11	current						100			16 V		
		-	-	0.5	-	5.0	-	5.0	μΑ	or		
								nt (An	Si reseri	GND		Havely A ni
		-	0.7	1.4	-	1.8	-	2.1	to bear	3.00	notispecon	y (Yn) tugnio
Icc	DC supply current	-	3.0	6.0	-	7.5	-	7.5	mA	5.25		mit nodlanst
		-	3.7	7.4	-	10.0	-	13.0		6.00		

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		T _{amb} (°C)								TEST CONDITIONS		
SYMBOL	PARAMETER	+25			-40 to +85 -40 to +			0 +125	UNIT	V _{cc}	WAVEFORMS	
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		(V)	WAVEFORMS	
	propagation	-	95	475	-	600	-	715		3.00		
tphL	delay	-	38	115	-	145	-	175	ns	4.75	Fig.8	
	nA, nB to nY	-	27	73	-	93	-	112		6.00		
	propagation	-	47	175	-	220	-	260		3.00		
t _{PLH}	delay	-	23	52	-	65	_	78	ns	4.75	Fig.8	
nA, nB to nY	nA, nB to nY	-	18	46	-	58	-	70		6.00		
	output transition	-	12	20	-	25	-	30		3.00		
t _{THL} /t _{TLH}	time	-	7	15	-	19	-	22	ns	4.75	Fig.8	
	ume	-	6	13	_	16	-	19		6.00		

Hex non-inverting precision Schmitt-trigger a maising principal

74HC7014

TRANSFER CHARACTERISTIC WAVEFORMS

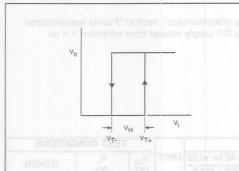


Fig.6 Transfer characteristic.

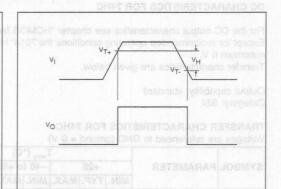


Fig.7 Waveforms showing the definition of $V_{T_{+}}, \ V_{T_{-}}$ and $V_{H}.$

AC WAVEFORMS

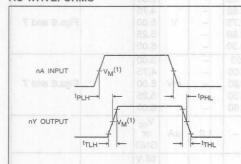
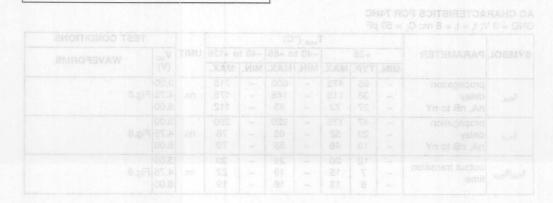


Fig.8 Waveforms showing the input (nA) to output (nY) propagation delay and the output transition times.

Note to the AC waveforms

(1)
$$V_M = 50\%$$
; $V_I = GND$ to V_{CC} .



9-BIT x 64-WORD FIFO REGISTER: 3-STATE

FEATURES THIRDESO JARBUEL

- Synchronous or asynchronous operation
- 3-state outputs
- Master-reset input to clear control functions
- 33 MHz (typ.) shift-in, shift-out rates with or without flags
- Very low power consumption
- Cascadable to 25 MHz (typ.)
- Readily expandable in word and bit dimensions
- Pinning arranged for easy board layout: input pins directly opposite output pins
- Output capability: standard
- · Icc category: LSI

GENERAL DESCRIPTION

The 74HC/HCT7030 are high-speed Si-gate CMOS devices specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7030 is an expandable, First-In First-Out (FIFO) memory organized as 64 words by 9 bits. A 33 MHz data-rate makes it ideal for high-speed applications. Even at high frequencies, the ICC dynamic is very low (fmax = 18 MHz; VCC = 5 V produces a dynamic ICC of 80 mA). If the device is not continuously operating at fmax, then ICC will decrease proportionally.

With separate controls for shift-in (SI) and shift-out (SO), reading and writing operations are completely independent,

GND 1	250000	28 Vcc
GND 2		27 MR
DIR 3		26 SO
SI 4		25 DOR
D ₀ 5		24 00
D ₁ 6		23 01
D ₂ 7	7020	22 02
D ₃ 8	7030	21 03
		20 04
D ₅ 10		19 Q ₅
06 11		18 06
D ₇ 12		17 07
D ₈ 13		16 Q8
GND 14		15 OE
(qu-slddua)	729388	7.1 9/11 el

SYMBOL	PARAMETER	CONDITIONS	TYP	LINUT		
	PARAMETER	CONDITIONS	НС	нст	UNIT	
^t PHL [/]	propagation delay MR to DIR and DOR SO to Q _n	C _L = 15 pF V _{CC} = 5 V	21 36	26 40	ns ns	
fmax	maximum clock frequency SI and SO	VCC = 5 V	33	29	MHz	
CI	input capacitance	mars I	3.5	3.5	pF	
Ср	power dissipation capacitance per package	notes 1 and 2	660	660	pF	

GND = 0 V;
$$T_{amb}$$
 = 25 °C; t_r = t_f = 6 ns

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

- fo = output frequency in MHz
 - VCC = supply voltage in V q and or arow
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
- For HCT the condition is $V_I = GND$ to $V_{CC} 1.5 V$

PACKAGE OUTLINES

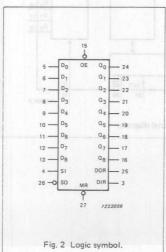
28-lead DIL; plastic (SOT117).

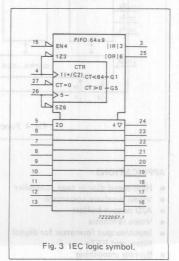
28-lead mini-pack; plastic (SO28; SOT136A).

allowing synchronous and asynchronous data transfers. Additional controls include a master-reset input (MR) and an output enable input (OE). Flags for data-in-ready (DIR) and data-out-ready (DOR) indicate the status of the device.

Devices can be interconnected easily to expand word and bit dimensions. All output pins are directly opposite the corresponding input pins thus simplifying board layout in expanded applications.

(continued on next page)



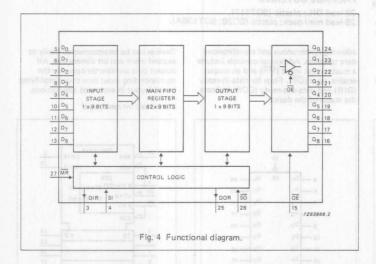


PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	JOENYS
1, 2, 14	GND	ground (0 V)	
3 80	DIR	data-in-ready output	
4 an 04-	Ste Ager	shift-in input (LOW-to-HIGH, edge	-triggered)
5, 6, 7, 8, 9, 10, 11, 12, 13	D ₀ to D ₈	parallel data inputs	
15 Aq 8.E	ŌĒ	output enable input (active LOW)	
24, 23, 22,		power dissipation - notes	
21, 20, 19, 18, 17, 16	Q ₀ to Q ₈	3-state parallel data outputs	
25	DOR	data-out-ready output	
26	SO	shift-out input (HIGH-to-LOW, edg	ge-triggered)
27	MR 09) nonsqia	asynchronous master-reset input (a	ctive LOW)
28	VCC	positive supply voltage	

Note to the pin description

Pin 14 must be connected to GND. Pins 1 and 2 can be left floating or connected to GND, however it is not allowed to let current flow in either direction between pins 1, 2 and 14.



APPLICATIONS

- · High-speed disc or tape controller
- Video timebase correction
- A/D output buffers
- Voice synthesis
- Input/output formatter for digital filters and FFTs
- · Bit-rate smoothing

GENERAL DESCRIPTION

INPUTS AND OUTPUTS

Data inputs (Do to Da)

As there is no weighting of the inputs, any input can be assigned as the MSB. The size of the FIFO memory can be reduced from the 9×64 configuration, i.e. $8\times64, 7\times64,$ down to $1\times64,$ by tying unused data input pins to V_{CC} or GND.

Data outputs (Q₀ to Q₈)

As there is no weighting of the outputs, any output can be assigned as the MSB. The size of the FIFO memory can be reduced from the 9 x 64 configuration as described for data inputs. In a reduced format, the unused data output pins must be left open circuit.

Master-reset (MR)

When $\overline{\text{MR}}$ is LOW, the control functions within the FIFO are cleared, and data content is declared invalid. The data-in-ready (DIR) flag is set HIGH and the data-out-ready (DOR) flag is set LOW. The output stage remains in the state of the last word that was shifted out, or in the random state existing at power-up.

Status flag outputs (DIR, DOR)

Indication of the status of the FIFO is given by two status flags, data-in-ready (DIR) and data-out-ready (DOR):

- DIR = HIGH indicates the input stage is empty and ready to accept valid data:
- DIR = LOW indicates that the FIFO is full or that a previous shift-in operation is not complete (busy):
- DOR = HIGH assures valid data is present at the outputs Q₀ to Q₈ (does not indicate that new data is awaiting transfer into the output stage):
- DOR = LOW indicates the output stage is busy or there is no valid data.

Shift-in control (SI)

Data is loaded into the input stage on a LOW-to-HIGH transition of SI. A HIGH-to-LOW transition triggers an automatic data transfer process (ripple through). If SI is held HIGH during reset, data will be loaded at the rising edge of the MR signal.

Shift-out control (SO)

A LOW-to-HIGH transition of \$\overline{SO}\$ causes the DOR flags to go LOW. A HIGH-to-LOW transition of \$\overline{SO}\$ causes upstream data to move into the output stage, and empty locations to move towards the input stage (bubble-up).

(continued on next page)

Output enable (OE)

The outputs Ω_0 to Ω_8 are enabled when \overline{OE} = LOW. When \overline{OE} = HIGH the outputs are in the high impedance OFF-state.

FUNCTIONAL DESCRIPTION

Data input

Following power-up, the master-reset (\overline{MR}) input is pulsed LOW to clear the FIFO memory (see Fig. 8). The data-in-ready flag (DIR = HIGH) indicates that the FIFO input stage is empty and ready to receive data. When DIR is valid (HIGH), data present at D₀ to D₈ can be shifted-in using the SI control input. With SI = HIGH, data is shifted into the input stage and a busy indication is given by DIR going LOW.

The data remains at the first location in the FIFO until SI is set to LOW. With SI = LOW data moves through the FIFO to the output stage, or to the last empty location. If the FIFO is not full after the SI pulse, DIR again becomes valid (HIGH) to indicate that space is available in the FIFO. The DIR flag remains LOW if the FIFO is full (see Fig. 6). The SI pulse must be made LOW in order to complete the shift-in process.

With the FIFO full, SI can be held HIGH until a shift-out (SO) pulse occurs. Then, following a shift-out of data, an empty location appears at the FIFO input and DIR goes HIGH to allow the next data to be shifted-in. This remains at the first FIFO location until SI again goes LOW (see Fig. 7).

Data transfer

After data has been transferred from the input stage of the FIFO following SI = LOW, data moves through the FIFO asynchronously and is stacked at the output end of the register. Empty locations appear at the input end of the FIFO as data moves through the device.

Data output

The data-out-ready flag (DOR = HIGH) indicates that there is valid data at the output (O_0 to O_0). The initial master-reset at power-on (MR = LOW) sets DOR to LOW (see Fig. 8). After MR = HIGH, data shifted into the FIFO moves through to the output stage causing DOR to go HIGH.

As the DOR flag goes HIGH, data can be shifted-out using the \overline{SO} control input. With \overline{SO} = HIGH, data in the output stage is shifted out and a busy indication is given by DOR going LOW. When \overline{SO} is made LOW, data moves through the FIFO to fill the output stage and an empty location appears at the input stage. When the output stage is filled DOR goes HIGH, but if the last of the valid data has been shifted out leaving the FIFO empty the DOR flag remains LOW (see Fig. 9). With the FIFO empty, the last word that was shifted-out is latched at the output Q_0 to Q_8 .

With the FIFO empty, the \overline{SO} input can be held HIGH until the SI control input is used. Following an SI pulse, data moves through the FIFO to the output stage, resulting in the DOR flag pulsing HIGH and a shift-out of data occurring. The \overline{SO} control must be made LOW before additional data can be shifted out (see Fig. 10).

High-speed burst mode

If it is assumed that the shift-in/shift-out pulses are not applied until the respective status flags are valid, it follows that the shift-in/shift-out rates are determined by the status flags. However, without the status flags a high-speed burst mode can be implemented. In this mode, the burst-in/burst-out rates are determined by the pulse widths of the shift-in/shift-out inputs and burst rates of 35 MHz can be obtained. Shift pulses can be applied without regard to the status flags but shift-in pulses that would overflow the storage capacity of the FIFO are not allowed (see Figs 11 and 12).

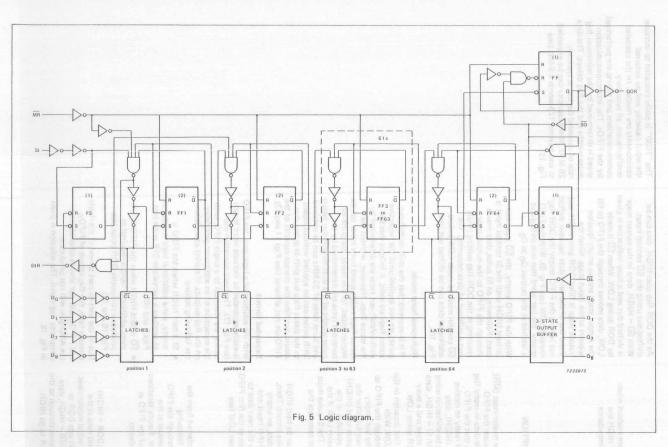
Expanded format

With the addition of a logic gate, the FIFO is easily expanded to increase word length (see Fig. 17). The basic operation and timing are identical to a single FIFO, with the exception of an additional gate delay on the flag outputs. If during application, the following occurs:

- SI is held HIGH when the FIFO is empty, some additional logic is required to produce a composite DIR pulse (see Figs 7 and 18).
- SO is held HIGH when the FIFO is full, some additional logic is required to produce a composite DOR pulse (see Figs 10 and 18).

Due to the part-to-part spread of the ripple through time, the flag signals of ${\sf FIFO}_{\sf A}$ and ${\sf FIFO}_{\sf B}$ will not always coincide and the AND-gate will not produce a composite flag signal. The solution is given in Fig. 18.

The "7030" is easily cascaded to increase the word capacity and no external components are needed. In the cascaded configuration, all necessary communications and timing are performed by the FIFOs. The intercommunication speed is determined by the minimum flag pulse widths and the flag delays. The data rate of cascaded devices is typically 25 MHz. Word-capacity can be expanded to and beyond 128-words x 9-bits (see Fig. 19).



Notes to Fig. 5 (see control flip-flops)

- 1. LOW on S input of flip-flops FS, FB and FP will set Q output to HIGH independent of state on R input.
 2. LOW on R input to FF1 to FF64 will set Q output to LOW independent of state on S input.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: LSI

AC CHARACTERISTICS FOR 74HC

	2.0 1.5 Fig. 7	20		8 8	Tamb			TEST CONDITIONS			
	0.3	8			74H	C					
SYMBOL	PARAMETER 0.5	A	+25		-40	to +85	-40 to +125		UNIT	V _{CC}	WAVEFORMS
	2.0	min.	typ.	max.	min.	max.	min.	max.			
tPHL/	propagation delay MR to DIR, DOR		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 8
t _{PHL} /	propagation delay SI to DIR		77 28 22	235 47 40	2	295 59 50	20	355 71 60	ns	2.0 4.5 6.0	Fig. 6
tPHL/	propagation delay SO to DOR		102 37 30	315 63 54		395 79 67	10	475 95 81	ns	2.0 4.5 6.0	Fig. 9
t _{PHL} /	propagation delay DOR to Q _n		11 4 3	35 7 6		45 9 8	88	55 11 9	ns	2.0 4.5 6.0	Fig. 10
t _{PHL} /	propagation delay SO to Q _n		113 41 33	345 69 59		430 86 73	8	520 104 88	ns	2.0 4.5 6.0	Fig. 14
^t PLH	propagation delay/ripple through delay SI to DOR		2.5 0.9 0.7	8.0 1.6 1.3		10 2.0 1.6	8	12 2.4 1.9	μs	2.0 4.5 6.0	Fig. 10
^t PLH	propagation delay/ bubble-up delay SO to DIR		3.3 1.2 1.0	10.0 2.0 1.6		12 2.5 2.0	8 74	15 3.0 2.4	μs	2.0 4.5 6.0	Fig. 7
^t PZH [/]	3-state output enable OE to Qn	peds A	52 19 15	175 35 30	R , "tagii	220 44 37	srio viii	265 53 45	ns (OH) 191	2.0 4.5 6.0	Fig. 16
^t PHZ [/]	3-state output disable OE to Q _n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 16 (2.1 2/1009450)
^t THL [/] ^t TLH	output transition time	ne fan Ine tel	19 7 6	75 15 13	oad of	95 19 16	of (55	110 22 19	ns	2.0 4.5 6.0	Fig. 14 Table to sulsy 9
tw	SI pulse width HIGH or LOW	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 6
tw	SO pulse width HIGH or LOW	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9 8 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

AC CHARACTERISTICS FOR 74HC

	Panoitabili	BCS VIII			T _{amb} (°C)		iet SOM	DH" 1636	TEST CONDITIONS			
SYMBOL	PARAMETER				74H	С	UNIT	Van	MANAGEO PAGE				
	PARAMETER	+25			-40	to +85	-40 to +125		TINIO	V _{CC}	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.	90	15 × 19	in 3 = 17 = 27 (V 0 = 0)		
t _W 2401	DIR pulse width HIGH	10 5 4	47 17 14	145 29 25	8 4 3	180 36 31	8 4 3	220 44 38	ns	2.0 4.5 6.0	Fig. 7		
tw	DOR pulse width HIGH	10 5 4	47 17 14	145 29 25	8 4 3	180 36 31	8 4 3	220 44 38	ns	2.0 4.5 6.0	Fig. 10		
t _W	MR pulse width	70 14 12	22 8 6	in sa	90 18 15	0	105 21 18	8	ns	2.0 4.5 6.0	Fig. 8		
^t rem	removal time MR to SI	80 16 14	24 8 7	ê	100 20 17	100	120 24 20	7	ns	2.0 4.5 6.0	Fig. 15		
^t su	set-up time D _n to SI	-35 -7 -6	-36 -13 -10	3	-45 -9 -8	8	-55 -11 -9	4	ns	2.0 4.5 6.0	Fig. 13		
^t h	hold time D _n to SI	135 27 23	44 16 13		170 34 29		205 41 35	E	ns	2.0 4.5 6.0	Fig. 13		
f _{max}	maximum clock pulse frequency SI, SO burst mode	20	9.9 30 36	0	2.8 14 16	Ö	2.4 12 14	6 1	MHz	2.0 4.5 6.0	Figs 11 and 12		
f _{max}	maximum clock pulse frequency SI, SO using flags	15	9.9 30 36		2.8 14 16		2.4 12 14	2	MHz	2.0 4.5 6.0	Figs 6 and 9		
f _{max}	maximum clock pulse frequency SI, SO cascaded	8	7.6 23 27		2.2 11 13	0	1.8 9.2 11	8	MHz	2.0 4.5 6.0	Figs 6 and 9		

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: LSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT							
OE	1.00							
SI	1.50							
Dn	0.75							
MR	1.50							
SO	1.50							

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V: t_r = t_f = 6 \text{ ns: } C_1 = 50 \text{ pF}$

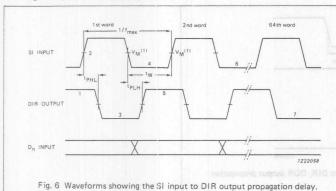
SYMBOL	PARAMETER V			-	T _{amb} (°C)		TEST CONDITIONS			
		125	+ 01 0	L Tas	74HC	Т	UNIT	8	MBOL PARAMETE		
		+25			-40	to +85	-40 to +125		UNII	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		etun de	maximum ch
tPHL/ tPLH	propagation delay MR to DIR, DOR		30	51		53		63	ns	4.5	Fig. 8
tPHL/ tPLH	propagation delay SI to DIR		29	49		61	į.	74	ns	4.5	Fig. 6
t _{PHL} /	propagation delay SO to DOR		39	67		84		101	ns	4.5	Fig. 9
^t PHL [/] ^t PLH	propagation delay SO to Q _n		46	78		98		117	ns	4.5	Fig. 14
^t PHL [/]	propagation delay DOR to Q _n		7	12		15		18	ns	4.5	Fig. 10
^t PLH	propagation delay/ripple through delay SI to DOR		0.9	1.6		2.0		2.4	μs	4.5	Fig. 10
^t PLH	propagation delay/ bubble-up delay SO to DIR		1.2	2.0		2.5		3.0	μs	4.5	Fig. 7
tPZH/	3-state output enable OE to Q _n		20	35		44		53	ns	4.5	Fig. 16
^t PHZ/ ^t PLZ	3-state output disable OE to Ω _n		19	35		44		53	ns	4.5	Fig. 16
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 14
tw	SI pulse width HIGH or LOW	12	6		15		18		ns	4.5	Fig. 6
tW	SO pulse width HIGH or LOW	15	9		19		22		ns	4.5	Fig. 9
tw	DIR pulse width HIGH	7.	22	37	6	46	6	56	ns	4.5	Fig. 7
tw	DOR pulse width HIGH	6	20	35	5	44	5	53	ns	4.5	Fig. 10
tw	MR pulse width LOW	18	10		23		27		ns	4.5	Fig. 8
t _{rem}	removal time MR to SI	18	10		23		27		ns	4.5	Fig. 15
^t su	set-up time D _n to SI	-5	-16		-4		-4		ns	4.5	Fig. 13
h	hold time D _n to SI	30	18		38		45		ns	4.5	Fig. 13

AC CHARACTERISTICS FOR 74HCT

							Tamb	°C)		TEST CONDITIONS					
SYMBOL	LEST CONDIT					74HC	т								
		PARAMETE	20V	THE		+25		-40	to +85	-40) to +1	25	UNIT	V _{CC}	WAVEFORMS
				min.	typ.	max.	min.	max.	min	. m	ax.				
^f max	maximum clo frequency SI, SO bur		an	15	26	(17) .36	12	-X	10	982 98	nier	MHz	4.5	Figs 11 and 12	UHS
f _{max}	maximum clock pulse frequency SI, SO using flags maximum clock pulse frequency SI, SO cascaded		an an	15	26		12		10	29		MHz	4.5	Figs 6 and 9	H7 _k
^f max			20	13	22		10		8.6	6		MHz	4.5	Figs 6 and 9	AHE/
													propagation delay DOR to Q ₀ DOR to Q ₀ propagation delay/rigple through delay St to DOR		

AC WAVEFORMS

Shifting in sequence FIFO empty to FIFO full



The SI pulse width and SI maximum pulse frequency.

Notes to Fig. 6

- 1. DIR initially HIGH; FIFO is prepared for valid data.
- 2. SI set HIGH; data loaded into input stage.
- 3. DIR drops LOW, input stage "busy"
- 4. SI set LOW; data from first location "ripple through".
- 5. DIR goes HIGH, status flag indicates FIFO prepared for additional data.
- 6. Repeat process to load 2nd word through to 64th word into FIFO.
- 7. DIR remains LOW; with attempt to shift into full FIFO, no data transfer occurs.

With FIFO full; SI held HIGH in anticipation of empty location

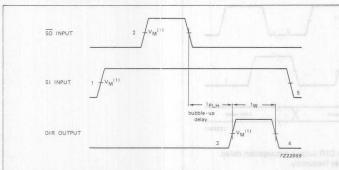


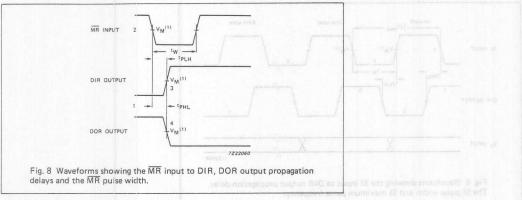
Fig. 7 Waveforms showing bubble-up delay, $\overline{\text{SO}}$ input to DIR output and DIR output pulse width.

Notes to Fig. 7

- 1. FIFO is initially full, shift-in is held HIGH.
- 2. SO pulse; data in the output stage is unloaded, "bubble-up process of empty locations begins".
- 3. DIR HIGH; when empty location reached input stage, flag indicates FIFO is prepared for data input.
- 4. DIR returns to LOW; FIFO is full again.
- 5. SI brought LOW; necessary to complete shift-in process, DIR remains LOW, because FIFO is full.

AC WAVEFORMS

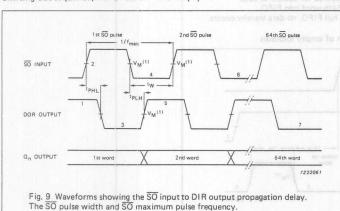
Master reset applied with FIFO full



Notes to Fig. 8

- 1. DIR LOW, output ready HIGH; assume FIFO is full. 2. $\overline{\rm MR}$ pulse LOW; clears FIFO.
- 3. DIR goes HIGH; flag indicates input prepared for valid data.
- 4. DOR drops LOW; flag indicates FIFO empty.

Shifting out sequence; FIFO full to FIFO empty



Notes to Fig. 9

- 1. DOR HIGH; no data transfer in progress, valid data is present at output stage.
- 2. SO set HIGH; results in DOR going LOW.
- 3. DOR drops LOW; output stage "busy"
- 4. SO is set LOW; data in the input stage is unloaded, and new data replaces it as empty location "bubbles-up" to input stage.
- 5. DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay.
- 6. Repeat process to unload the 3rd through to the 64th word from FIFO.
- 7. DOR remains LOW; FIFO is empty.

With FIFO empty; SO is held HIGH in anticipation

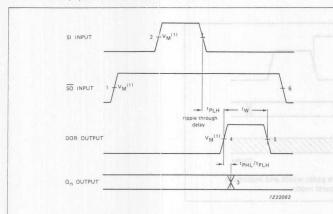


Fig. 10 Waveforms showing ripple through delay SI input to DOR output, DOR output pulse width and propagation delay from the DOR pulse to the Q_n output.

Notes to Fig. 10

- 1. FIFO is initially empty, \$\overline{SO}\$ is held HIGH.
 2. SI pulse; loads data into FIFO and initiates ripple through process.
- 3. DOR flag signals the arrival of valid data at the output stage.
- 4. Output transition; data arrives at output stage after the specified propagation delay between the rising edge of the DOR pulse to the Q_n output.
- 5. DOR goes LOW; FIFO is empty again.
- 6. SO set LOW; necessary to complete shift-out process. DOR remains LOW, because FJFO is empty.

Shift-in operation; high-speed burst mode

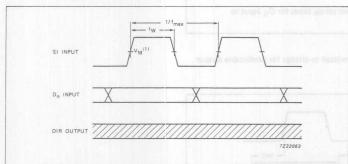
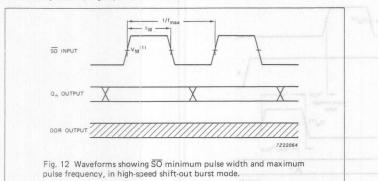


Fig. 11 Waveforms showing SI minimum pulse width and SI maximum pulse frequency, in high-speed shift-in burst mode.

Note to Fig. 11

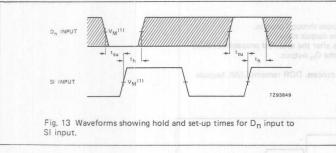
In the high-speed mode, the burst-in rate is determined by the minimum shift-in HIGH and shift-in LOW specifications. The DIR status flag is a don't care condition, and a shift-in pulse can be applied regardless of the flag. A SI pulse which would overflow the storage capacity of the FIFO is ignored.

Shift-out operation; high-speed burst mode



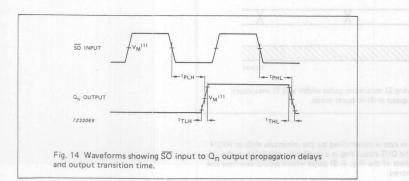
Note to Fig. 12

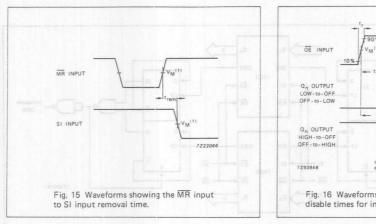
In the high-speed mode, the burst-out rate is determined by the minimum shift-out HIGH and shift-out LOW specifications. The DOR flag is a don't care condition and a $\overline{\text{SO}}$ pulse can be applied without regard to the flag.



Note to Fig. 13

The shaded areas indicate when the input is permitted to change for predictable output performance.





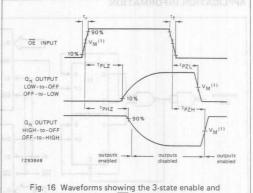
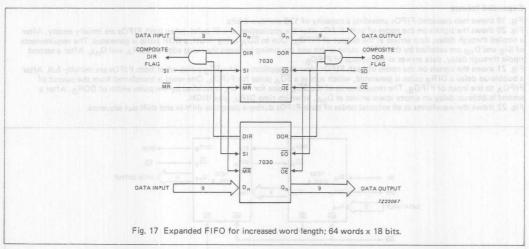


Fig. 16 Waveforms showing the 3-state enable and disable times for input $\overline{\text{OE}}$.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}. HCT: $V_M = 1.3 V$; $V_I = GND$ to 3 V.

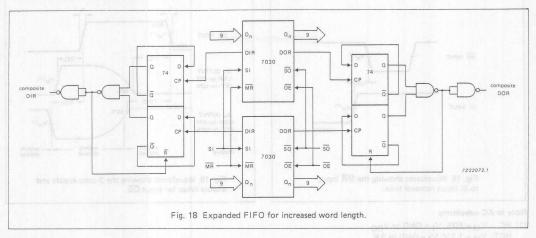
APPLICATION INFORMATION



Note to Fig. 17

The PC74HC/HCT7030 is easily expanded to increase word length. Composite DIR and DOR flags are formed with the addition of an AND gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.

APPLICATION INFORMATION



Note to Fig. 18

This circuit is only required if the SI input is constantly held HIGH, when the FIFO is empty and the automatic shift-in cycles are started or if \overline{SO} output is constantly held HIGH, when the FIFO is full and the automatic shift-out cycles are started (see Figs 7 and 10).

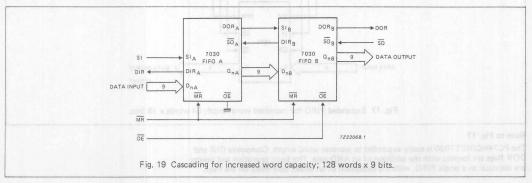
Expanded format

Fig. 19 shows two cascaded FIFOs providing a capacity of 128 words x 9 bits.

Fig. 20 shows the signals on the nodes of both FIFOs after the application of a SI pulse, when both FIFOs are intially empty. After a rippled through delay, data arrives at the output of FIFO $_A$. Due to \overline{SO}_A being HIGH, a DOR pulse is generated. The requirements of SIB and D_{nB} are satisfied by the DOR $_A$ pulse width and the timing between the rising edge of DOR $_A$ and Q_{nA} . After a second ripple through delay, data arrives at the output of FIFO $_B$.

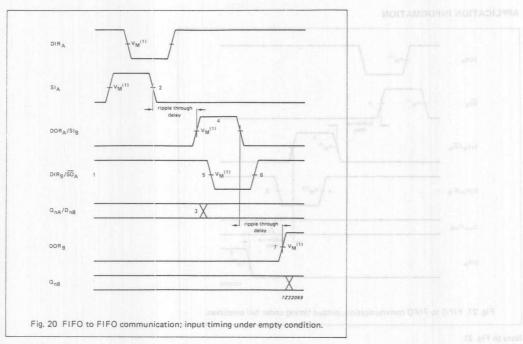
Fig. 21 shows the signals on the nodes of both FIFOs after the application of a \overline{SO}_B pulse, when both FIFOs are initially full. After a bubble-up delay a DIR_B pulse is generated, which acts as a \overline{SO}_A pulse for FIFO_A. One word is transferred from the output of FIFO_A to the input of FIFO_B. The requirements of the \overline{SO}_A pulse for FIFO_A is satisfied by the pulse width of DOR_B. After a second bubble-up delay an empty space arrives at D_{nA} , at which time DIR_A goes HIGH.

Fig. 22 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.



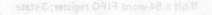
Note to Fig. 19

The PC74HC/HCT7030 is easily cascaded to increase word capacity without any external circuitry. In cascaded format, all necessary communications are handled by the FIFOs. Figs 17 to 19 demonstrate the intercommunication timing between FIFO $_{\rm A}$ and FIFO $_{\rm B}$. Fig. 22 gives an overview of pulses and timing of two cascaded FIFOs, when shifted full and shifted empty again.

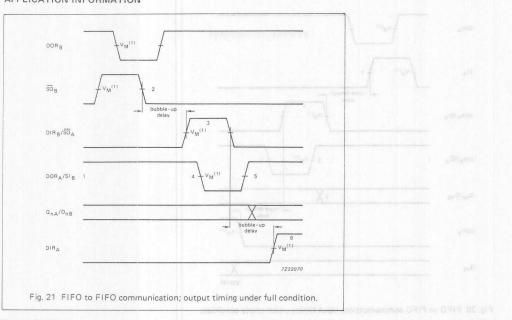


Notes to Fig. 20

- FIFO_A and FIFO_B initially empty, SO_A held HIGH in anticipation of data.
 Load one word into FIFO_A; SI pulse applied, results in DIR pulse.
 Data out _A/data in _B transition; valid data arrives at FIFO_A output stage after a specified delay of the DOR flag, meeting data input set-up requirements of FIFO_B.
 DOR_A and SI_B pulse HIGH; (ripple through delay after SI_A LOW) data is unloaded
- DOAQ and SIB bulse in IGAT, (Inject Infough easy after SIA Low) data is unloaded from FIFO_A as a result of the data output ready pulse, data is shifted into FIFO_B.
 DIRB and SO_A go LOW; flag indicates input stage of FIFO_B is busy, shift-out of FIFO_A is complete.
 DIRB and SO_A go HIGH automatically; the input stage of FIFO_B is again able to receive data, SO is held HIGH in anticipation of additional data.
- DORB goes HIGH; (ripple through delay after SIB LOW) valid data is present one propagation delay later at the FIFOB output stage.







Note to Fig. 21

- 1. FIFOA and FIFOB initially full, SIB held HIGH in anticipation of shifting in new

- data as empty location bubbles-up.

 2. Unload one word from FIFOB; \$\overline{SO}\$ pulse applied, results in DOR pulse,

 3. DIRB and \$\overline{SO}\$A pulse HIGH; (bubble-up delay after \$\overline{SO}\$B LOW) data is loaded into FIFOB as a result of the DIR pulse, data is shifted out of FIFOA.

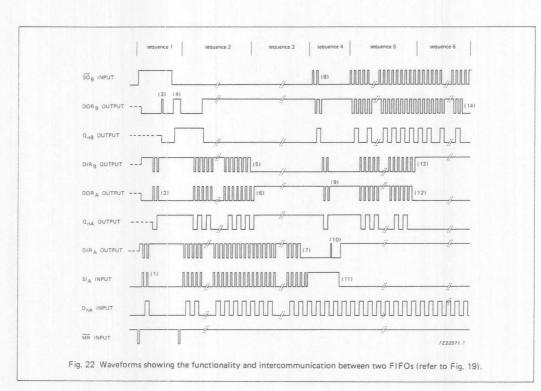
 4. DORA and \$\overline{SO}\$B LOW; flag indicates the output stage of FIFOA is sourced.
- to FIFOB is complete.

 5. DORA and SIB go HIGH; flag indicates valid data is again available at FIFOA output stage, SIB is held HIGH, awaiting bubble-up of empty location.

 6. DIRA goes HIGH; (bubble-up delay after SOA LOW) an empty location is present at

Note to application waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.



Note to Fig. 22

Sequence 1 (Both FIFOs empty, starting shift-in process):

After a MR pulse has been applied FIFO $_{\rm A}$ and FIFO $_{\rm B}$ are empty. The DOR flags of FIFO $_{\rm A}$ and FIFO $_{\rm B}$ go LOW due to no valid data being present at the outputs. The DIR flags are set HIGH due to the FIFOs being ready to accept data. SO $_{\rm B}$ is held HIGH and two SIA pulses are applied (1). These pulses allow two data words to ripple through to the output stage of FIFO $_{\rm A}$ and to the input stage of FIFO $_{\rm B}$ (2). When data arrives at the output of FIFO $_{\rm B}$, a DOR $_{\rm B}$ pulse is generated (3). When SO $_{\rm B}$ goes LOW, the first bit is shifted out and a second bit ripples through to the output after which DOR $_{\rm B}$ goes HIGH (4).

Sequence 2 (FIFOB runs full):

After the $\overline{\text{MR}}$ pulse, a series of 64 SI pulses are applied. When 64 words are shifted in, DIRB remains LOW due to FIFOB being full (5). DORA goes LOW due to FIFOB being empty.

Sequence 3 (FIFOA runs full):

When 65 words are shifted in, DORA remains HIGH due to valid data remaining at the output of FIFOA. QnA remains HIGH, being the polarity of the 65th data word (6). After the 128th SI pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

Sequence 4 (Both FIFOs full, starting shift-out process):

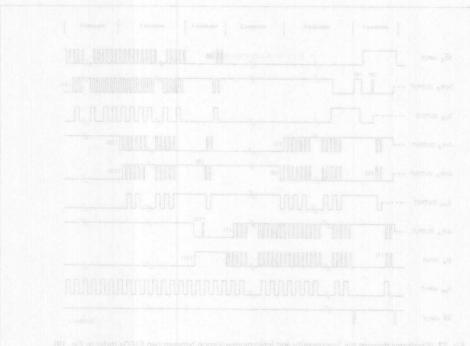
 SI_A is held HIGH and two \overline{SO}_B pulses are applied (8). These pulses shift out two words and thus allow two empty locations to bubble-up to the input stage of $FIFO_B$, and proceed to $FIFO_A$ (9). When the first empty location arrives at the input of $FIFO_A$, a DIR A pulse is generated (10) and a new word is shifted into $FIFO_A$. SI_A is made LOW and now the second empty location reaches the input stage of $FIFO_A$, after which DIR_A remains HIGH (11).

Sequence 5 (FIFOA runs empty):

At the start of sequence 5 FIFO_A contains 63 valid words due to two words being shifted out and one word being shifted in in sequence 4. An additional series of \overline{SO}_B pulses are applied. After 63 \overline{SO}_B pulses, all words from FIFO_A are shifted into FIFO_B. DOR_A remains LOW (12).

Sequence 6 (FIFOB runs empty):

After the next \overline{SO}_B pulse, DIRB remains HIGH due to the input stage of FIFOB being empty (13). After another 63 \overline{SO}_B pulses, DORB remains LOW due to both FIFOs being empty (14). Additional \overline{SO}_B pulses have no effect. The last word remains available at the output Q_D .



The state of the s

Note to Fig. 22

Sequence 1 (Both F1FOs empsy, starting shift-in process)

After a MR pulse has been applied FIFO_A and FIFO_B are empty. The DOR Hags of FIFO_A and FIFO_B go'LOW due to no valid data being present as the outputs. The DIR Hags are at HIGH due to the FIFO being ready to adopt data SGg is hald filled and two SIs pulses allow awards to ripple through to the output stage of FIFO_B and to the input of a FIFO_B and to the input of AFIFO_B and to the input of AFIFO_B and to the first bit is shifted out and a second bit hipples through to the output after which DORS, goes HIGH (A).

Sequence 2 (FIFOg ning full

After the MR pulse, a series of 64 St pulses are applied. When 64 words are shifted In, DIRg remains LOW due to FJFOg being to ISD DORA loos LOW due to FIFOA being empty.

(Unit and a OFIF) & somoupal

When 05 words are shifted in, 00R A remains HIGH due to valid data remaining at the output of PIFOA, 0_{RA} remains HIGH, being the polarity of the 6c; it due word (6). After the 128th SI ouise, DIR remains COW and both FIFOs are full (7). Additional pulses there is a state of the control of

Sequence 4 (Both FIFOs full, starting shift out proces

SIA is field titGH and two SOg outsize are soplied (8). These pulses with out two words set that allow but empty locations to be bubble up to the input stage of FIFGg, and necessed to FIFG (8). When the first empty location entires at the input of FIFGg, and an every word is the that the FIFG A. SIA is made LOW and new time second among the second among the input location reaches the input stage of FIFGA, when which DIA camera and IAM.

demo suns Aunta) de ausupes

At the san or sequence 6 REDA, containt 33 valid words are to two words being shifted out and one word being shifted to the acquence A. An additional series of SDg pales, where 23 SDg pulse, all words from PECQ are shifted into PEPCQ.

OOR, remains LOW (12).

sourced & (FIFOe nate

Fuer the next SOg pulse, DIRB remains HIGH due to the input stage of FIFIng being smort (13). After another 63 SOg pulses, ORB remains LOW due to both FIFDs traing smort (14). Additional SOg pulses have do affect. This last word remains shalloule at security Co.

PHASE-LOCKED-LOOP WITH LOCK DETECTOR

FEATURES

- Low power consumption
- Centre frequency up to 17 MHz (typ.) at $V_{CC} = 4.5 \text{ V}$
- Choice of two phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop;
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operation power supply voltage range: VCO section 3.0 to 6.0 V
- digital section 2.0 to 6.0 V Zero voltage offset due to op-amp buffering
- Output capability: standard
- ICC category: MSI

OV/MPOI	DADAMETED	CONDITIONS	TYI	UNIT		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT	
f _o	VCO centre frequency	C1 = 40 pF R1 = 3 kΩ VCC = 5 V	19	19	MHz	
CI	input capacitance (pin 5)	OV TUO	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per package	notes 1 and 2	24	24	pF a	

GND = 0 V; Tamb = 25 °C

PACKAGE OUTLINES

- 1. Applies to the phase comparator section only (VCO disabled). For power dissipation of VCO and demodulator sections see Figs 20, 21 and 22.
- 2. CpD is used to determine the dynamic power dissipation (PD in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_0)$$
 where:

- f; = input frequency in MHz
 - = output frequency in MHz
- CL = output load capacitance in pF V_{CC} = supply voltage in V
- f_0 = output frequency in Birst Σ (C_L x V_{CC}² x f_0) = sum of outputs

16-lead DIL; plastic (SOT38CP). 16-lead mini-pack; plastic (SO16; SOT109 A).

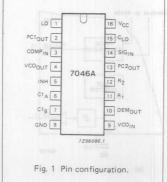
GENERAL DESCRIPTION

The 74HC/HCT7046 are high-speed Si-gate CMOS devices and are specified in compliance with JEDEC standard no. 7.

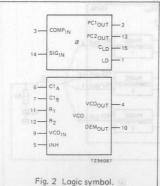
The 74HC/HCT7046 are phase-locked-loop circuits that comprise a linear voltagecontrolled oscillator (VCO) and two different phase comparators (PC1 and PC2) with a common signal input amplifier and a common comparator input.

A lock detector is provided and this gives a HIGH level at pin 1 (LD) when the PLL is locked. The lock detector capacitor must be connected between pin 15 (CLD)

(continued on next page) 16 VCC 15 CLD PC1OUT 2



and pin 8 (GND). The value of the CLD capacitor can be determined, using information supplied in Fig. 32 The input signal can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "7046" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.



APPLICATIONS

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control



PHASE-LOCKED-LOOP WITH LOCK DETECTOR

PIN DESCRIPTION

PIN NO.		SYMBOL	NAME AND FUNCTION
1 2 3	19	PC1 _{OUT}	lock detector output (active HIGH) phase comparator 1 output
4 4 4 5		VCO _{OUT}	VCO output
6 3 9		C1 _A S bns i am	capacitor C1 connection A capacitor C1 connection B
8		GND	ground (0 V) 0° 85 = gmsT (V 0 = QND
9		VCO _{IN} DEMOUT	VCO input demodulator output
11 25 60		R ₁ as annitos y	resistor R1 connection resistor R2 connection
13 14 - 14		PC2 _{OUT}	signal input
15 16		CFD or Alddon = 2	lock detector capacitor input positive supply voltage

GENERAL DESCRIPTION VCO

The VCO requires one external capacitor C1 (between C1 $_{\rm A}$ and C1 $_{\rm B}$) and one external resistor R1 (between R1 and GND) or two external resistors R1 and R2 (between R1 and GND, and R2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of

resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEMOUT). In contrast to conventional techniques where the DEMOUT voltage is one threshold voltage lower than the VCO input voltage, here the DEMOUT voltage equals that of the VCO input. If DEMOUT is used, a load resistor (Rs) should be connected from DEMOUT to GND; if unused, DEMOUT should be left open. The VCO output (VCOOUT) can be connected directly to the comparator input (COMP_IN), or connected via a frequency-divider. The

VCO output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

The only difference between the HC and HCT versions is the input level specification of the INH input. This input disables the VCO section. The comparators' sections are identical, so that there is no difference in the ${\rm SIG_{IN}}$ (pin 14) or COMP $_{\rm IN}$ (pin 3) inputs between the HC and HCT versions.

Phase comparators

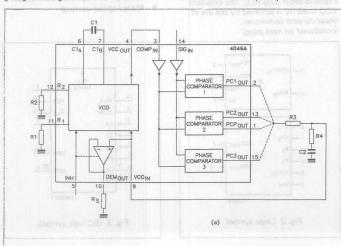
The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

Phase comparator 1 (PC1)

This is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple $(f_r = 2f_i)$ is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{\pi} (\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;
V_{DEMOUT} = V_{PC1OUT} (via low-pass



identical to 4046A

7046A

7046A

7046A

PHASE
COMPARATOR
PC2-OUT 13

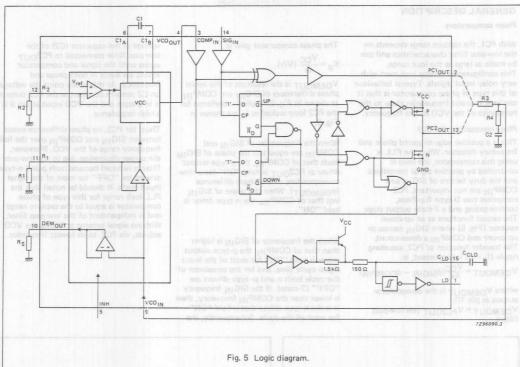
LOCK
DETECTOR

15

CLD
15

CCLD
9CA129

Fig. 4 Functional diagram.



The phase comparator gain is:

$$K_p = \frac{V_{CC}}{\pi} (V/r).$$

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (VDEMOUT), is the resultant of the phase differences of signals (SIG_IN) and the comparator input (COMP_IN) as shown in Fig. 6. The average of VDEMOUT is equal to 1/2 VCC when there is no signal or noise at SIG_IN and with this input the VCO oscillates at the centre frequency (f_o). Typical waveforms for the PC1 loop locked at f_o are shown in Fig. 7.

The frequency capture range $(2f_{\rm c})$ is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range $(2f_{\rm L})$ is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

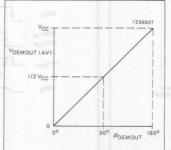


Fig. 6 Phase comparator 1: average output voltage versus input phase difference:

VDEMOUT = VPC1OUT = $\frac{\text{VCC}}{\pi} (\phi \text{SIGIN} - \phi \text{COMPIN})$ $\phi \text{DEMOUT} = (\phi \text{SIGIN} - \phi \text{COMPIN}).$

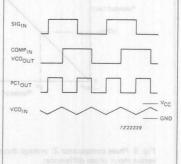


Fig. 7 Typical waveforms for PLL using phase comparator 1, loop locked at $f_{\rm O}$.

GENERAL DESCRIPTION

Phase comparators

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration retains lock even with very noisy input signals. Typical behaviour of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

Phase comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and COMP_{IN} are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig. 5) where SIG_{IN} causes an up-count and COMP_{IN} a down-count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{4\pi} (\phi_{SIGIN} - \phi_{COMPIN})$$

where VDEMOUT is the demodulator output at pin 10;

VDEMOUT = VPC2OUT (via low-pass filter).

The phase comparator gain is:

$$K_p = \frac{V_{CC}}{4\pi} (V/r).$$

 $V_{\mbox{\footnotesize DEMOUT}}$ is the resultant of the initial phase differences of ${\rm SIG}_{1N}$ and ${\rm COMP}_{1N}$ as shown in Fig. 8. Typical waveforms for the PC2 loop locked at ${\rm f}_0$ are shown in Fig. 9.

When the frequencies of SIG_{IN} and COMP_{IN} are equal but the phase of SIG_{IN} leads that of COMP_{IN}, the p-type output driver at PC2_{OLT} is held "ON" for a time corresponding to the phase difference (ϕ_{DEMOUT}). When the phase of SIG_{IN} lags that of COMP_{IN}, the n-type driver is held "ON".

When the frequency of SIG_{1N} is higher than that of $COMP_{1N}$, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n and p- type drivers are "OFF" (3-state). If the SIG_{1N} frequency is lower than the $COMP_{1N}$ frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the

voltage at the capacitor (C2) of the low-pass filter connected to PC2_{OUT} varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance.

Thus, for PC2, no phase difference exists between SIGIN and COMPIN over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIGIN the VCO adjusts, via PC2, to its lowest frequency.

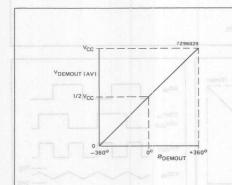


Fig. 8 Phase comparator 2: average output voltage versus input phase difference:

VDEMOUT = VPC2OUT =

 $\frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

 ϕ DEMOUT = $(\phi$ SIGIN - ϕ COMPIN)

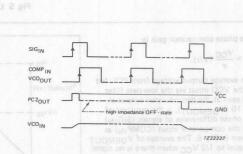


Fig. 9 Typical waveforms for PLL using phase comparator 2, loop locked at f_0 .

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

			74HC			74HC1	г	UNIT	CONDITIONS	
SYMBOL	PARAMETER	min.	typ.	max.	min.	typ.	max.	GMD ex	page of the conditions	
VCC EMON	DC supply voltage	3.0	5.0	6.0	4.5	5.0	5.5	V		
Vcc	DC supply voltage if VCO section is not used	2.0	5.0	6.0	4.5	5.0	5.5	٧	SAMBOL CARAM	
VI	DC input voltage range	0	07 00	Vcc	0		Vcc	٧		
V _O	DC output voltage range	0	FIR .CI	VCC	0	mim	VCC	V		
Tamb	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC	
Tamb	operating ambient temperature range	-40	28	+125	-40		+125	°C	CHARACTERISTICS	
t _r , t _f	input rise and fall times (pin 5)		6.0	1000 500 400		6.0	500	ns	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	

RATINGS TO TRAIT

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS	
Vcc	DC supply voltage	-0.5	+7	V	OC coupled 1.5 1.2	
±11K	DC input diode current	2	20	mA	for $V_1 < -0.5 \text{ V or } V_1 > V_{CC} + 0.5 \text{ V}$	HIV
±10K	DC output diode current	6.0 Eli	20	mA	for $V_0 < -0.5 \text{ V}$ or $V_0 > V_{CC} + 0.5 \text{ V}$	нV
±IO	DC output source or sink current	1.8	25	mA	for -0.5 V < V _O < V _{CC} + 0.5 V	
±ICC; ±IGND	DC V _{CC} or GND current	\$.	50	mA	LD, PCnOUT S.6 6.0	HOV
T _{stg}	storage temperature range	- 65	+150	°C	HIGH level output voltage 3.88 4.32	
Am 5.8	power dissipation per package	5.		5.34	for temperature range: - 40 to +125 °C	110,
P _{tot}	plastic DIL	10	750	mW	74HC/HCT above +70 °C: derate linearly with 12 mW/K	
	plastic mini-pack (SO)	ro	500	mW	above +70 °C: derate linearly with 8 mW/K	104

pins 3, 5, and 14 at VCC;

pin 9 at GND; I₁ at pins 3 and 14 to be excluded

DC CHARACTERISTICS FOR 74HC

Quiescent supply current
Voltages are referenced to GND (ground = 0 V)

Tamb (°C)

SYMBOL PARAMETER

+25

-40 to +85

-40 to +125

V

TAMA A T

min. max.

80.0

160.0 µA

6.0

max.

8.0

min. typ.

Phase comparator section

ICC TO

Voltages are referenced to GND (ground = 0 V)

quiescent supply current (VCO disabled)

					T _{amb} (°C)				TEST CONDITIONS			
0)/44001				(AE)	74H	Systeio			UNIT		nstroo	OTHER	
SYMBOL	PARAMETER	+25			-40	to +85	-40 to +125		= bruo	V _{CC}	VI	ortages are referen	
		min.	typ.	max.	min.	max.	min.	max.		я	AMET	YMBOL PAR	
VIH	DC coupled HIGH level input voltage SIGIN, COMPIN	1.5 3.15 4.2	1.2 2.4 3.2	not	1.5 3.15 4.2	20	1.5 3.15 4.2		V	4.5		196 99 199 99	
VIL	DC coupled LOW level input voltage SIG _{IN} , COMP _{IN}	/ a.o.	0.8 2.1 2.8	0.5 1.35 1.8	Anı	0.5 1.35 1.8		0.5 1.35 1.8	v inam	2.0 4.5 6.0	utput o	OK DC	
V _{OH}	HIGH level output voltage LD, PC _{nOUT}	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9	08	1.9 4.4 5.9		V	2.0 4.5 6.0	VIH or VIL	$-1_{O} = 20 \mu A$ $-1_{O} = 20 \mu A$ $-1_{O} = 20 \mu A$	
V _{OH}	HIGH level output voltage	3.98 5.48	4.32 5.81	not	3.84 5.34	0814	3.7 5.2		vegnar V	4.5 6.0	V _{IH} or V _{IL}	-I _O = 4.0 mA -I _O = 5.2 mA	
VOL	LOW level output voltage LD, PCnOUT	°C; der	0 0	0.1 0.1 0.1	Wm	0.1 0.1 0.1		0.1 0.1 0.1	V (C	2.0 4.5 6.0	V _{IH} or V _{IL}	I _O = 20 μA I _O = 20 μA I _O = 20 μA	
VOL	LOW level output voltage LD, PC _{nOUT}		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	VIH or VIL	I _O = 4.0 mA I _O = 5.2 mA	
±Iı	input leakage current SIG _{IN} , COMP _{IN}			3.0 7.0 18.0 30.0		4.0 9.0 23.0 38.0		5.0 11.0 27.0 45.0	μΑ	2.0 3.0 4.5 6.0	V _{CC} or GND		
±1 _{OZ}	3-state OFF-state current PC2 _{OUT}			0.5		5.0		10.0	μА	6.0	V _{IH} or V _{IL}	V _O = V _{CC} or GND	
RI	input resistance SIG _{IN} , COMP _{IN}		800 250 150						kΩ	3.0 4.5 6.0	point;	elf-bias operating $\Delta V_1 = 0.5 V$; as 10, 11 and 12	

VCO section

Voltages are referenced to GND (ground = 0 V)

					T _{amb} (°C)			= bnuo	TEST CONDITIONS			
	TEST CONDITIE				74H	C			LIMIT	.,	.,	OTHER	
SYMBOL	PARAMETER		+25		-40	to +85	-40 to	+125	UNIT	V _{CC}	VI	OTHER	
	ASHTO DOV TH	min.	typ.	max.	min.	max.	min.	max.		P. Carlot	a i sinA	MAN JURINYS	
VIH	HIGH level input voltage INH	2.1 3.15 4.2	1.7 2.4 3.2	sem	2.1 3.15 4.2	ien x	2.1 3.15 4.2	min. 0	V	3.0 4.5 6.0			
VIL VOO	LOW level input voltage	0.4	1.3 2.1 2.8	0.9 1.35 1.8		0.9 1.35 1.8	30	0.9 1.35 1.8	V	3.0 4.5 6.0	periov t	nello gri	
Vон	HIGH level output voltage VCOOUT	2.9 4.4 5.9	3.0 4.5 6.0		2.9 4.4 5.9		2.9 4.4 5.9	2	V 70	3.0 4.5 6.0	VIH or VIL	- I _O = 20 μA - I _O = 20 μA - I _O = 20 μA	
V _{OH}	HIGH level output voltage VCOOUT	3.98 5.48			3.84 5.34		3.7 5.2	S	V	4.5 6.0	V _{IH} or V _{IL}	-I _O = 4.0 mA -I _O = 5.2 mA	
VOL	LOW level output voltage VCOOUT		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	3.0 4.5 6.0	V _{IH} or V _{IL}	I _O = 20 μA I _O = 20 μA I _O = 20 μA	
VOL	LOW level output voltage VCOOUT		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V _{IH} or V _{IL}	I _O = 4.0 mA I _O = 5.2 mA	
VoL	LOW level output voltage C1 _A , C1 _B (test purposes only)			0.40 0.40		0.47 0.47		0.54 0.54	V	4.5 6.0	V _{IH} or V _{IL}	I _O = 4.0 mA I _O = 5.2 mA	
±1 ₁	input leakage current INH, VCO _{IN}			0.1		1.0		1.0	μА	6.0	V _{CC} or GND		
R1	resistor range	3.0 3.0 3.0		300 300					kΩ	3.0 4.5 6.0		note 1	
R2	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1	
C1	capacitor range	40 40 40		no limit					pF	3.0 4.5 6.0			
VVCOIN	operating voltage range at VCO _{IN}	1.1 1.1 1.1		1.9 3.4 4.9					V	3.0 4.5 6.0		over the range specified for R1; for linearity see Figs 18 and 19.	

Note

^{1.} The parallel value of R1 and R2 should be more than 2.7 k Ω . Optimum performance is achieved when R1 and/or R2 are/is > 10 k Ω .

DC CHARACTERISTICS FOR 74HC

Dame	dulate	or section

Voltages are	referenced	to GND	(ground = 0 V)

				******				Tamb	(°C)						TEST CONDITIO	NS
	HTO			THIC	851	+010	1	74H	С				UNIT	V	OTHER	
SYMBOL	PAR	AMETE	К		250	+25	im a	-40	to +85	-40	to +1	25	UNIT	V _{CC}		
			3.0		min.	typ.	max.	min.	max.	min.	m	ax.	91		favel HD)H	14 61
RS	resis	tor range			50 50 50	0	300 300 300	8.0	3.1	8.0	3.8		kΩ	3.0 4.5 6.0	at R _S > 300 kΩ the leakage curr influence V _{DEN}	ent can
VOFF		et voltage O _{IN} to \	DEMOU	т	8	±30 ±20 ±10	2.8	8.1	2.8	8.1	2.8	6	mV	3.0 4.5 6.0	V _I = V _V COIN = values taken ove see Fig. 13	= 1/2 V _{CC} ; er R _S range
RD		amic outp	out t DEM _{OU}	т		25 25 25	5.8		5.5		0.8	80	Ω	3.0 4.5 6.0	VDEMOUT = 1	/2 V _{CC}
= 5.2 mA	ŏi-	JIV.	6.0	7			8.2	1	5.3		5.81	48	8		THOOSY	HU.
	speci for li															

AC CHARACTERISTICS FOR 74HC

Phase comparator section

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

SNOL	TEST CONDIT				Tamb (°C)					TEST CONDI	ITIONS
CVMPOL	DADAMETER				74H	9			LINUT		OTHER	
SYMBOL	PARAMETER	+25		- 85	-40 to +85		-40 to +125		UNIT	V _{CC}	OTHER	
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/	propagation delay SIG _{IN} , COMP _{IN} to PC1 _{OUT}	0.081	58 21 17	200 40 34	8	250 50 43	8	300 60 51	nsiaam	2.0 4.5 6.0	Fig. 14	
tPZH/	3-state output enable time SIG _{IN} , COMP _{IN} to PC2 _{OUT}	061	74 27 22	280 56 48		350 70 60	6 001	420 84 71	ns	2.0 4.5 6.0	Fig. 15	nnia
^t PHZ [/]	3-state output disable time SIG _{IN} , COMP _{IN} to PC2 _{OUT}		96 35 28	325 65 55		405 81 69		490 98 83	ns	2.0 4.5 6.0	Fig. 15	
t _{THL} /	output transition time	evods in thi	19 7 6	75 15 13	eol sine	13	ορίΔ) e by th	110 22 19	ns	2.0 4.5 6.0	Fig. 14	to teten To detent
V _{1(p-p)}	AC coupled input sensitivity (peak-to-peak value) at SIGIN or COMPIN		9 11 15 33						mV	2.0 3.0 4.5 6.0	f _i = 1 MHz	INPUT

VCO section

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)				TEST CONDITIONS		
0)///00/					74H	С			UNIT		OTHER	
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNII	V _{CC}	OTHER	
		min.	typ.	max.	typ.	max.	min.	max.				
Δf/T	frequency stability with temperature change				0.20 0.15 0.14				%/K	3.0 4.5 6.0	$V_1 = V_{VCOIN} = 1/2 V_{CC};$ $R1 = 100 \text{ k}\Omega; R2 = \infty;$ C1 = 100 pF; see Fig. 16	
fo	VCO centre frequency (duty factor = 50%)	3.0 11.0 13.0	10.0 17.0 21.0						MHz	3.0 4.5 6.0	$V_{VCOIN} = 1/2 V_{CC};$ $R1 = 3 k\Omega; R2 = \infty;$ C1 = 40 pF; see Fig. 17	
∆fvco	VCO frequency linearity		1.0 0.4 0.3						%	3.0 4.5 6.0	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 18 and 19	
δνςο	duty factor at VCO _{OUT}		50 50 50						%	3.0 4.5 6.0		

DC CHARACTERISTICS FOR 74HCT

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

	REST COMES				Tamb (°C)				TEST CONDITIONS			
SYMBOL	SENTO LOOV THEO	74HCT								, B	OTHER		
STINDOL PARAINETER	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC	OTHER		
		min.	typ.	max.	min.	max.	min.	max.					
¹ cc	quiescent supply current (VCO disabled)	300 60 61		8.0	4 0 4	80.0	2 B	160.0	μΑ	6.0	pins 3, 5 and 14 at V _{CI} pin 9 at GND; I _I at pin 3 and 14 to be exclude		
ΔICC	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) V ₁ = V _{CC} - 2.1 V	420 71 480 480	100	360	8	450	27 S 27 S 22 4 S 28 3	490	μΑ	4.5 to 5.5	pins 3 and 14 at V _{CC} ; pin 9 at GND; I ₁ at pin 3 and 14 to be exclude		

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given above. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
INH	1.00

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

						T _{amb} (°C)		IV 0	= briught	GMD (TEST C	ONDIT	IONS
SMOIT						74HC	т			UNIT	Vcc	Vı	отн	FR
SYMBOL	PARAMETE			+25		-40	to +85	-40 t	o +125	Olvii	V			
	ITO IV		min.	typ.	max.	min.	max.	min.	max.		R:	AMET	PAR	TORMAS
VIH	DC coupled HIGH level SIG _{IN} , CO	oltage	3.15	2.4	d 368	n ani	7 25	yp. n	tmim	V	4.5	levsi i	ЭН	
VIL	DC coupled LOW level	Itage		2.1	1.35	0.		Đ.	2.0	V	4.5	it velta	INI INI INI	BI
V _{OH}	HIGH level of LD, PC _{nOL}	oltage	4.4	4.5	8	4.4	8	4.4		V	4.5	V _{IH} or V _{IL}	-10	= 20 μΑ
VOH	HIGH level of LD, PCnOL	oltage	3.98	4.32		3.84	h	3.7	4,4	V	4.5	V _{IH} or V _{IL}	-10	= 4.0 mA
Am 0.4 = VOL	LOW level o	oltage		0	0.1	28.	0.1	.32	0.1	V	4.5	V _{IH} or V _{IL}	10 =	20 μΑ
V _{OL}	LOW level o	oltage	1.0	0.15	0.26	0	0.33	0	0.4	V	4.5	V _{IH} or V _{IL}	10 =	4.0 mA
Am 0,8 ±1 ₁	input leakag SIG _{IN} , CO	t	2.4		30	.0	38	o ar.	45	μА	5.5	V _{CC} or GND	DV	10/
±IOZ	3-state OFF-state PC2OUT	V	0.54		0.5	0	5.0	0	10.0	μА	5,5	VIH or VIL	VO = GND	= VCC or
RI	input resista SIG _{IN} , CO	Au	0.1	250	0			0	0.0	kΩ	4.5	point	; △V1 =	es operation 0.5 V; 11 and 12
the range fried for R1 ineurity see 18 and 19,														

DC CHARACTERISTICS FOR 74HCT

VCO section

Voltages are referenced to GND (ground = 0 V)

	UNIT VCC VI OTH				Tamb (°C)				511	TEST C	ONDITIONS	
	V	951	+ 07.02	- 39	74H0	ст	25.4		UNIT	\/	1	OTHER	
SYMBOL	PARAMETER	+25 -40 to +85 -40 to +125								V _{CC}	VI	OTHER	
	as v	min.	typ.	max.	min.	max.	min.	max.	l and the		palquo:	00	
VIH	HIGH level input voltage INH	2.0	1.6		2.0	35	2.0		V	4.5 to 5.5	ing, Cti coupled W level		
VIL Autos =	LOW level input voltage INH		1.2	0.8	35,	0.8	8,1	0.8	V	4.5 to 5.5	level H	DIH HOV	
Vон	HIGH level output voltage VCOOUT	4.4	4.5	E.	4.4		4.4	88.8	V	4.5	V _{IH} or V _{IL}	-1 _O = 20 μA	
Vон	HIGH level output voltage VCOOUT	3.98	4.32		3.84		3.7		V	4.5	VIH or VIL	-1 _O = 4.0 mA	
VOL	LOW level output voltage VCOOUT	3.6	0	0.1	0	0.1	0 38 0	0.1	V 900710	4.5	VIH or VIL	Ι _Ο = 20 μΑ	
VOL	LOW level output voltage VCOOUT	T di	0.15	0.26		0.33		0.4	V	4.5	VIH or VIL	I _O = 4.0 mA	
V _{OL}	LOW level output voltage C1 _A , C1 _B (test purposes only)	0.01		0.40	a la	0.47	0	0.54	V	4.5	VIH or VIL	I _O = 4.0 mA	
s operatifit 0.5 V;	input leakage current INH, VCO _{IN}			0.1		1.0	025	1.0	μΑ	5.5	V _{CC} or GND	egni ja	
R1	resistor range	3.0	1	300					kΩ	4.5	1911	note 1	
R2	resistor range	3.0		300					kΩ	4.5		note 1	
C1	capacitor range	40		no limit					pF	4.5			
VVCOIN	operating voltage range at VCOIN	1,1		3.4					V	4.5		over the range specified for R1; for linearity see Figs 18 and 19.	

Note

^{1.} The parallel value of R1 and R2 should be more than 2.7 k Ω . Optimum performance is achieved when R1 and/or R2 are/is > 10 k Ω .

Demodulator section

Voltages are referenced to GND (ground = 0 V)

		T _{amb} (°C)								TEST CONDITIONS			
CVANDOL	DARAMETER				74HC	т			UNIT	Vcc	OTHER		
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	ONT	VCC	OTHER		
	STATE OTHER	min.	typ.	max.	min.	max.	min.	max.			SYMBOL PARAMETER		
Rs	resistor range	50	ani	300	aps -na	19 20	un ion	d Julia	kΩ	4.5	at R _S $>$ 300 k Ω the leakage current can influence VDEMOUT		
VOFF	offset voltage VCO _{IN} to VDEMOUT	08	±20		8)): I	2	mV	4.5	V _I = V _{VCOIN} = 1/2 V _{CC} , values taken over R _S range see Fig. 13		
RD	dynamic output resistance at DEMOUT	1 12	25		36		88		Ω	4.5	V _{DEMOUT} = 1/2 V _{CC}		

AC CHARACTERISTICS FOR 74HCT

Phase comparator section

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

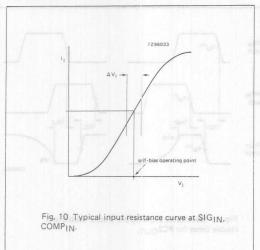
					T _{amb} (°C)				RS	TEST CONDITIONS
0.448.01	No.	92:	7 CZ \$1	- 38	74HC	т	+25			.,	OTUED
SYMBOL	PARAMETER	XBC	+25	.30	-40	to +85	-40 to	+125	UNIT	VCC	OTHER
	$\alpha R_{\rm S} > 300$ kg. 4.5 the lackage α	min.	typ.	max.	min.	max.	min.	max.		95	na rotties) aR
^t PHL/ ^t PLH	propagation delay SIG _{IN} , COMP _{IN} to PC1 _{OUT}		21	40		50	20	60	ns	4.5	Fig. 14
t _{PZH} /	3-state output enable time SIG _{IN} , COMP _{IN} to PC2 _{OUT}		27	56		70	83	84	ns TUO	4.5 qt	Fig. 15 yb
^t PHZ [/]	3-state output disable time SIG _{IN} , COMP _{IN} to PC2 _{OUT}		35	65		81		98	ns	4.5	Fig. 15
t _{THL} /	output transition time		7	15		19		22	ns	4.5	Fig. 14
V _I (p-p)	AC coupled input sensitivity (peak-to-peak value) at SIGIN or COMPIN		15						mV	4.5	f _i = 1 MHz

VCO section

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (°C)				TEST CONDITIONS			
CVMPOI	DADAMETER				74H	ст				.,	071150		
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	VCC	OTHER		
		min.	typ.	max.	typ.	max.	min.	max.					
Δf/T	frequency stability with temperature change				0.15				%/K	4.5	$V_1 = V_{VCOIN}$ within recommended range; R1 = 100 k Ω ; R2 = ∞ ; C1 = 100 pF; see Fig. 16t		
f _O	VCO centre frequency (duty factor = 50%)	11.0	17.0						MHz	4.5	$V_{VCOIN} = 1/2 V_{CC};$ $R1 = 3 k\Omega; R2 = \infty;$ C1 = 40 pF; see Fig. 17		
∆f∨co	VCO frequency linearity		0.4						%	4.5	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 18 and 19		
δνςο	duty factor at VCOOUT		50						%	4.5			

FIGURE REFERENCES FOR DC CHARACTERISTICS



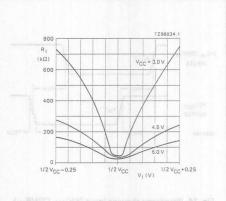


Fig. 11 Input resistance at SIG_{IN}, COMP_{IN} with ΔV_{I} = 0.5 V at self-bias point.

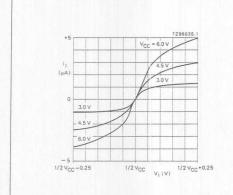
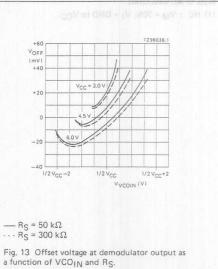


Fig. 12 Input current at SIG $_{IN}$, COMP $_{IN}$ with $\Delta\,V_{I}$ = 0.5 V at self-bias point.



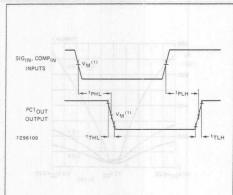
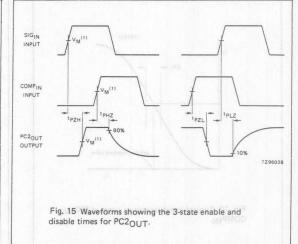
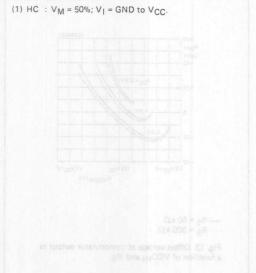


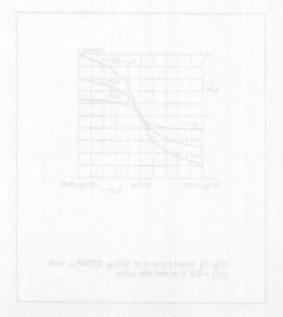
Fig. 14 Waveforms showing input (SIG $_{IN}$, COMP $_{IN}$) to output (PC1 $_{OUT}$) propagation delays and the output transition times.

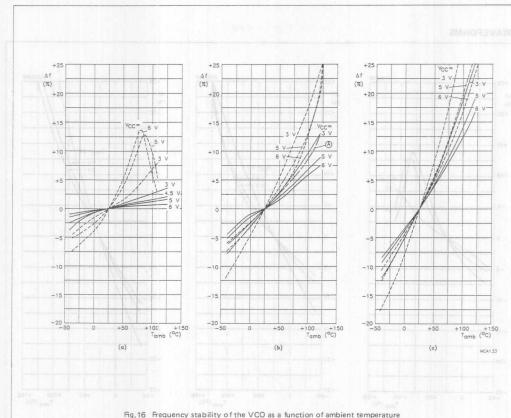
FIGURE REFERENCES FOR DC CHARACTERISTICS

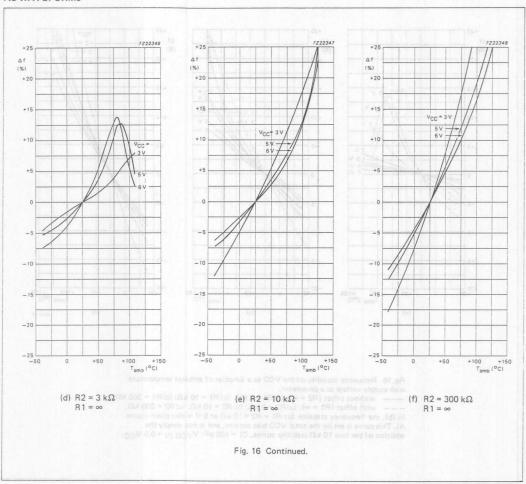


Note to AC waveforms



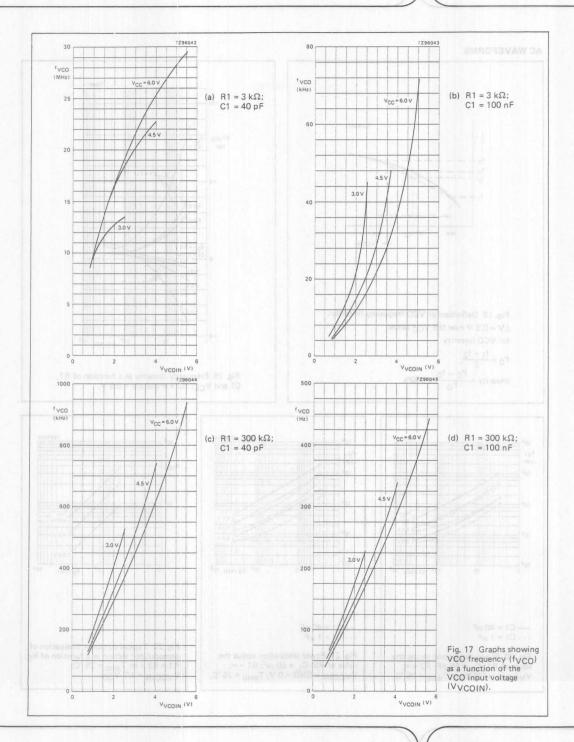






Note to Fig. 16

To obtain optimum temperature stability, C₁ must be as small as possible, but larger than 100 pF.



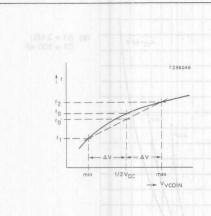


Fig. 18 Definition of VCO frequency linearity: $\Delta V = 0.5 \ V \ \text{over the V}_{CC} \ \text{range:}$ for VCO linearity

$$f'_0 = \frac{f_1 + f_2}{2}$$
,
linearity = $\frac{f'_0 - f_0}{f'_0} \times 100\%$

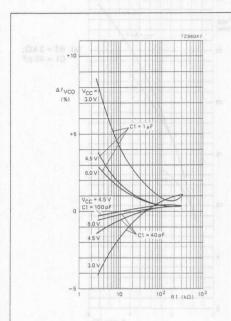
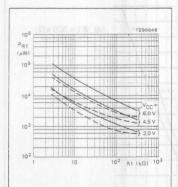
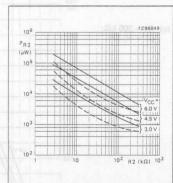


Fig. 19 Frequency linearity as a function of R1, C1 and V_{CC}: R2 = ∞ and Δ V = 0.5 V.



--- C1 = 40 pF --- C1 = 1 μF

Fig. 20 Power dissipation versus the value of R1: $C_L = 50 \text{ pF}$; $R2 = \infty$; $V_{VCOIN} = 1/2 V_{CC}$; $T_{amb} = 25 \,^{\circ}\text{C}$.



- C1 = 40 pF --- C1 = 1 μ F

Fig. 21 Power dissipation versus the value of R2: $C_L = 50 \text{ pF}$; R1 = ∞ ; $V_{COIN} = GND = 0 \text{ V}$; $T_{amb} = 25 \,^{\circ}\text{C}$.

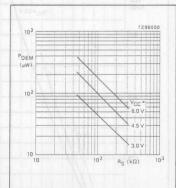


Fig. 22 Typical dc power dissipation of demodulator section as a function of Rs: R1 = R2 = ∞ ; T_{amb} = 25 °C; VVCOIN = 1/2 V_{CC}.

APPLICATION INFORMATION

This information is a guide for the approximation of values of external components to be used with the 74HC/HCT7046 in a phase-lock-loop system.

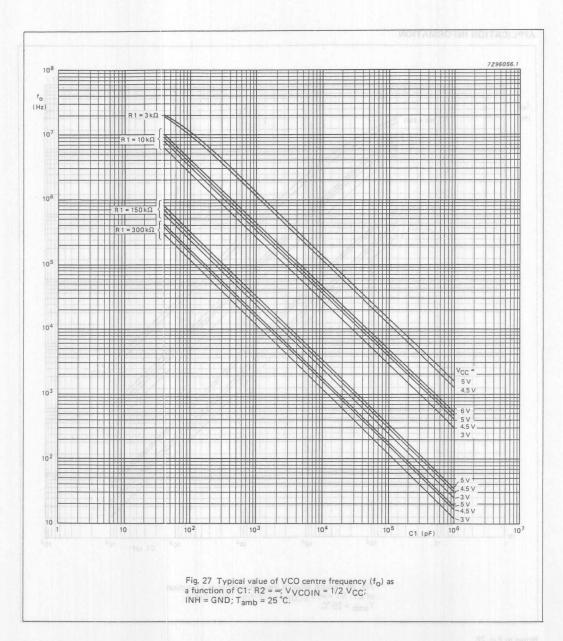
References should be made to Figs 27, 28 and 29 as indicated in the table.

Values of the selected components should be within the following ranges: R1 between $3~k\Omega$ and $300~k\Omega$; R2 between $3~k\Omega$ and $300~k\Omega$; R1 + R2 parallel value $> 2.7~k\Omega$; C1 greater than 40~pF.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency without extra offset	$f(2t_0=1/\pi)(\sqrt{2\pi t_0/r})$	VCO frequency characteristic With R2 = ∞ and R1 within the range 3 k Ω < R1 < 300 k Ω , the characteristics of the VCO operation will be as shown in Fig. 23. (Due to R1, C1 time constant a small offset remains when R2 = ∞ .) **Description** Type 10
	28 45 45 45 51 51 51 51 51 51 51 51 51 51 51 51 51	fmax formulation
	PC1 P Selfo di W J.J.	Given 10, determine the variety of 111 and 01 using 11g. 27.
V00.6		Given f _{max} and f ₀ , determine the values of R1 and C1 using Fig. 27, use Fig. 29 to obtain 2f _L and then use this to calculate f _{min} . VCO frequency characteristic
VCO frequency with extra offset		With R1 and R2 within the ranges $3 k\Omega < R1 < 300 k\Omega$, $3 k\Omega < R2 < 300 k\Omega$, the characteristics of the VCO operation will be as shown in Fig. 24.
		Fig. 24 Frequency characteristic of VCO operating with
	PC1, PC2	offset: f_0 = centre frequency; $2f_L$ = frequency lock range. Selection of R1, R2 and C1 Given f_0 and f_L , determine the value of product R1C1 by using Fig. 29. Calculate f_0 ff from the equation f_0 ff = f_0 — 1.6 f_L . Obtain the values of C1 and R2 by using Fig. 28. Calculate the value of R1 from the value of C1 and the product R1C1.

APPLICATION INFORMATION

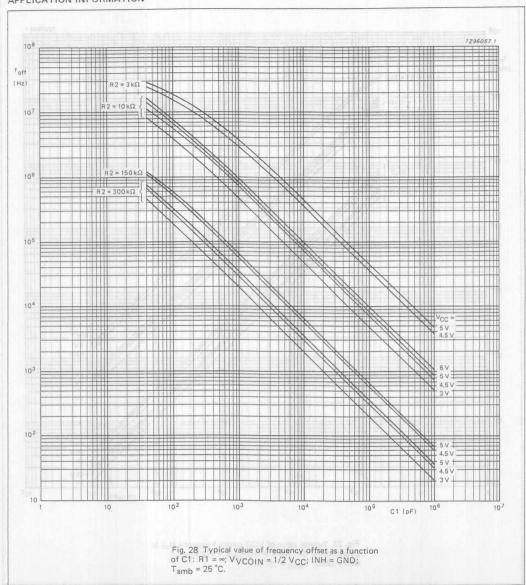
SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS IN THE SECOND S									
PLL conditions	PC1	VCO adjusts to f_0 with $\phi_{DEMOUT} = 90^{\circ}$ and $V_{VCOIN} = 1/2 V_{CC}$ (see Fig. 6).									
with no signal at the SIG _{IN} input	PC2	VCO adjusts to f_0 with $\phi_{DEMOUT} = -360^{\circ}$ and $V_{VCOIN} = min.$ (see Fig. 8).									
PLL frequency capture range	PC1, PC2	Loop filter component selection									
		UBJECT PRASE DESIGN CONSIDERATIONS									
	$R\Omega < R1 < 300 k\Omega$, the										
	Fig. 23. set remains when R2 = x	(a) $\tau = R3 \times C2$ (b) amplitude characteristic (c) pole-zero diagram									
		A small capture range (2f _c) is obtained if $2f_{\rm c}\approx 1/\pi~(\sqrt{2\pi f_{\rm L}/\tau})$									
	20/4 A 6 8 - 20/4 3 7 2 4 2 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	Fig. 25 Simple loop filter for PLL without offset; R3 \geqslant 500 Ω . INPUT OUTPUT $m = \frac{R4}{R3 + R4}$ $m = \frac{R4}{R3 + R4}$ 7298054									
	ctedatic of VCO operation (27) = frequency for	τ ₂ = R4 x C2; τ ₃ = (R3 + R4) x C2									
PLL locks on	PC1 may to be a fer to	To real teaching and managed the control of the con									
harmonics at centre frequency	PC2	no									
noise rejection at	PC1E CON ODE > IR >	With R1 and R2 within the range delific									
signal input	PC2	low									
AC ripple content when PLL is	PC1	$f_r = 2f_1$, large ripple content at $\phi_{DEMOUT} = 90^\circ$									
locked	PC2	$f_r = f_i$, small ripple content at $\phi_{DEMOUT} = 0^\circ$									



Notes to Fig. 27

 To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
 Interpolation for various values of R1 can be easily calculated because, a constant R1C1 product will produce almost the same VCO. output frequency.

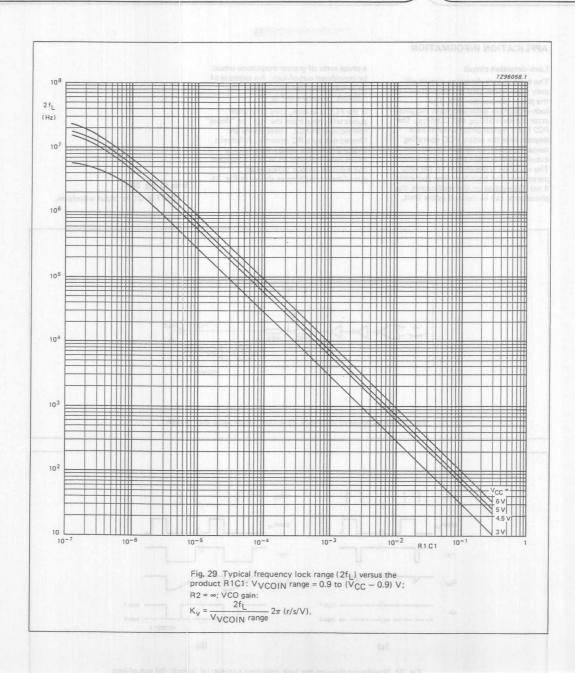
APPLICATION INFORMATION



Notes to Fig. 28

1. To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.

Interpolation for various values of R2 can be easily calculated because, a constant R2C2 product will produce almost the same VCO output frequency.



APPLICATION INFORMATION

Lock-detection circuit

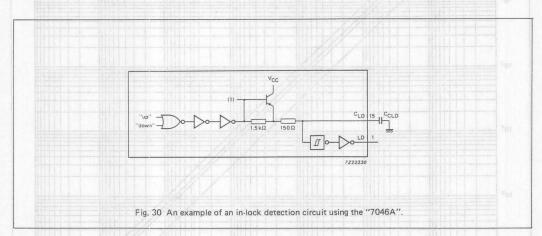
The built-in lock-detection circuit will only work when used in conjunction with the phase comparator PC2. The lock-indication is derived from the phase error between SIG_{IN} and COMP_{IN}. The PC2 has a typical phase error of zero degrees over the entire VCO operating range. However, to remain in-lock the circuit requires some small adjustments. The variation is dependent on the loop parameters and back-lash time (typically 5 ns). Depending on the application, the phase error can be defined as the limit,

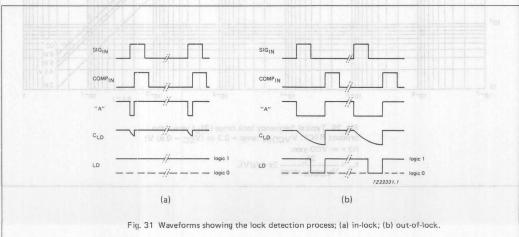
a phase error of greater magnitude would be considered out-of-lock. An example of an in-lock detection circuit using the "7046A" is shown in Fig. 30.

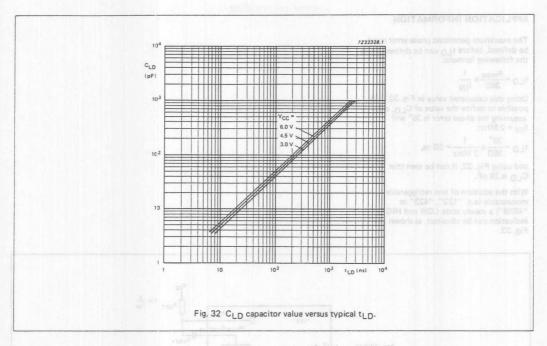
If the PLL is in-lock, only very small pulses will come from the "up" or "down" connections of PC2. These pulses are filtered out by a RC network. A Schmitt trigger produces a steady state level, a HIGH level indicates an in-lock condition and a pulsed output indicates an out-of-lock condition as shown in Fig. 31.

Note to Fig. 30

(1) See Fig. 31 for input waveform.







Where:

C_{LD} = capacitor connected to pin 15

(includes the parasitic input capacitance of the IC, approximately 3.5 pF).

t_{LD} = phase difference between SIG_{IN} and COMP_{IN} (positive-going edges).

APPLICATION INFORMATION

The maximum permitted phase error must be defined, before t_{LD} can be defined using the following formula:

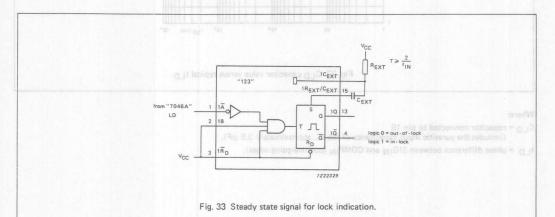
$$t_{LD} = \frac{\phi_{max}}{360} \times \frac{1}{f_{IN}}.$$

Using this calculated value in Fig. 32, it is possible to define the value of C_{LD}, e.g. assuming the phase error is 36° and fin = 2 MHz:

$$t_{LD} = \frac{36^{\circ}}{360} \times \frac{1}{2 \text{ MHz}} = 50 \text{ ns,}$$

and using Fig. 32, it can be seen that $\rm C_{LD}$ is 26 pF.

With the addition of one retriggerable monostable (e.g. "123", "423" or "4538") a steady state LOW and HIGH indication can be obtained, as shown in Fig. 33.



PLL design example

The frequency synthesizer, used in the design example shown in Fig. 34, has the following parameters:

The open-loop gain is H (s) \times G (s) = $K_0 \times K_f \times K_0 \times K_n$.

Where:

K_p = phase comparator gain K_f = low-pass filter transfer gain

 $K_0 = K_v/s$ VCO gain $K_n = 1/n$ divider ratio

The programmable counter ratio $K_{\mbox{\scriptsize n}}$ can be found as follows:

$$N_{min.} = \frac{f_{out}}{f_{step}} = \frac{2 \text{ MHz}}{100 \text{ kHz}} = 20$$

$$N_{\text{max.}} = \frac{f_{\text{out}}}{f_{\text{step}}} = \frac{3 \text{ MHz}}{100 \text{ kHz}} = 30$$

The VCO is set by the values of R1, R2 and C1, R2 = $10~\mathrm{k}\Omega$ (adjustable). The values can be determined using the information in the section

"DESIGN CONSIDERATIONS". With f_0 = 2.5 MHz and f_L = 500 kHz this gives the following values (V_{CC} = 5.0 V):

 $R1 = 10 \text{ k}\Omega$ $R2 = 10 \text{ k}\Omega$

The VCO gain is:

$$K_V = \frac{2f_L \times 2 \times \pi}{0.9 - (V_{CC} - 0.9)} =$$

= $\frac{1 \text{ MHz}}{3.2} \times 2\pi \approx 2 \times 10^6 \text{ r/s/v}$

The gain of the phase comparator is:

$$K_p = \frac{V_{CC}}{4 \times \pi} = 0.4 \text{ V/r}.$$

The transfer gain of the filter is given by:

$$K_f = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2) s}$$

Where:

$$\tau_1$$
 = R3C2 and τ_2 = R4C2.

The characteristics equation is: $1 + H(s) \times G(s) = 0$.

This results in:

$$\begin{split} s^2 + \frac{1 + \mathsf{K}_\mathsf{p} \times \mathsf{K}_\mathsf{v} \times \mathsf{K}_\mathsf{n} \times \tau_2}{(\tau_1 + \tau_2)} \, s + \\ \frac{\mathsf{K}_\mathsf{p} \times \mathsf{K}_\mathsf{v} \times \mathsf{K}_\mathsf{n}}{(\tau_1 + \tau_2)} &= 0. \end{split}$$

The natural frequency ω_n is defined as follows:

$$\omega_{n} = \sqrt{\frac{K_{p} \times K_{v} \times K_{n}}{(\tau_{1} + \tau_{2})}}.$$

and the damping value ξ is defined as

$$\zeta = \frac{1}{2\omega_{n}} \times \frac{1 + K_{p} \times K_{v} \times K_{n} \times \tau_{2}}{\tau_{1} + \tau_{2}}.$$

The overshoot and settling time percentages are now used to determine ω_n . From Fig. 35 it can be seen that the damping ratio $\zeta=0.8$ will produce an overshoot of less than 20% and settle to within 5% at $\omega_n t=4.5$. The required settling time is 1 ms. This results in:

$$\omega_{\rm n} = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3 \text{ r/s}.$$

Rewriting the equation for natural frequency results in:

$$(\tau_1 + \tau_2) = \frac{K_p \times K_v \times K_n}{\omega_n^2}.$$

The maximum overshoot occurs at N_{max}.:

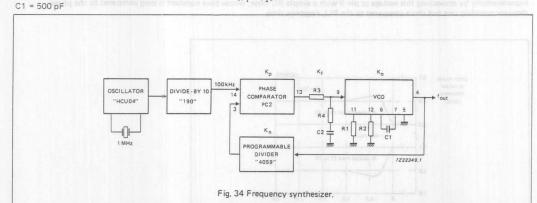
$$(\tau_1 + \tau_2) = \frac{0.4 \times 2 \times 10^6}{5000^2 \times 30} = 0.0011 \text{ s.}$$

When C2 = 470 nF, then

R4 =
$$\frac{(\tau_1 + \tau_2) \times 2 \times \omega_n \times \zeta - 1}{K_p \times K_v \times K_n}$$
 = 790 Ω .

R3 is calculated using the damping ratio equation:

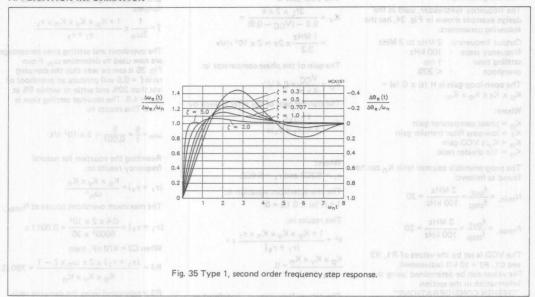
$$R3 = \frac{\tau_1}{C2} - R4 = 2 k\Omega.$$



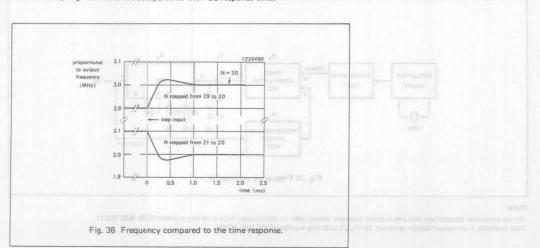
None

For an extensive description and application example please refer to application note ordering number 9398 649 90011. Also available a computer design program for PLL's ordering number 9398 961 10061.

APPLICATION INFORMATION



Since the output frequency is proportional to the VCO control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 9 of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin 9 with a simple RC filter, whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time.



16-BIT EVEN/ODD PARITY GENERATOR/CHECKER

FEATURES

- · Word-length easily expanded by cascading
- Generates either even or odd parity for 16-data bits
- Output capability: standard
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT7080 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7080 are 16-bit parity generators or checkers commonly used to detect errors in high-speed data transmission or data retrieval systems.

The even and odd parity output is available for generating or checking even/ odd parity up to 16-bits.

The even/odd parity output (E/\overline{O}) is HIGH when an even number of data inputs (I₀ to I₁₅) are HIGH and the cascade/even-odd-changing input (\overline{X}) is

Expansion to larger word sizes is accomplished by connecting the even/odd parity output (E/\overline{O}) to the cascade/even-odd-changing input (X) of the final stage.

OV CARDON	DADAMETER	CONDITIONS	TYF	UNIT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
^t PHL [/] ^t PLH	propagation delay I_{Π} to E/\overline{O} \overline{X} to E/\overline{O}	C _L = 15 pF V _{CC} = 5 V	29 12	32 15	ns ns
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	24	25	pF

GND = 0 V; $T_{amb} = 25 \,^{\circ}\text{C}$; $t_r = t_f = 6 \, \text{ns}$

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

PD = CPD x
$$VCC^2$$
 x f_i + Σ (CL x VCC^2 x f_o) where:

fi = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_1 \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

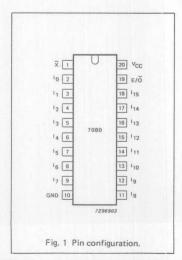
2. For HC the condition is VI = GND to VCC For HCT the condition is $V_1 = GND$ to $V_{CC} - 1.5 \text{ V}$

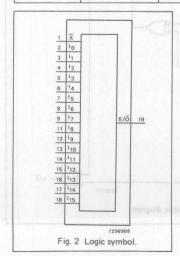
PACKAGE OUTLINES

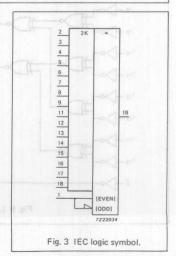
20-lead DIL; plastic (SOT146). 20-lead mini-pack; plastic (SO20; SOT163A).

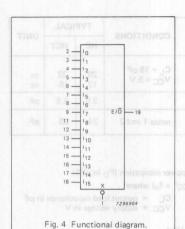
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	₹	cascade/even-odd-changing input
2, 3, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16, 17, 18	I ₀ to I ₁₅	data inputs
10	GND	ground (0 V)
19	E/O	even/odd parity output
20	Vcc	positive supply voltage









F

INPU'	TS	OUTPUTS
In	X	E/Ō
$\Sigma = E$	ioneHib o	t beau at H. 9.3
$\Sigma \neq E$	Ĥ	andui H ij

For HCT the condition is V neve = 3

H = HIGH voltage level L = LOW voltage level

7296995 Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

			T _{amb} (°C)							TEST CONDITIONS	
	74HC		-	WAVEFORMS							
SYMBOL	PARAMETER	+25				v _{CC}	WAVELORMS				
		min.	typ.	max.	min.	max.	min.	max.	e cascad	d) priby	Fig. 6 Weveforms she input (X) to the even
^t PHL [/]	propagation delay		91 33 26	280 56 48		350 70 60		420 84 71	ns no	2.0 4.5 6.0	Fig. 7
t _{PHL} /	propagation delay X to E/O		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t _{THL} /	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\frac{I_n}{X}$	1.0

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

					T _{amb} (°C)				TEST CONDITIONS		
SYMBOL	DADAMETED				74HC	т			UNIT	V	WAVEFORMS	
STIMBUL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/	propagation delay		37	63		79		95	ns	4.5	Fig. 7	
t _{PHL} /	propagation delay X to E/O		18	32		40		48	ns	4.5	Fig. 6	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7	

AC WAVEFORMS

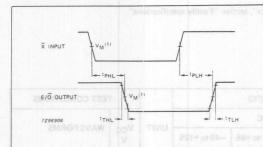


Fig. 6 Waveforms showing the cascade/even-odd-changing input (\overline{X}) to the even/odd parity output (E/\overline{O}) propagation delays and the output transition times.

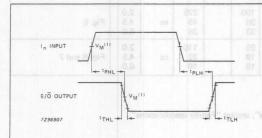


Fig. 7 Waveforms showing the data inputs (I $_{\rm I}$) to the even/odd parity output (E/ $\bar{\odot}$) propagation delays and the output transition times.

AC CHARACTERISTICS FOR 7AHC

SYMBOL PARAMETER +28

28 48 150 200 appropriate the tensition time 7 15 26 13 27 15 26 27 15 2

DC CHARACTERISTICS FOR TAHCT
For the DC characteristics sea chapter "HCMOS family char

Note to AC waveforms

(1) HC: $V_M = 50\%$; $V_I = GND \text{ to } V_{CC}$. HCT: $V_M = 1.3 \text{ V}$; $V_I = GND \text{ to } 3 \text{ V}$.

AC CHARACTERISTICS FOR TAHCT

TEST CIRCUIT AND WAVEFORMS

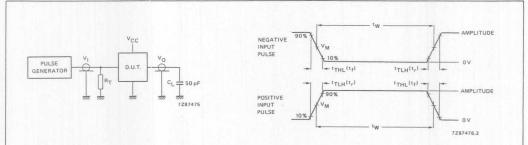


Fig. 8 Test circuit for measuring AC performance.

Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for value)

(see AC CHARACTERISTICS for values).

RT = termination resistance should be equal to the output impedance Z_O of the pulse generator.

		t _r ;t		
FAMILY	AMPLITUDE	VM	f _{max} ; PULSE WIDTH	OTHER
74HC	Vcc	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

TEST CIRCUIT AND WAVEFORMS

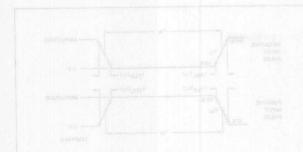


Fig. 8. Test circuit for measuring AC performance.

Definitions for Figs 8 and 6:

C_L = load capacitance including (ilp and

97 = termination resistance should be equal to the ductout impactance 20 of the pulse



anominitab artus rugal 8 pi-

Quad precision adjustable Schmitt-trigger/comparator with output latches; 3-state

74HC/HCT7132

FEATURES

- Precision inputs
- 2 operation modes: PAST and comparator
- In PAST mode: Inverting outputs in view of the precision oscillator application
- In comparator mode: Non-inverting outputs to simplify the design of an external hysteresis network
- 3-state outputs for bus oriented applications
- · Output capability: Bus driver
- I_{cc} category: MSI

APPLICATIONS

- · Precision oscillators
- · Signal reconditioning
- Level conversion
- Process control (temperature, pressure, power e.g.)
- Accurate level detectors
- Time delays
- Overvoltage, overcurrent protection
- · Bargraph display with LED's
- · Battery charge control
- · Analog to digital conversion

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25 \, ^{\circ}\text{C}$; $t_r = t_f = 6 \, \text{ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
	High trip level	PAST mode; V _{cc} = 3 to 6 V	1.15 to V _{cc} - 1.2	V
V _{rH}	reference level	Comparator mode; V _{cc} = 3 to 6 V	0.6 to V _{cc}	V
V _{rL}	Low trip level	PAST mode; V _{cc} = 3 to 6 V	1.10 to V _{cc} – 1.25	V
δV_t	DC inaccuracy	V _{cc} = 3 to 6 V	±20	mV
C _{PD}	power dissipation capacitance per function	V _{CC} = 5 V PAST mode Comparator mode	100	pF pF
P _d	Total DC power dissipation	Comparator mode; $V_{CC} = 4.5 \text{ V};$ $V_{rL} = V_{INn} = 0 \text{ V};$ $V_{rH} = 2.25 \text{ V}$	SYMBOL	mW
t_{min}/t_{min}	Minimum rise and fall time for optimum operation	PAST mode; V _{CC} = 4.5 V; V _{rH} = 3 V; V _{rL} = 1.5 V	180	ns
t _{PHL} /t _{PLH}	propagation delay V _{inn} to Q	PAST mode; V _{cc} = 4.5 V	40/60	ns

DESCRIPTION

The 74HC/HCT7132 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7132 contain 4 comparators with two common reference inputs $V_{\rm rh}$ and $V_{\rm rL}$ and four separate signal inputs $V_{\rm in0}$ to $V_{\rm in3}$. The circuits can be applied in two modes:

1) The PAST (precision adjustable Schmitt-trigger) mode at which a voltage level equal to the wanted $V_{T_{+}}$ must be applied to the V_{rH} input and a voltage level equal to the wanted $V_{T_{-}}$ to the V_{rL} input.

Notes to the quick reference data:

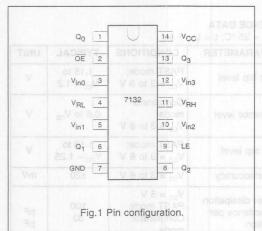
- 1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW): $P_D = C_{PD} \times V_{CC}^2 \times f_i + C_L \times V_{CC}^2 \times f_o \text{ where:}$
 - f_i = input frequency in MHz; C_L = output load capacity in pF; f_a = output frequency in MHz; V_{CC} = supply voltage in V.

ORDERING INFORMATION

TYPE NUMBER	and to the	PAC	KAGE	
MAD about about a	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT7132P	14	DIL DIL	plastic	SOT27
74HC/HCT7132T	14	so	plastic	SOT108

Quad precision adjustable Schmitt-trigger/comparator with output latches; 3-state

74HC/HCT7132



| 9 | LE | 3 | V_{in0} | Q₀ | 1 | 5 | V_{in1} | Q₁ | 6 | 10 | V_{in2} | Q₂ | 8 | 12 | V_{in3} | Q₃ | 13 | 11 | V_{rH} | V_{rL} | Q_E | Q_D
PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 6, 8, 13	Q _o to Q ₃	3-state latch outputs
2	ŌĒ	3-state output enable input (active LOW)
3, 5, 10, 12	V _{in0} to V _{in3}	signal inputs
4 an	V _{rL}	low reference voltage input
7	GND	ground (0 V)
9	LE 08:04	latch enable input (active HIGH)
11	V _{rH}	high reference voltage input
14	V _{cc}	positive supply voltage

FUNCTION TABLE for PAST mode (table 1)

V _{inn} (rising edge)	LE	OE	Qn
$V_{inn} < V_{LL}$	L no	trevac	Hava
$V_{LL} < V_{inn} < V_{rH}$	19 (rem <u>7</u> let	GENOO!	HOOTH
$V_{HH} > V_{inn} > V_{rH}$	Francis in	L	L
$V_{inn} > V_{HH}$	L	Lavol	L
V _{inn} (falling edge)	LE LE	OE	Qn
$V_{HH} > V_{inn} > V_{rL}$	L	L no	Listorq
$V_{LL} < V_{inn} < V_{rL}$	Liw vs	Leib ri	BargH
$V_{inn} < V_{LL}$	Franco	Grauo	Hamed
$V_{inn} = X$	H	F	Q _{t-1}
$V_{inn} = X$	X	H	Z

2) The comparator mode at which the V_{rL} input must be connected to GND and the V_{rH} input is the active reference level input. In this mode a few resistors must be added to achieve a small hysteresis in order to avoid oscillations. The operation in both modes will be further explained by means of the logic diagram of fig.5.

DETAILED DESCRIPTION

The mode selector.

See fig.5 for logic diagram. The circuit can be applied in two modes that are selected by the mode selector on bases of the level on the $V_{\rm RL}$ input. When the level on

this input is in the operating area of the PAST mode ($V_{\rm rL} > 1$ V) the true output of the mode detector is "0" which means that the PAST mode is selected. When the $V_{\rm rL}$ input is at GND level the true output of the mode detector is "1" by which the comparator mode is selected. This mode needs only one reference input being the $V_{\rm rH}$ input.

The Power-on Detector

The power-on detector selects a window typically between $V_{\text{INn}} = 1 \text{ V}$

H = HIGH voltage level

L = LOW voltage level

Z = high impedance OFF-state

X = don't care

 Q_{t-1} = initial state

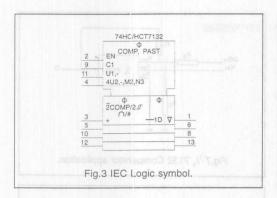
and $V_{\text{INn}} = V_{\text{CC}} - 1$ V in which in case of the PAST mode the power of the analog part (comparator) is switched on. When operating in the comparator mode the power is always switched on by means of an OR gate.

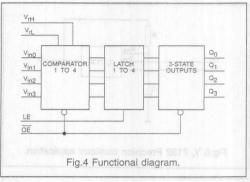
The digital detector

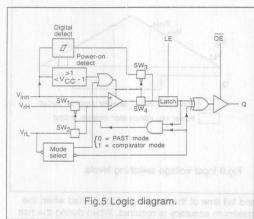
The digital detector is a Flip-Flop which output is set to LOW when

Quad precision adjustable Schmitt-trigger/comparator with output latches; of same 3-state

74HC/HCT7132







 $V_{\rm INn}$ < 1 V and to HIGH when $V_{\rm INn}$ > $V_{\rm CC}$ = 1 V. This detector controls the output stage in the cases that the power of the comparator is switched off. This is performed by means of the switches SW₃ and SW₄.

The latch

The output information can be stored in a latch on activating the LE input. In the PAST mode this latch is also used to control the reference input of the comparator which is either connected to the V_{rH} input via SW_1 or to the V_{rL} input via SW_2 . In case of the comparator mode the reference input is always connected to the V_{rH} input. This is done by means of an AND gate.

The exclusive OR gate

By means of this function the output stage is switched between inverting and non-inverting. In the PAST mode the inverting output of the mode selector is "1"

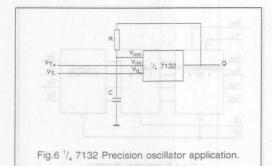
so the exclusive OR is inverting. In the comparator mode this output is "0" so the exclusive OR is non-inverting.

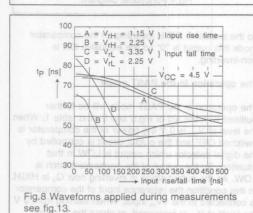
The operation in the PAST mode

The operation in the PAST mode will be further outlined with the aid of Fig.5 and 9, and table 1. When the level of V_{INn} is 0 V the power of the comparator is switched OFF and the output circuit is controlled by the digital detector which output is LOW in that situation. So the output of the transparent latch is LOW. As the output stage is inverting now Q is HIGH. In this condition the reference input of the comparator is connected to the +V_{rH} input. When starting from 0 V the level at V_{inn} is increased, at about the V_{II} level (≈1 V) the DC power of the comparator is switched ON. The control of the output circuit is switched over from the digital detector output to the comparator output, when after a delay the voltage at this node is stabilised. During this operation the output level of the latch output remains LOW and the level of Q HIGH. When the level at V_{inn} reaches the V_{rH} level the output level of the comparator turns to HIGH and so the output level of the transparent latch. The level at Q turns to LOW. In this instant the reference input of the comparator is switched over from V_{rH} to V_{rI} leaving the output voltage at Q constant. When the level at Vinc reaches the V_{HH} level (≈V_{CC} - 1 V) the DC power of the comparator is switched OFF. The control of the output circuit is switched over from the comparator output to the digital detector output which voltage level is HIGH in this situation. During this action the level at Q_n remains LOW. When the level at the V_{inn} input is decreased starting at V_{CC} level, at the V_{HH} level (≈V_{CC} - 1 V) the power of the comparator will be switched on again. The control of the output circuit

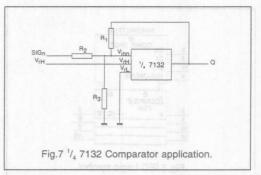
Quad precision adjustable Schmitt-trigger/comparator with output latches; 3-state

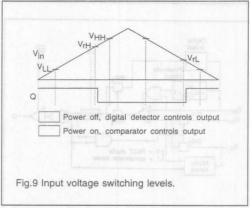
74HC/HCT7132





is switched over from the digital detector output to the comparator output when after a delay the voltage at this node is stabilised. As the comparator output level is HIGH in this situation the output level of the latch remains HIGH and the Q output LOW. When the level at V_{inn} reaches the V_{rL} level the output level of the comparator turns to LOW and so the output level of the transparent latch. The level at Q turns to HIGH. In this instant the reference input of the comparator is switched over from V_{rt} to V_{rt} leaving the output voltage at Q_n constant. When the level at V_{inn} reaches about 1 V the DC power of the comparator is switched OFF again. The control of the output circuit is switched over from the comparator output to the digital detector output which voltage level is LOW in this situation. During this action the level at Q remains HIGH. The function of the circuit is a Schmitt-Trigger of which the V_{T+} and V_{T-} levels can be set at the V_{rH} and V_{rL} inputs. These levels can be varied from $\approx 1 \text{ V}$ up to ≈V_{CC} - 1 V. so the maximum obtainable hysteresis is ≈V_{cc} - 2 V. The on-and off switching of the power and the stabilisation of the comparator needs time, therefore the minimum applicable rise-





and fall time of the input signal are limited when the maximum accuracy is required. When during the rise time of the input signal the input level has past the V, level, the power starts to switch on. Only when the comparator is stable at the moment that the input signal passes the V_H level the comparator has its true delay and its optimal accuracy. When the V, level is passed before the comparator is stable an extra delay occurs due to the switching of the power and the accuracy of the comparator is less. At the positive going edge, this extra delay depends on the difference between V₁₁ and V₂₁ and the rise time of the signal. This is shown in Fig.8, where by means of curves A and B t_{PHL} is plotted at V_{rH} is 1.15 V and 2.25 V respectively and V_{cc} = 4.5 V. As with curve a V_{rH} is very close to V₁₁ the part of the input edge that is available for switching the power on is very small. This causes that only at a rise time > 500 ns/V the delay will be equal to the true delay of the comparator. At V_{rH} = 2.25 V this situation is reached already at a rise time of 120 ns/V. At a very short rise time, the major part of the propagation delay is due to the switching (Continued) and application has primary assured

Quad precision adjustable Schmitt-trigger/comparator with output latches; 3-state

74HC/HCT7132

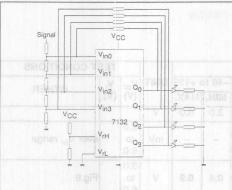


Fig. 10 Possible circuit for a bargraph.

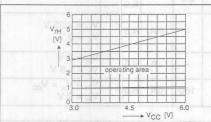


Fig.12 Operating area for V_{rH} in comparator mode.

time of the power. At the negative going edge, the power is switched on when the level V_{HH} is passed so the extra delay depends on the difference between V_{HH} and V_{rl} and the fall time of the signal. This situation is referred to with curves C and D where tpl H is drawn against the fall time of the input signal. With curve C V_{rt} is 3.25 V which is on the edge of the operating region. Curve D corresponds with a V_{rt} value of 2.25 V. For linear input edges the recommended minimum rise time at V_{cc} = 4.5 V or 6 V is 100 ns/V and at V_{cc} = 3 V, 300 ns/V. For non-linear input signals, during the rising edge there must be a delay between the time at which the VLL level is passed and the time at which the V_{rH} level is passed. This delay will be dependent on the V_{cc} level and the amplitude of the overdrive of V_{LL}. There is no limitation on the signal slope during the passing of the levels. For the same reasons, during the falling edge there must be a delay between the time at which the V_{HH} level is passed and the time at which the V_{rL} level is passed.

A possible application of the circuit is as precision oscillator see Fig.6. The operating frequency is:

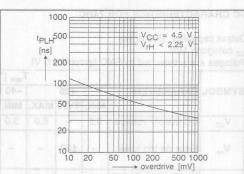


Fig.11 Curve showing the $t_{\text{PLH}}/t_{\text{PHL}}$ as a function of the overdrive for the comparator application. Waveforms applied during measurements see fig.13.

$$f = \frac{1}{t_{\text{RC}} + 2 \times (t_{\text{PLH}} + t_{\text{PNL}})} \text{ where } t_{\text{RC}} = 2 \times \text{In } \left(\frac{V_{\text{CC}} - V_{\text{rL}}}{V_{\text{CC}} - V_{\text{rH}}}\right) \times \text{RC}$$

The operation in the comparator mode

The IC can be applied as a comparator by connecting the $V_{\rm nL}$ input to GND and adjusting the level at $V_{\rm nL}$ to the wanted detection level see Fig.7. In this mode the DC power of the comparator is always on and the output stage is set to non-inverting. The function table for this operation mode is given in table 2.

FUNCTION TABLE for Comparator mode (table 2)

INPUT	LE	ŌĒ	Q _n
$V_{inn} < V_{ref}$	L	L ("V) de	JeL MV
$V_{inn} > V_{ref}$	L	L NAME OF THE PARTY NAME OF TH	Н
$V_{inn} = X$	Н	L (L ₁ V) ,le	Q _{n-1}
$V_{inn} = X$	X	H mumir	Z

H = HIGH voltage level

L = LOW voltage level

Z = high impedance OFF-state

X = don't care

The fact that the power is always on offers the feature of a more extended operation region of the V $_{\rm H}$ input voltage which is at a V $_{\rm CC}$ of 4.5 V from 1.1 V up to 4.2 V see also Fig.12. A hysteresis of about 50 mV is required to overcome oscillations. This has to be performed by means of a few external resistors. The DC power in this operation mode at V $_{\rm CC}$ = 4.5 V is typical 2 mW per function. A curve showing t $_{\rm PD}$ as a function of the overdrive is given in Fig.11. A possible diagram for a bargraph display is shown in Fig.10.

Quad precision adjustable
Schmitt-trigger/comparator with output latches; 74HC/HCT7132 3-state

DC CHARACTERISTICS FOR 74HC

Output capability: Bus driver

Icc category: MSI

Voltages are referenced to GND (ground = 0 V)

					T _{amb} (°	C)					TES	ST CONDITIONS
SYMBOL	PARAMETER		+25		-40 t	0 +85	-40 to	0 +125	UNIT	V _{cc}	V	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		(V)	(V)	OTTIER
V _{cc}	DC supply voltage	3.0	-	6.0	3.0	6.0	3.0	6.0	V		SIN	n vec
V _{err}	Error on trip level	08	±20	-	-	-	-	-	mV	3.0 to 6.0	10	over V _{ref} range
VILLOIT	V _{IN} at which power for comparator is switched ON	0.4	0.7	0.9	0.4	0.9	0.4	0.9	V	3.0 to 6.0		Fig.9
V _{HH}	V _{IN} at which power for comparator is switched OFF	V _{cc} -	V _{cc} - 0.9	V _{cc} - 0.5	V _{cc} -	V _{cc} - 0.5	V _{cc} -	V _{cc} - 0.5	V	3.0 to 6.0		Fig.9
I _{cc}	active supply current. Comparator mode	(19) (Gal	2.0	3.4	in a	-	_		mA	4.5		$V_{rH} = 2.25 \text{ V}$ $V_{rL} = 0 \text{ V}$
I _{cc}	supply current. PAST mode	00 00	30	50	0 9(1)	-	-	-	μА	4.5	1000	$V_{rH} = 3 V$ $V_{rL} = 1.5 V$
I _{cc}	quiescent supply current	C end	MG-01	8	V anti	80	-	160	μА	6.0		$V_{rH} = V_{rL} = V_{CC}$ $V_{IN} = 0 V$

eldel no	i-inventing. I he rundt	ion of	tea at	stage	T _{amb} (°	C)	10	nparate	in coi	V 10	TES	T CONDITIONS
SYMBO	PARAMETER	8001	+25	BISUD I	-40 t	0 +85	-40 to	+125	UNIT	V _{cc}	V,	OTHER
(> aint	dealing and mode in	MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		(V)	(V)	OTHER
V _{rH}	HIGH reference level, (V _{T+})	1.15	-	V _{cc} - 1.2	1.15	V _{cc} - 1.2	1.15	V _{cc} - 1.2	of Supplemental Su	3.0 to 6.0	to alt	e extra delay depen
V _{rL}	LOW reference level, (V _{T-})	1.1	-	V _{cc} - 1.25	1.1	V _{cc} - 1.25	W .lar 1.1;	V _{cc} - 1.25	m ent V no spond	3.0 to 6.0	all tir which	drawn against the fi rve C V _{v.} is 3.25 V erating region. Curv
V_{Hmin}	Minimum hysteresis voltage, (V _{rH} - V _{rL})	ioval	50	V HBIR	anlV	-	5 ¥ ol For	(he co = 4 ns/V.	mV	3.0 to 6.0	neen in mi	liue of 2,25 V. For li commended minima V is 100 ns/V and a

COMPARATOR mode date 440 sonsbegin doin = X

		T _{amb} (°C)					leval	V erit	which	TEST CONDITIONS			
SYMBOL	PARAMETER	+25		isru to	-40 to +85 -40 to +125		UNIT	+125 UNIT		V,	OTHER		
	Value region of the V	MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		(V)	(V)	lo ebuilding and bo	
V _{rHmin}	minimum reference level	Ă ST	0.6	la <u>e</u> 93	V <u>e</u> A	- 81	bs-gn	e past he-fall	V	4.5	1000	over V _{ref} range	
V	maximum reference level	lo an	V _{cc}	med b	perior	lav	ar W	rit dail	٧	4.5	rii b	over V _{ref} range	

Quad precision adjustable
Schmitt-trigger/comparator with output latches; 74HC/HCT7132 3-state

AC CHARACTERISTICS FOR 74HC

					T _{amb} (°	C)			LIMIT		TE	ST C	ONDITIONS
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	0 +125	UNI	V _{cc}	V _{rH}	W	WAVEFORMS
	DOMOS TRAT	MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	OF LOO	(V)	V _{rH}	V _{rL}	WAVEFURING
t _{PHL}	propagation delay V _{inn} to Q _n ; PAST mode	V)	80 50 40	MAN	-40 MIN 4.5	BBT of	-40 MM	MAX.	ns	3.0 4.5 6.0		1.50	t _r = 300 ns/V t _r = 100 ns/V t _r = 100 ns/V Fig.13
t _{PLH} 50	propagation delay V _{inn} to Q _n ; PAST mode	6,4 67 6.6	80 50 40		-	-	-	-	ns	3.0 4.5 6.0	1.67 3.00 4.00	1.50 1.50 2.00	t _r = 300 ns/V t _t = 100 ns/V t _t = 100 ns/V Fig.13
t _{PHL}	propagation delay V _{inn} to Q _n ; Comparator mode	3.A - - - - - -	100 60 50	0.9	Þ.0 - - - - -	e.o - - 0. +	0.4 - - - 3.4	0.9	ns 8.8	3.0 4.5 6.0	V _{cc} /2	erate NO	Fig.14, overdrive: 100 m
t _{РLН}	propagation delay V _{inn} to Q _n ; Comparator mode	8.H	80 50 40		-	-	-	5.4	2.0 ns	3.0 4.5 6.0	V _{cc} /2	0.00	Fig.14, overdrive: 100 m
t _{PHL} /t _{PLH}	propagation delay LE to Q _n	a 4	35 23 18	160	-	09	-	8-	ns	3.0 4.5 6.0	ylo	que 1	Fig.15
t _{PZH} /t _{PZL}	3-state output enable time OE to Q _n	T#//(22 15 13	- - - + + 0	- - 5-48	(D*)	dma ^T	- - -	ns S+	3.0 4.5 6.0		RB 13	Fig.17
t _{PHZ} /t _{PLZ}	3-state output disable time DE to Qn	-	22 17 14	M = JA F ac	MH.O	oV_	40A .	XAAA SoV	ns	3.0 4.5 6.0	63	inere	Fig.17
t _{THL} /t _{TLH}	output transition time	-	25 10 9	<u> </u>		- '- oV_ (0.7	- V	ns	3.0 4.5 6.0	9	pnend	Fig.13
t _w	LE pulse width	- - ∀m	12 6 5	-	1	-	-	-	ns	3.0 4.5 6.0	SUB	lov a	Fig.15
t _{su}	set-up time V _{inn} to LE	-	30		-			-	ns	4.5	3.00	1.50	Fig.16, for V_{INn} : $t_r = t_f = 180 \text{ ns}$
t _n sa	hold time V _{inn} to LE	V T	-30	10 ±12	OE-	284_08 XAM	OP-	XAM .	ns	4.5 6.0	3.00	1.50	Fig.16, for V_{INn} : $t_r = t_f = 180 \text{ ns}$

Quad precision adjustable Schmitt-trigger/comparator with output latches; of stage 3-state

74HC/HCT7132

DC CHARACTERISTICS FOR 74HCT

Output capability: Bus driver

I_{cc} category: MSI

Voltages are referenced to GND (ground = 0 V)

177				Totaliet.	T _{amb} (°	C)	CHECKEN !	APRILL	37113	mint.	TE	ST CONDITIONS
SYMBOL	PARAMETER	2 1	+25		-40 t	0 +85	-40 t	0 +125	UNIT	Vcc	V	OTHER
	4.00 2.00t = 100	MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		(V)	(V)	10 of V
V _{cc}	DC supply voltage	4.5	-	5.5	4.5	5.5	4.5	5.5	V		1	PAST mod
V _{err} \alpha	Error on trip level	3.0	±20	-	-	-	-	1.1	mV	4.5 to 5.5		over V _{ref} range
V _{LL}	V _{IN} at which power for comparator is switched ON	0.4	0.7	0.9	0.4	0.9	0.4	0.9	V 001	4.5		Fig.9
V _{HH} 001	V _{IN} at which power for comparator is switched OFF	3.4	3.6	4.0	3.4	4.0	3.4	4.0	□ V	4.5		Fig.9
I _{cc}	active supply current. Comparator mode	3.0	2.0	3.4	-				mA	4.5		V _{rH} = 2.25 V V _{rL} = 0 V
Icc	supply current. PAST mode	-	30	50	-	-	-	-	μА	4.5		$V_{rH} = 3 V$ $V_{rL} = 1.5 V$
I _{cc}	quiescent supply current	4-5	en-	8	-	80	-	160	μА	4.5		$V_{rH} = V_{rL} = V_{CC}$ $V_{IN} = 0 V$

PAST mode

	Fig.17	4.5	an		Tamb (°C)	-	15 -			TES	T CONDITIONS
SYMBOL	PARAMETER	0.8	+25	-	-40	to +85	-40 to	0 +125	UNIT	V _{cc}	V,	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		(V)	(V)	3-Sizia C
14	HIGH reference	0.6	61).	Vcc	4.05	Vcc	1.05	Vcc	1,4	4.5	am	Percent Singular Communication of Commun
V _{rH}	level, (V _{T+})	1.05	-	V _{cc} - 1.20	1.05	- 1.20	1.05	V _{cc} - 1.20	V	to 5.5	n	
	LOW reference	0.2	86	Voc		Voc		Voc		4.5	titi:	rottenent surfluer
V _{rL}	level, (V _{T-})	1.00	-	V _{cc} - 1.25	1.00	- V _{cc} - 1.25	1.00	V _{cc} - 1.25	V	to 5.5		
	Minimum	0.6	SIT					1 9		4.5	SEVER S	MOT M
V _{Hmin}	hysteresis voltage, (V _{rH} - V _{rL})	0.0	50		-	-	Ť	Ē	mV	to 5.5		

COMPARATOR mode

	AF 6/3				T _{amb} (°							ST CONDITIONS													
SYMBOL	PARAMETER	ARAMETER +25 -40 to +85 -40 to +125 L		AMETER +25 -40 to +85 -40 to +125 UNIT	+25		+25		+25		+25		+25		-40 to +125		Vcc	V,	OTHER						
	1 = 1 = 1	MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		(V)	(V)	BUOTHER													
V_{rHmin}	minimum reference level	-	0.6	_	-	-	-	-	٧	4.5		over V _{ref} range													
V_{rHmax}	maximum reference level	_	V _{cc}	-	-	-	-	-	٧	4.5		over V _{ref} range													

Quad precision adjustable Schmitt-trigger/comparator with output latches; 74HC/HCT7132 3-state

AC CHARACTERISTICS FOR 74HCT

v a.					T _{amb} (°	C)	ooV	in South				ST C	ONDITIONS
SYMBOL	PARAMETER		+25		-40 1	0 +85	-40 to	0 +125	UNIT	Vcc	· ·	V	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		(V)	V _{rH}	V _{rL}	WAVEFORING
t _{PHL}	propagation delay V _{inn} to Q _n ; PAST mode	10%	50	-	um <u>u</u> o ,	0 _	-	-	ns	4.5	3.00	1.50	Fig.13, t _r = 100 ns/V
t _{PLH}	propagation delay V _{inn} to Q _n ; PAST mode	stron don e	50 ₁₀	va₩ i	t.ga outpu	-	-	of C _m V abom T	ns	231.0	3.00	1.50	Fig.13, t _f = 100 ns/V
t _{PHL}	propagation delay V _{inn} to Q _n ; Comparator mode	AV AV	60	Jugi	go.V		-	-	ns	4.5	V _{cc} /2	0.00	Fig.14, overdrive: 100 m
t _{PLH}	propagation delay V _{inn} to Q _n ; Comparator mode	-	50	- Jugo	- 31		1-1	7	ns	4.5	V _{cc} /2	0.00	Fig.14, overdrive: 100 m
t _{PHL} /t _{PLH}	propagation delay LE to Q	vorta :	28	ivisVV a	Fig.1	-	-	of (3.1	ns	4.5	primo	de er	Fig.15
t _{PZH} /t _{PZL}	3-state output enable time OE to Qn	nai V	20	nii bio	I DAS	_	-	lofened -	ns	4.5	(aleta	houar	Fig.17 .ebom
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Qn	/10 = /10 = /V	22	=	HGT:	(† <u>)</u>	-	-	ns	4.5		aroe \	Fig.17
t _{THL} /t _{TLH}	output transition time	-	10	-	-	-	-	-	ns	4.5		JAN S	Fig.13
t _w	LE pulse width LOW	-	6	-	-	-	-	-	ns	4.5	1038		Fig.15
t _{su}	set-up time V _{inn} to LE	-	25	-	-	-		(1)	ns	4.5	3.00	1.50	Fig.16, for V_{INn} : $t_r = t_f = 180 \text{ ns}$
t _h	hold time V _{inn} to LE	-	-25	_	-	_	- 151	ustuo_ ida ne	ns	4.5	3.00	1.50	Fig.16, for V_{INn} : $t_r = t_f = 180 \text{ ns}$

AC WAVEFORMS

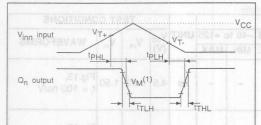


Fig.13 Waveforms showing the input (Vinn) to output Q propagation delays for PAST mode.

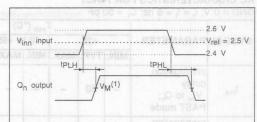


Fig.14 Waveforms showing the input (V_{inn}) to output Q propagation delays for Comparator mode at $V_{cl} = 0 \text{ V}$ and $V_{rel} = \frac{1}{2}V_{CC}$.

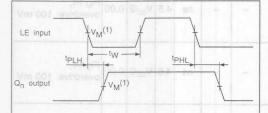


Fig.15 Waveforms showing the input (LE) to output Q_n propagation delays for Comparator mode.

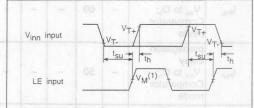
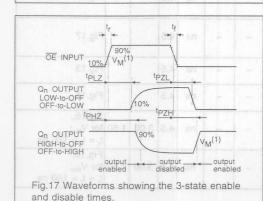


Fig.16 Waveforms showing the input set-up and hold times for $V_{\rm inn}$ input to LE input.



OCTAL BUS SCHMITT-TRIGGER TRANSCEIVER: 3-STATE

FEATURES

- Octal bidirectional bus interface
- Non-inverting 3-state outputs
- Output capability: bus driver
- · Icc category: MSI
- Schmitt-trigger action on all data inputs

GENERAL DESCRIPTION

The 74HC/HCT7245 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7245 are octal transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions.
The "7245" features and output enable:
(OE) input for easy cascading and a send/receive input (DIR) for direction control. OE controls the outputs so that the buses are effectively isolated. The 74HC/HCT7245 have Schmitt-trigger inputs. These inputs are capable of transforming slowly changing input signals into sharply defined jitter-free output signals.

The "7245" is identical to the "245" but has hysteresis on the data inputs.

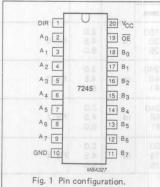
FUNCTION TABLE

An	Bn
A = B inputs	inputs B = A

H = HIGH voltage level L = LOW voltage level

X = don't care

Z = high impedance OFF-state



SYMBOL	DADAMETED	CONDITIONS	TY		
	PARAMETER	CONDITIONS	НС	нст	UNIT
tPHL/ tPLH	propagation delay An to Bn	C _L = 15 pF V _{CC} = 5 V	8	12	ns
CI	input capacitance	bnuorg) (IMD or b	3.5	3.5	pF
C _{I/O}	input/output capacitance		10	10	pF
C _{PD}	power dissipation capacitance per transceiver	notes 1 and 2	40	40	pF

GND = 0 V; Tamb = 25 °C; tr = tf = 6 ns

Notes and .mm .xam .qy2 .nim

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

 $PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$ where:

fi = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

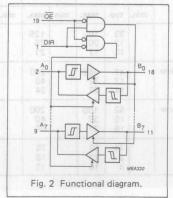
2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

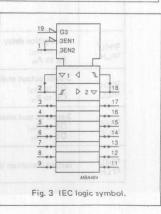
PACKAGE OUTLINES

20-lead DIL; plastic (SOT146). 20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₇	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B ₀ to B ₇	data inputs/outputs
19	ŌĒ	output enable input (active LOW)
74HC 02	Vcc	positive supply voltage





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are refered to GND (ground = 0 V)

	Life .		T _{amb} (°C)						branch of	TEST CONDITIONS		
	OB OB Come t anon		noiting sold toward 74HC							UNIT	Vcc	WAVEFORMS
31111	SYMBOL PARAMETER	+25 00 20		-40 to +85		-40 to +125		ni berilos	V	adi Aliftali 213		
		min.	typ.	max.	min.	max.	min.	max.	las	o sto 3	The 74HC/HCT724	
V _{T+}	W); roecite	positive-going threshold	elsayba ; (Cl. x s	ine cha c ft # 3 in ME	1.50 3.15 4.20	put fre CPD x seed to	1.50 3.15 4.20		1.50 3.15 4.20	V	2.0 4.5 6.0	Figs. 4 and 5
V _T _	V ni i	negative-going threshold	0.30 1.35 1.80	o mus V si i	edisibne	0.30 1.35 1.80	Cr HC	0.30 1.35 1.80	3.00	V	2.0 4.5 6.0	Figs. 4 and 5
VH		hysteresis ($V_{T+} - V_{T-}$)	0.1 0.25 0.3	0.2 0.4 0.5	LINES Itic (SC	0.1 0.25 0.3	SKAG cad Di	0.1 0.25 0.3		V	2.0 4.5 6.0	Figs. 4 and 5

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	data linguts/outputs			80 10	Tamb	(°C)	er l		2	TEST CONDITIONS	
SYMBOL	PARAMETER	74HC								tov	o spatiov WOJ = J
STIVIBUL	PARAMETER		+25		-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS
	The second secon	min.	typ.	max.	min.	max.	min.	max.			
tPHL/ tPLH	propagation delay A _n to B _n ; B _n to A _n		33 12 10	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t _{PZH} /	3-state output enable time OE to An; OE to Bn	U 0€	47 17 14	160 32 27	U	200 40 34		240 48 41	ns a	2.0 4.5 6.0	Fig. 7
^t PHZ/	3-state output disable time OE to An; OE to Bn	1	52 19 16	160 32 27	u +	200 40 34		240 48 41	ns an	2.0 4.5 6.0	Fig. 7
tTHL/ tTLH	output transition time	CATAG	14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A.,	0.33
Bn	0.33
OE	1.50
DIR	1.00

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are refered to GND (ground = 0 V)

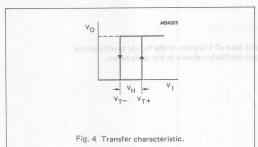
			T _{amb} (°C)							TEST CONDITIONS		
SYMBOL	242445752				74HC	т			LIAUT		WAVEFORMS	
	PARAMETER		+25		-40	to +85	-40 to	+125	UNIT	VCC V	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			Turner	
V _{T+}	positive-going threshold	1		2.0		2.0 2.1	s- 10,91	2.0 2.1	٧	4.5 5.5	Figs. 4 and 5	
V _T	negative-going threshold	0.7 0.8	WC3+2	WOJ 180	0.64 0.74		0.6 0.7		V	4.5 5.5	Figs. 4 and 5	
VH	hysteresis (V _{T+} – V _T _)	0.17 0.17	0.23 0.23	TUG - HORA		HJT -			٧	4.5 5.5	Figs. 4 and 5	

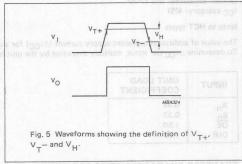
AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V; } t_r = t_f = 6 \text{ ns; } C_L = 50 \text{ pF}$

			T _{amb} (°C)							TEST CONDITIONS	
0)//4001		74HCT							V of GM		
SYMBOL	PARAMETER	+25		-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/ tPLH	propagation delay A _n to B _n ; B _n to A _n		17	30		37		45	ns	4.5	Fig. 6
tPZH/ tPZL	3-state output enable time OE to An; OE to Bn		19	32		40		48	ns	4.5	Fig. 7
tPHZ/ tPLZ	3-state output disable time OE to An; OE to Bn		19	32		40		48	ns	4.5	Fig. 7
tTHL/ tTLH	output transition time		5	12		15		18	ns	4.5	Fig. 6

TRANSFER CHARACTERISTIC WAVEFORMS OF "Moliferterbehalfs cliented and the Company of the Company





AC WAVEFORMS

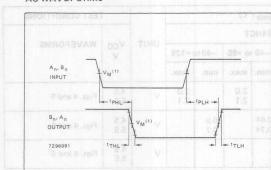


Fig. 6 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

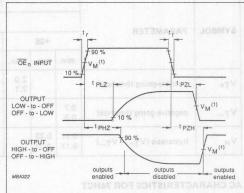


Fig. 7 Waveforms showing the 3-state enable and disable times.

QUAD 2-INPUT EXCLUSIVE-NOR GATE

FEATURES

- Output capability: standard
- ICC category: SSI

GENERAL DESCRIPTION

The 74HC7266 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC7266 provide the EXCLUSIVE-NOR function with active push-pull output.

CVMDOL	DADAMETER	CONDITIONS	TYPICAL	
SYMBOL	PARAMETER	CONDITIONS	НС	ns pF
tPHL/	propagation delay nA, nB to nY	C _L = 15 pF V _{CC} = 5 V	11	ns
CI	input capacitance		3.5	pF
C _{PD}	power dissipation capacitance per gate	note 1	17	pF

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD
$$\times$$
 VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

f; = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

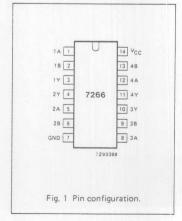
2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

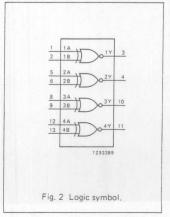
PACKAGE OUTLINES

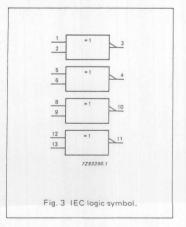
14-lead DIL; plastic (SOT27). 14-lead mini-pack; plastic (SO14; SOT108A).

PIN DESCRIPTION

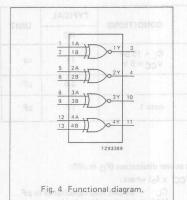
PIN NO.	SYMBOL	NAME AND FUNCTION	
1, 5, 8, 12	1A to 4A	data inputs	
2, 6, 9, 13	1B to 4B	data inputs	
3, 4, 10, 11	1Y to 4Y	data outputs	
7	GND	ground (0 V)	
14	Vcc	positive supply voltage	

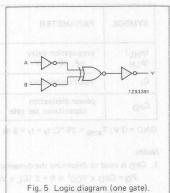










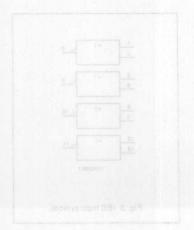


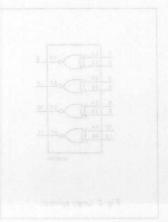
FUNCTION TABLE 23RUTA33

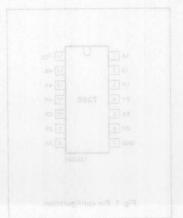
INP	UTS 122:	OUTPUT
nA Managara		30 JANY M35
L b	and Lord an	The 74HC7285 a
L nig a	vices Hd are	Si quite UMOS de
Historia	low pawer S	raw eld-regmo
H baiti	ange His year	T CONTROL T

H = HIGH voltage level
L = LOW voltage level

MOLTHEROZHO MIN







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Output capability: standard I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

				٦	amb (°C)				1	TEST CONDITIONS
SYMBOL	PARAMETER				74H0					.,	
STNIBOL	PARAMETER		+25	193	-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/ tPLH	propagation delay nA, nB to nY		39 14 11	115 23 20		145 29 25		175 35 30	ns	2.0 4.5 6.0	Fig. 6
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC WAVEFORMS

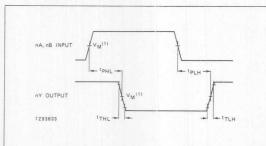


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} .

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "PCMOS family characteristics", section "Family specifications"

Output capability: standard

AC CHARACTERISTICS FOR 74HC

GWD = 0 V: $t_F = t_f = 8 \text{ ns; } C_1 = 80 \text{ pF}$

						EST CONDITIONS
					oov.	

AC WAVEFORMS

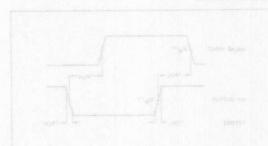


Fig. 6 Waveforms showing the input (nA. nB) to output (nY) propagation delays and the output transition times.

Vote to AC waveforms

1) HC: V_M = 80%; V₁ = GND to V_{CC}

74HC/HCT7403

FEATURES

- Synchronous or assynchronous operation
- · 3-state outputs
- 30 MHz (typical) shift-in and shift-out rates
- Readily expandable in word and bit dimensions
- Pinning arranged for easy board layout: input pins directly opposite output pins
- Output capability: driver (8 mA)
- I_{cc} category: LSI.

APPLICATIONS

- · High-speed disc or tape controller
- · Communications buffer.

GENERAL DESCRIPTION

The 74HC/HCT7403 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no.7A.

The "7403" is an expandable, First-In First-Out (FIFO) memory organized as 64 words by 4 bits. A guaranteed 15 MHz data-rate makes it ideal for high-speed applications. A higher data-rate can be obtained in applications where the status flags are not used (burst-mode).

With separate controls for shift-in (SI) and shift-out (\overline{SO}), reading and writing operations are completely independent, allowing synchronous and asynchronous data transfers. Additional controls include a master-reset input (\overline{MR}), an output enable input (\overline{OE}) and flags. The data-in-ready (DIR) and data-out-ready (DOR) flags indicate the status of the device.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25 \, ^{\circ}\text{C}$; $t_r = t_f = 6 \, \text{ns}$.

CVMDOL	DARAMETER	CONDITIONS	Т	YP.	UNIT
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
t _{PHL} /t _{PLH}	propagation delay SO, SI to DIR and DOR	C _L = 15 pF	15	17	ns
f _{max}	maximum clock frequency	V _{CC} = 5 V	30	30	MHz
Cı	input capacitance	p sunmoranousas	3.5	3.5	pF _
C _{PD}	power dissipation capacitance per package	note 1	475	490	pF ₀

Note

For HC the condition is V_1 = GND to V_{CC} . For HCT the condition is V_1 = GND to V_{CC} –1.5 V.

ORDERING INFORMATION

EXTENDED		PAC	KAGE	
TYPE NUMBER	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT7403N	16	DIL	plastic	SOT38Z
74HC/HCT7403D	16	SO16L	plastic	SOT162

74HC/HCT7403

PINNING

SYMBOL	PIN	DESCRIPTION
OEMU	1	output enable input (active LOW)
DIR	2	data-in-ready output
SI an	3 2	shift-in input (active HIGH)
Do to D ₃	4, 5, 6, 7	parallel data input
GND	8	ground
MR	9	assynchronous master-reset input (active LOW)
Q_3 to Q_0	10, 11, 12, 13	data output
DOR	14	data-out-ready output
SO	15	shift-out input (active LOW)
V _{cc}	16	positive supply voltage

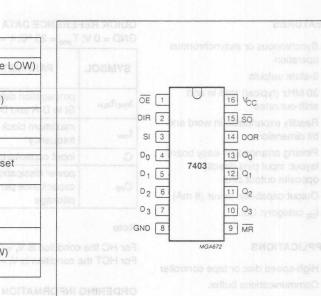


Fig.1 Pin configuration.

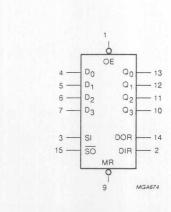
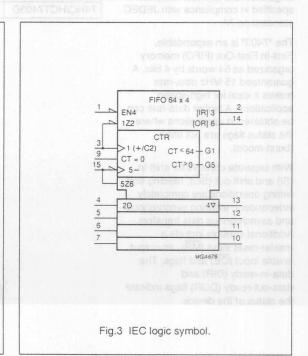
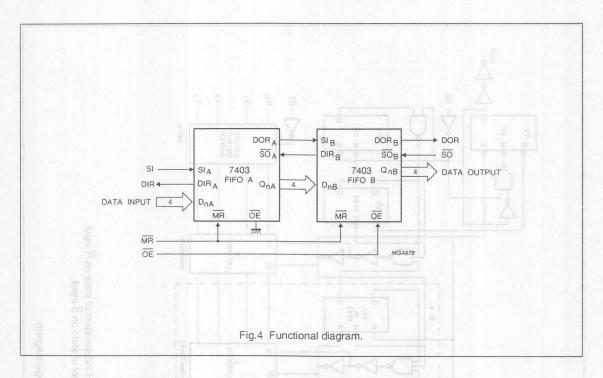


Fig.2 Logic symbol.



74HC/HCT7403



FUNCTIONAL DESCRIPTION

A DIR flag indicates the input stage status, either empty and ready to receive data (DIR = HIGH) or full and busy (DIR = LOW). When DIR and SI are HIGH, data present at D_0 to D_3 is shifted into the input stage; once complete DIR goes LOW. When SI is set LOW, data is automatically shifted to the output stage or to the last empty location. A FIFO which can receive data is indicated by DIR set HIGH.

A DOR flag indicates the output stage status, either data available (DOR = HIGH) or busy (DOR = LOW). When \overline{SO} and DOR are HIGH, data is available at the outputs (Q_0 to Q_3). When \overline{SO} is set LOW new data may be shifted into the output stage, once complete DOR is set HIGH.

Expanded format (see Fig.17)

The DOR and DIR signals are used to allow the "7403" to be cascaded. Both parallel and serial expansion is possible.

Serial expansion is only possible with typical devices.

Parallel expansion

Parallel expansion is accomplished by logically ANDing the DOR and DIR signals to form a composite signal.

Serial expansion

Serial expansion is accomplished by:

- tying the data outputs of the first device to the data inputs of the second device
- connecting the DOR pin of the first device to the SI pin of the second device
- connecting the SO pin of the first device to the DIR pin of the second device.

74HC/HCT7403

4-Bit \times 64-word FIFO register; 3-state

Philips Semiconductors

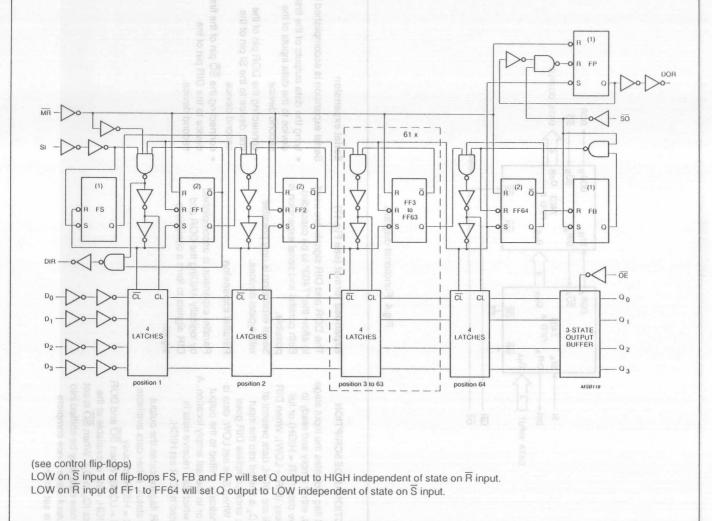


Fig.5 Logic diagram.

4-Bit × 64-word FIFO register;

74HC/HCT7403

3-state

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS Family Characteristics", section "Family specifications", except that V_{OH} and V_{OI} are not valid for driver output.

They are replaced by the values given below.

Output capability: driver 8 mA

Icc category: LSI.

Voltages are referenced to GND (ground = 0 V).

DC CHARACTERISTICS FOR 74HC

			an	240		T _{amb} (°	C)	160	52		T.	EST COND	ITION
SYMBOL	PARA	AMETER	en -	+25		-40	to +85	-40 to	+125	UNIT	V _{cc}	delay	OTLIED
	-		MIN	TYP	MAX	MIN	MAX	MIN	MAX		(V)	n V ₁ PM	OTHER
V _{OH}	HIGH outpu all out	t voltage	1.9 4.4 5.9	2.0 4.5 6		1.9 4.4 5.9		1.9 4.4 5.9	24 - 19 -	V V	2.0 4.5 6.0	V _{IH} or I _O =	–20 μΑ
V _{OH}		level t voltage outputs	3.98 5.48	4.32 5.81		3.84 5.34		3.70 5.20	34. 27.	V	4.5 6.0	Or	-8 mA -10 mA
V _{OL}	LOW outpu all out	t voltage	7.05 7.05	0 0	0.1 _ 0.1 _ 0.1	- 8 - 8	0.1 0.1 0.1	7 8.0 - 306 -	0.1 0.1 0.1	V V	2.0 4.5 6.0	V _{IH} or V _{IL} l _O =	20 μΑ
V _{OL}	1 .	level t voltage outputs	su	0.15 0.15	0.26 0.26	_ 18 _ 18	0.33	95 55	0.40 0.40	V	4.5 6.0		8 mA 10 mA
				2.1	-	1.8	-	1.4	2.2 0.8 0.6			delay/rippl through os SI to DOR	

74HC/HCT7403

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_i = 6$ ns; $C_L = 50$ pF.

					T _{amb} (°C	()		nugtuo ne	for driv	TES	TCONDITION
SYMBOL	PARAMETER		+25		-40 1	o +85	-40 to	+125	UNIT	V _{cc}	MANEEODM
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	Arn 8	(V)	WAVEFORMS
t _{PHL} /t _{PLH}	propagation delay MR to DIR, DOR	- - -	69 25 20	210 42 36	-	265 53 45	£V 0 ≈ - -	315 63 54	ns ns ns	2.0 4.5 6.0	Fig.8
t _{PHL}	propagation delay MR to Qn	- -THO -	52 19 15	160 32 27	- (6 -88+0	200 40 34	-	240 48 41	ns ns ns	2.0 4.5 6.0	Fig.8
t _{PHL} /t _{PLH}	propagation delay SI to DIR	- v - v	66 24 19	205 41 35		255 51 43		310 62 53	ns ns ns	2.0 4.5 6.0	Fig.6
t _{PHL} /t _{PLH}	propagation delay SO to DOR	- V	94 34 27	290 58 49	- 5	365 73 62		435 87 74	ns ns ns	2.0 4.5 6.0	Fig.9
t _{PHL} /t _{PLH}	propagation delay DOR to Q _n	- V	11 4 3	35 7 6.0	- 1.0 - 1.0	45 9 8	- t.0 - t.0 - t.0	55 11 9	ns ns ns	2.0 4.5 6.0	Fig.10
t _{PHL} /t _{PLH}	propagation delay SO to Q _n	- V	105 38 30	325 65 55	- 88,0 - 88,0	406 81 69	0.26 0.26	488 98 83	ns ns ns	2.0 4.5 6.0	Fig.14
t _{PLH}	propagation delay/ripple through delay SI to DOR	_ _ _	2.2 0.8 0.6	7 1.4 1.2	- - -	8.8 1.8 1.5	=	10.5 2.1 1.8	μs μs μs	2.0 4.5 6.0	Fig.10
t _{PLH}	propagation delay/bubble-up delay SO to DIR	- - -	2.8 1.0 0.8	9 1.8 1.5	-	11.2 2.2 1.9	-	13.5 2.7 2.3	μs μs μs	2.0 4.5 6.0	Fig.7
t _{PZH} /t _{PZL}	3-state output enable OE to Qn	- - -	44 16 13	150 30 26	- - -	190 38 32	- - -	225 45 38	ns ns ns	2.0 4.5 6.0	Fig.16
t _{PHZ} /t _{PLZ}	3-state output disable OE to Qn	- - -	50 18 14	150 30 26	- - -	190 38 33	_ _ _	225 45 38	ns ns ns	2.0 4.5 6.0	Fig.16
t _{THL} /t _{TLH}	output transition time	- - -	14 5 4	60 12 10	-	75 15 13	-	90 18 15	ns ns ns	2.0 4.5 6.0	Fig.16
t _w	SI pulse width HIGH or LOW	35 7 6.0	11 4 3	-	45 9 8	-	55 11 9	- - -	ns ns ns	2.0 4.5 6.0	Fig.6

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					T _{amb} (°C	;)			N MO-	TES	T CONDITION
SYMBOL	PARAMETER	Allering	+25	Suus, s	-40	to +85	-40 t	0 +125	UNIT	V _{cc}	or the DC chart
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	alues d	(V)	WAVEFORMS
t _w	SO pulse width HIGH or LOW	70 14 12	22 8 6.0	-	90 18 15	-	105 21 18	-	ns ns ns	2.0 4.5 6.0	Fig.9
t _w	DIR pulse width HIGH	10 5 4	41 15 12	130 26 22	8 4 3	165 33 28	8 4 3	195 39 33	ns ns ns	2.0 4.5 6.0	Fig.7
tw	DOR pulse width HIGH	14 7 6.0	52 19 15	160 32 27	12 6 5	200 40 34	12 6.0 5.0	240 48 41	ns ns ns	2.0 4.5 6.0	Fig.10
t _w	MR pulse width	120 24 20	39 14 11	<u>5</u> .5	150 30 26	4_4	180 36 31	-	ns ns ns	2.0 4.5 6.0	Fig.8
t _{rem}	removal time MR to SI	80 16 14	24 8 7	3.2	100 20 17	- 8_8	120 24 20	- - - 8	ns ns ns	2.0 4.5 6.0	Fig.15
t _{su}	set-up time D _n to SI	-8 -4 -3	-36 -13 -10	-	-6 -3 -3	-	-6 -3 -3	<u>-</u>	ns ns ns	2.0 4.5 6.0	Fig.13
t _h 8 =	hold time D _n to SI	135 27 23	44 16 13	-	170 34 29	- 8	205 41 35	-	ns ns ns	2.0 4.5 6.0	Fig.13
f _{max}	maximum clock pulse frequency SI, SO burst mode	3.6 18 21	9.9 30 36	- - ! load of	2.8 14 16	- - - (ool()) 1	2.4 12 14	- solite - solite	MHz MHz MHz	2.0 4.5 6.0	Figs 11 and 12
f _{max}	maximum clock pulse frequency SI, SO using flags	3.6 18 21	9.9 30 36	eiomeos - -	2.8 14 16	by the u	2.4 12 14	rii yigiili	MHz MHz MHz	2.0 4.5 6.0	Figs 6 and 9
f _{max}	maximum clock pulse frequency SI, SO cascaded	1 3-1 1-5 17.0	7.6 23 27	-	-	- - -	-	_ _ _	MHz MHz MHz	2.0 4.5 6.0	Figs 6 and 9

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS Family Characteristics", section "Family Specifications", except that V_{OH} and V_{OL} are not valid for driver output.

They are replaced by the values given below.

Output capability: driver 8 mA.

Icc category: LSI.

Voltages are referenced to GND (ground = 0 V).

DC CHARACTERISTICS FOR 74HCT

	0.5	en (\$1	T _{amb} (°C	12 (14	TE	EST CC	NOITION
SYMBOL	PARAMETER	ns	+25	0.8	-40 to +85		_40 to	o +125	UNIT	V _{cc}	dfbi	OTHER
	0.8	MIN	TYP	MAX	MIN	MAX	MIN	MAX	6.0	(V)	Viol	OTHER
V _{OH} 8	HIGH level output voltage all outputs	4.4	4.5	38	4.4	30	4.4	14	V ₀₈	4.5	V _{IH} or V _{IL}	I _O = -20 μA
V _{OH}	HIGH level output voltage driver outputs	3.98	4.32	24	3.84	20	3.7	8 7 -	16 14 14	4.5	V _{IH} or V _{IL}	$I_0 = -8 \text{ mA}$
V _{OL}	LOW level output voltage all outputs	an an	0	0.1	-	0.1		0.1	V ₈₋	4.5	V _{IH} or V _{IL}	Ι ₀ = 20 μΑ
V _{OL}	LOW level output voltage driver outputs	su su	0.15	0.26		0.33		0.4	V ₂₃ V	4.5	V _{IH} or V _{IL}	I _O = 8 mA

Notes to the HCT DC Characteristics

- 1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
- 2. To determine △I_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

UNIT LOAD COEFFICIENT

		INPUT			UNIT LOAD COEFFICIENT								
E LE LE	2.0	ŌĒ					7.6	1	salug xbolo				
Figs 6 and 9	4.5	SI	-	- 100		-	23	1.5	Irequency	max			
	U.6	Dn					12	0.75	181,80				
		MR						1.5	- Consome J				
		SO						1.5					

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AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t = t = 6 ns; C_1 = 50 pF$

	AW SOV TIM	67	1 + 01 01	68	T _{amb} (°C	C)	25		H2	TES	T CONDITION
SYMBOL	PARAMETER	AA	+25	N XA	-40	to +85	-40 t	o +125	UNIT	V _{cc}	MANTEODIA
	4.5 Fig	MIN	TYP	MAX	MIN	MAX	MIN	MAX	8	(V)	WAVEFORMS
	propagation									P	DIH
t _{PHL} /t _{PLH}	delay MR to DIR, DOR	<u>-</u>	30	51	A (53	- 88	63	ns	4.5	Fig.8
t _{PHL} 8	propagation delay MR to Q _n	2	22	38	-	48	-	57	ns	4.5	Fig.8
t _{PHL} /t _{PLH}	propagation delay SI to DIR	in i	25	43	-	54	- 8	65	ns	4.5	Fig.6
t _{PHL} /t _{PLH}	propagation delay SO to DOR	ia l	36	61	-	76	-	92	ns	4.5	Fig.9
t _{PHL} /t _{PLH}	propagation delay SO to Q _n	vī i	42	72	-	90	=	108	ns	4.5	Fig.14
t _{PHL} /t _{PLH}	propagation delay DOR to Q _n	-	7	12	-	15	-	18	ns	4.5	Fig.10
Q bns a c	propagation delay/ripple through delay SI to DOR	M	0.8	1.4	-	1.75	-	2.1	μs	4.5	Fig.10
t _{PLH}	propagation delay/bubble-up delay SO to DIR	M	1	1.8	-	2.25	=	2.7	μѕ	4.5	Fig.7
t _{PZH} /t _{PZL}	3-state output enable time OE to Qn	-	16	30	-	38	-	45	ns	4.5	Fig.16
t_{PHZ}/t_{PLZ}	3-state output disable time OE to Qn	-	19	30	-	38	-	45	ns	4.5	Fig.16
t _{THL} /t _{TLH}	output transition time	-	5	12	-	15	-	18	ns	4.5	Fig.16
t _w	SI pulse width HIGH or LOW	9	5	-	6	-	8	-	ns	4.5	Fig.6
t _w	SO pulse width HIGH or LOW	14	8	-	18	-	21	-	ns	4.5	Fig.9

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					T _{amb} (°C)		AHGT	0. = 50	TES	T CON	DITION
SYMBOL	PARAMETER		+25		-40 t	0 +85	-40 to	+125	UNIT	V _{cc}	MAN	EFORMS
	704	MIN	TYP	MAX	MIN	MAX	MIN	MAX	93	(V)	WAVE	EFORMS
t _w	DIR pulse width HIGH	5 XA	417 MH	29 XA	4 1/11	36 ^{XA}	4 97	44 MB	ns	4.5 notispec	Fig.7	
t _w	DOR pulse width HIGH	7	21	36	6.0	45	6.0	54	ns	4.5	Fig.10	لَفِيرِ الْمِيرِ
t _w	MR pulse width LOW	26	15	-	33	-	39	25	ns	4.5	Fig.8	Jed
t _{rem}	removal time MR to SI	18	10	-	23	-	27	-	ns	4.5	Fig.15	5
t _{su}	set-up time D _n to SI	-5	-16	-	-4	-	-4	-	ns	4.5	Fig.13	3 Flay/Hay
t _h	hold time D _n to SI	30	18	-	38	-	45	19	ns	4.5	Fig.13	Bust med
f _{max}	maximum clock pulse frequency SI, SO burst mode	18	30	-	14	-	12	4	MHz	4.5 of	UG	1 and 12
f _{max}	maximum clock pulse frequency SI, SO using flags	18	30	- 87	14	- 4	12	0	MHz	O of R	Figs 6	and 9
f _{max}	maximum clock pulse frequency SI, SO cascaded	ьц s	23	= 88	5	- 8		ī	MHz	A.5dW	Figs 6	and 9
81	4.5 Fig.	an	45		80	- (30	81	- 10	ate outp ble time to Q _n		1241/HZq1

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AC WAVEFORMS

Shifting in sequence FIFO empty to FIFO full

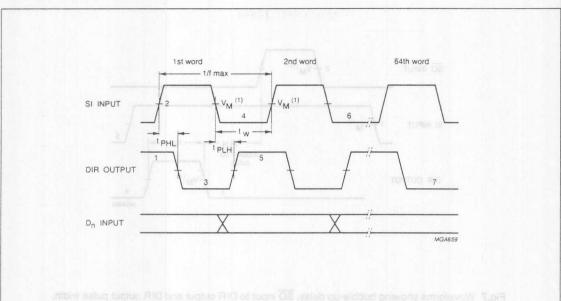
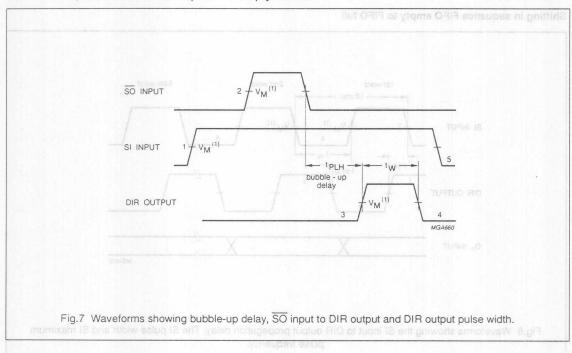


Fig.6 Waveforms showing the SI input to DIR output propagation delay. The SI pulse width and SI maximum pulse frequency.

- 1. DIR initially HIGH; FIFO is prepared for valid data
- 2. SI set HIGH; data loaded into input stage
- 3. DIR goes LOW, input stage "busy"
- 4. SI set LOW; data from first location "ripple through"
- 5. DIR goes HIGH, status flag indicates FIFO prepared for additional data
- Repeat process to load 2nd word through to 64th word into FIFO DIR remains LOW; with attempt to shift into full FIFO, no data transfer occurs.

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With FIFO full; SI held HIGH in anticipation of empty location



- 1. FIFO is initially full, shift-in is held HIGH
- 2. SO pulse; data in the output stage is unloaded, "bubble-up" process of empty location begins thou will be a stage of the stage of th
- 3. DIR HIGH; when empty location reaches input stage, flage indicates FIFO is prepared for data input HOIH 198 IS US
- 4. DIR returns to LOW; data shift-in to empty location is complete, FIFO is full again and application would see Alia .
- 5. SI set LOW; necessary to complete shift-in process, DIR remains LOW, because FIFO is full.

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Master reset applied with FIFO full

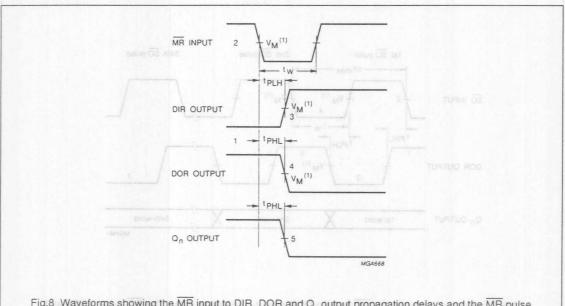
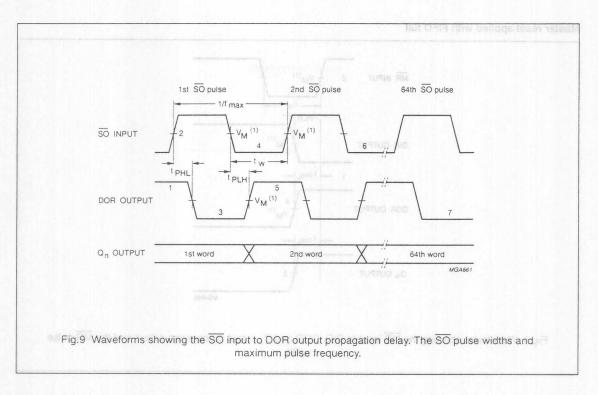


Fig.8 Waveforms showing the $\overline{\text{MR}}$ input to DIR, DOR and Q_n output propagation delays and the $\overline{\text{MR}}$ pulse width.

- 1. DIR LOW, output ready HIGH; assume FIFO is full Insecting at all billing assume FIFO is full Insecting at all billing assume FIFO is full Insecting at all billing assume FIFO is full Insecting at all billing assume FIFO is full Insecting at all billing assume FIFO is full Insecting at all billing assume FIFO is full Insecting at all billing assume FIFO is full Insecting at all billing assume FIFO is full Insecting at all billing assume FIFO is full Insecting at all billing assume FIFO is full Insecting at all billing assume FIFO is full Insecting at all billing assume FIFO is full Insecting at all billing at al
- 2. MR pulse LOW; clears FIFO
- 3. DIR goes HIGH; flag indicates input prepared for valid data
- 4. DOR goes LOW; flag indicates FIFO empty sign slab wen bits abbasing at spate tright and in stab two 142 OR 4.
- 5. Q_n outputs go LOW (only last bit will be reset).
 - ORIG most force of the act of department and beautiful at several partment from EIPO
 - Ultimo di CEIE VVC Lamento, CCC T

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- 1. DOR HIGH; no data transfer in progress, valid data is present at output stage was MDIH visser fuglish WOJ RIG IT
- 2. SO set HIGH; results in DOR going LOW
- 3. DOR goes LOW; output stage "busy"
- 4. SO set LOW; data in the input stage is unloaded, and new data replaces it as empty location "bubbles-up" to input stage
- 5. DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay
- 6. Repeat process to unload the 3rd through to the 64th word from FIFO
- 7. DOR remains LOW; FIFO is empty.

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With FIFO empty; SO is held HIGH in anticipation

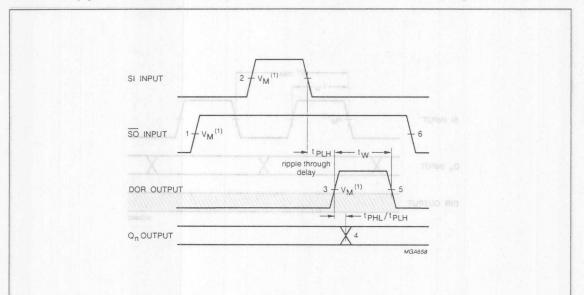
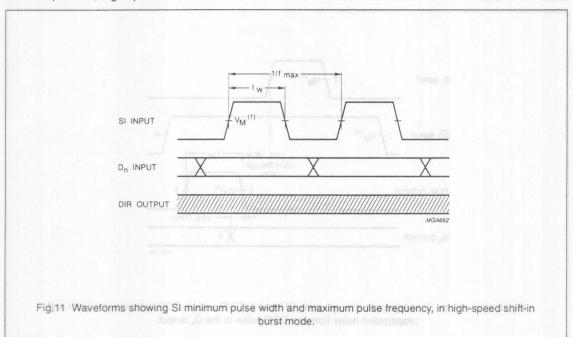


Fig.10 Waveforms showing ripple through delay SI input to DOR output, DOR output pulse width and propagation delay from the DOR pulse to the Q_n output.

- 1. FIFO is initially empty, SO is held HIGH
- 2. SI pulse; loads data into FIFO and initiates ripple through process and model and model and an arrangement of the second and initiates ripple through process and model are second and initiates ripple through process.
- 3. DOR flag signals the arrival of valid data at the output stages ORIR and to villages agencia and wolhavo bluow nointw
- 4. Output transition; data arrives at output stage after the specified propagation delay between the rising edge of the DOR pulse to the Q_n output
- 5. DOR goes LOW; data shift-out is complete, FIFO is empty again
- 6. SO set LOW; necessary to complete shift-out process. DOR remains LOW, because FIFO is empty.

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Shift-in operation; high-speed burst mode



Note to Fig.11

In the high-speed mode, the burst-in rate is determined by the minimum shift-in HIGH and shift-in LOW specifications. The DIR status flag is a don't care condition, and a shift-in pulse can be applied regardless of the flag. A SI pulse which would overflow the storage capacity of the FIFO is ignored.

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Shift-out operation; high-speed burst mode

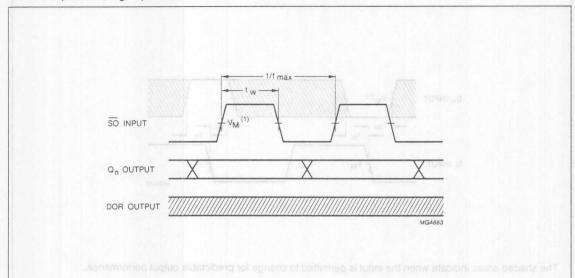
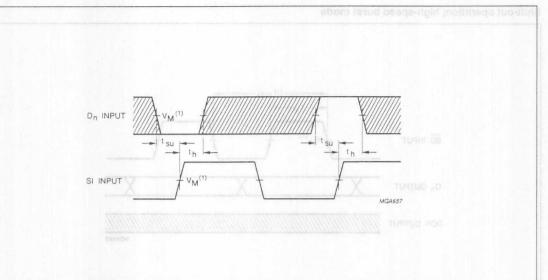


Fig.12 Waveforms showing SO minimum pulse width and maximum pulse frequency, in high-speed shift-out burst mode.

Note to Fig.12

In the high-speed mode, the burst-out rate is determined by the minimum shift-out HIGH and shift-out LOW specifications. The DOR flag is a don't care condition and an \overline{SO} pulse can be applied without regard to the flag.

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The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 13 Waveforms showing hold and set-up times for D_n input to SI input.

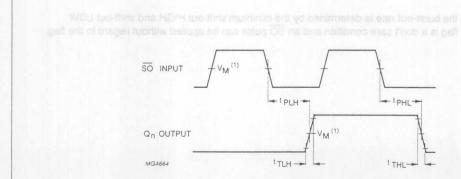
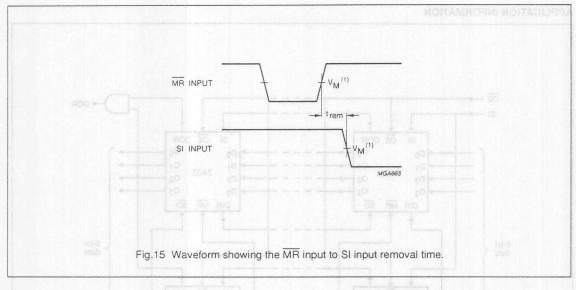
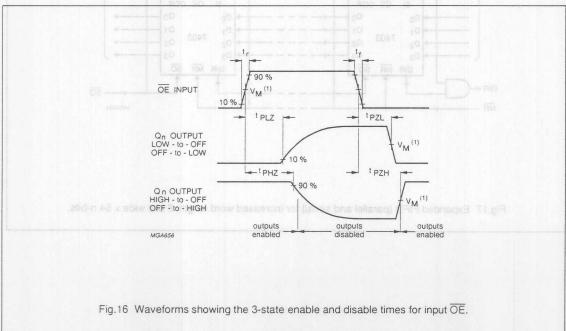


Fig.14 Waveforms showing \overline{SO} input to Q_n output propagation delays and output transition time.

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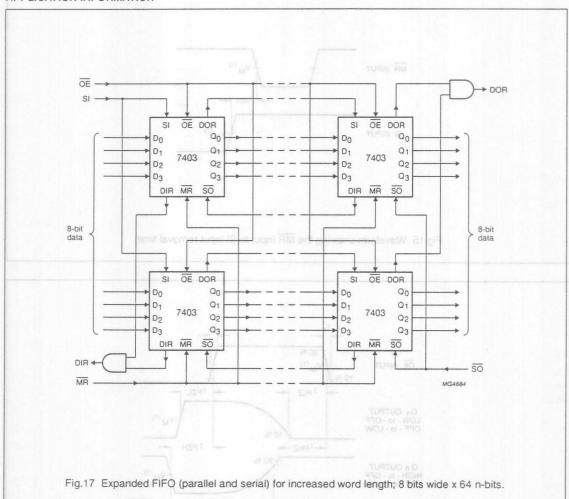


Note to AC waveforms

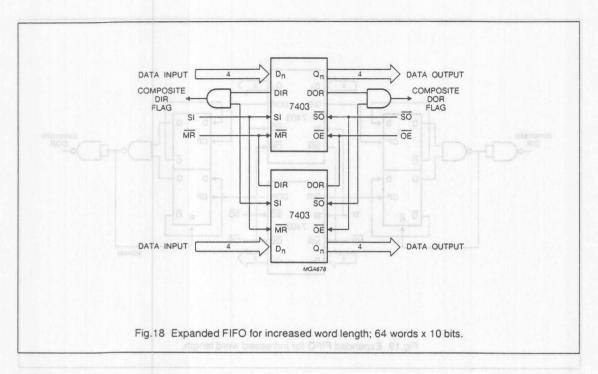
HC : VM = 50%; V_1 = GND to V_{CC} . HCT: VM = 1.3 V; V_1 = GND to 3 V.

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APPLICATION INFORMATION



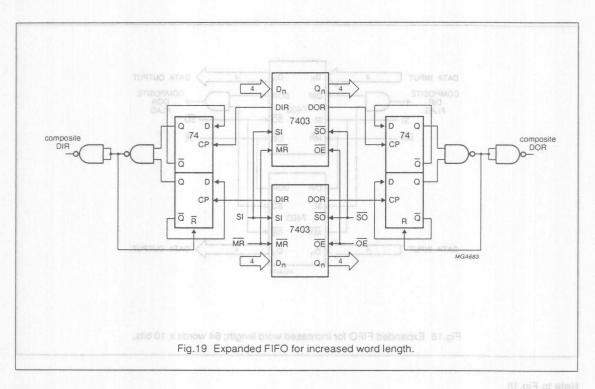
74HC/HCT7403



Note to Fig.18

The "7403" is easily expanded to increase word length. Composite DIR and DOR flags are formed with the addition of an AND gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.

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Note to Fig.19

This circuit is only required if the SI input is constantly held HIGH, when the FIFO is empty and the automatic shift-in cycles are started or if \overline{SO} output is constantly held HIGH, when the FIFO is full and the automatic shift-out cycles are started (see Figs 7 and 10).

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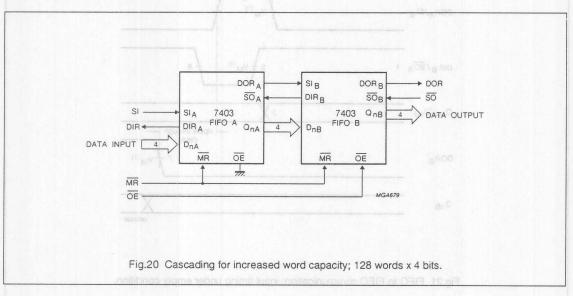
Expanded format

Figure 20 shows two cascaded FIFOs providing a capacity of 128 words x 4 bits. Figure 21 shows the signals on the nodes of both FIFOs after the application of a SI pulse, when both FIFOs are initially empty. After a ripple through delay, data arrives at the output of FIFO_ $\!_{A}$. Due to $\overline{SO}_{\!_{A}}$ being HIGH, a DOR $_{\!_{A}}$ pulse is generated. The requirements of SI $_{\!_{B}}$ and D $_{\!_{BB}}$ are

satisfied by the DOR_A pulse width and the timing between the rising edge of DOR_A and Q_nA . After a second ripple through delay, data arrives at the output of FIFO_B .

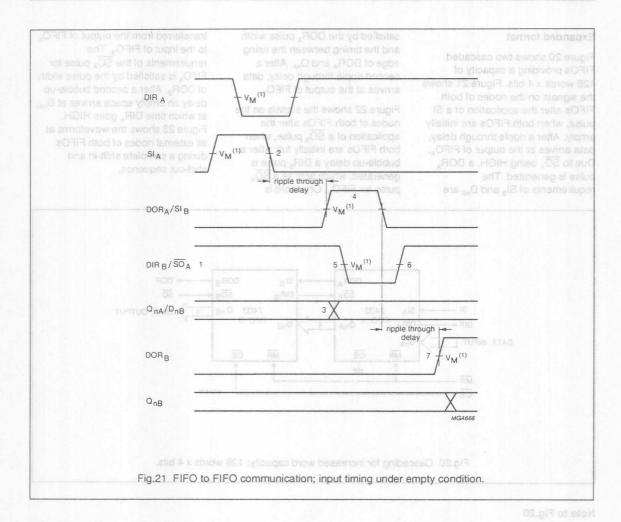
Figure 22 shows the signals on the nodes of both FIFOs after the application of a \overline{SO}_B pulse, when both FIFOs are initially full. After a bubble-up delay a DIR_B pulse is generated, which acts as a \overline{SO}_A pulse for FIFO_A. One word is

transferred from the output of FIFO_A to the input of FIFO_B. The requirements of the $\overline{\text{SO}}_{\text{A}}$ pulse for FIFO_A is satisfied by the pulse width of DOR_B. After a second bubble-up delay an empty space arrives at D_{nA}, at which time DIR_A goes HIGH. Figure 23 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.



Note to Fig.20

The "7404" is easily cascaded to increase word capacity without any external circuitry. In cascaded format, all necessary communications are handled by the FIFOs. Figures 21 and 22 demonstrate the intercommunication timing between FIFO_A and FIFO_B. Figure 23 provides an overview of pulses and timing of two cascaded FIFOs, when shifted full and shifted empty again.

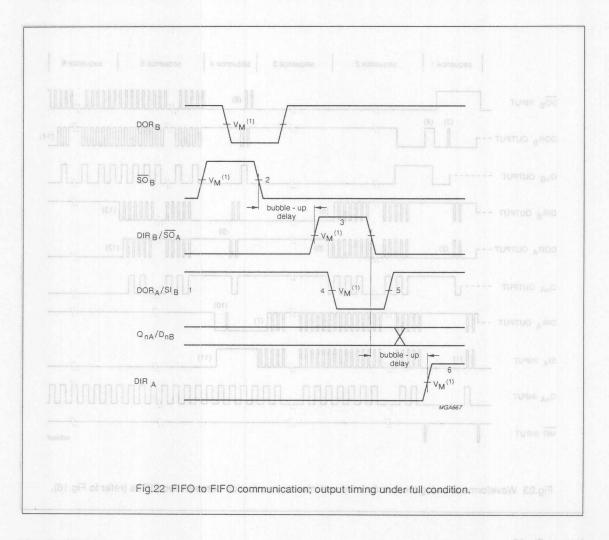


Notes to Fig.21 not debagas in crouter. In cascaded for Williams to Fig.21 not debagas and crowden in the Fig.21 not debagas and crowden in the Fig.21 not debagas and crowden in the Fig.21 not debagas and crowden in the Fig.21 not debagas and crowden in the Fig.21 not debagas and crowden in the Fig.21 not debagas and crowden in the Fig.21 not debagas and crowden in the Fig.21 not debagas and crowden in the Fig.21 not debagas and crowden in the Fig.21 not debagas and crowden in the Fig.22 not debagas and crowden in the Fi

- 1. ${\sf FIFO_A}$ and ${\sf FIFO_B}$ initially empty, $\overline{\sf SO_A}$ held HIGH in anticipation of data
- 2. Load one word into FIFO_A; SI pulse applied, results in DIR pulse
- Data-out Adata-in B transition; valid data arrives at FIFOA output stage after a specified delay of the DOR flag, meeting data input set-up requirements of FIFOB
- DOR_A and SI_B pulse HIGH; (ripple through delay after SI_A LOW) data is unloaded from FIFO_A as a result of the data output ready pulse, data is shifted into FIFO_B
- DIR_B and SO_A go LOW; flag indicates input stage of FIFO_B is busy, shift-out of FIFO_A is complete
- DIR_B and SO_A go HIGH automatically; the input stage of FIFO_B is again able to receive data, SO is held HIGH in anticipation of additional data
- DOR_B goes HIGH; (ripple through delay after SI_B LOW) valid data is present one propagation delay later at the FIFO_B output stage.

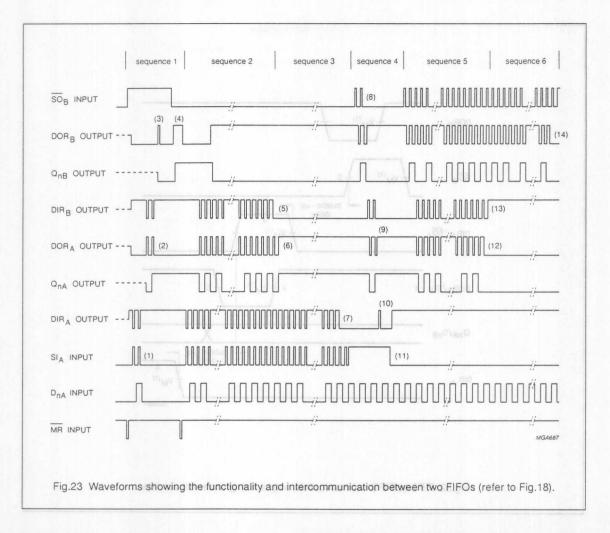
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- 1. FIFO_a and FIFO_B initially full, SI_B held HIGH in anticipation of shifting in new data as an empty location bubbles-up
- 2. Unload one word from FIFO_B; $\overline{\text{SO}}$ pulse applied, results in DOR pulse beautiful paigns used and salug $\overline{\text{RM}}$ a 15 $\overline{\text{RA}}$
- 3. DIR_B and \overline{SO}_A pulse HIGH; (bubble-up delay after \overline{SO}_B LOW) data is loaded into FIFO_B as a result of the DIR pulse, data is shifted out of FIFO_A
- 4. DOR_A and SI_B go LOW; flag indicates the output stage of $FIFO_A$ is busy, shift-in to $FIFO_B$ is complete
- DOR_A and SI_B go HIGH; flag indicates valid data is again available at FIFO_A output stage, SI_B is held HIGH, awaiting bubble-up of empty location
- DIR_A goes HIGH; (bubble-up delay after SO_A LOW) an empty location is present at input stage of FIFO_A.

74HC/HCT7403



Note to Fig.23

Sequence 1 (both FIFOS empty, starting SHIFT-IN process) with an HOH blant all all of villation and HOH blant all all of villation and HOH blant all all of villations and HOH blant all all of villations and HOH blant all all of villations and HOH blant all all of villations and HOH blant all all of villations and HOH blant all all of villations and HOH blant all all of villations and HOH blant all all of villations are set of villations and villations and HOH blant all all of villations are set of villations and villations are set of villations are set of villations and villations are set of villations and villations are set of villations are set of villations are set of villations are set of villations are set of villations are set of villations are set of villations are set of villations are set of villations are set of villations are set of villations are set of villations are set of

After a $\overline{\text{MR}}$ pulse has been applied FIFO_A and FIFO_B are empty. The DOR flags of FIFO_A and FIFO_B go LOW due to no valid data being present at the outputs. The DIR flags are set HIGH due to the FIFOs being ready to accept data. $\overline{\text{SO}}_{\text{B}}$ is held HIGH and two SI_A pulses are applied (1). These pulses allow two data words to ripple through to the output stage of FIFO_A and to the input stage of FIFO_B (2). When data arrives at the output of FIFO_B, a DOR_B pulse is generated (3). When $\overline{\text{SO}}_{\text{B}}$ goes LOW, the first bit is shifted out and a second bit ripples through to the output after which DOR_B goes HIGH (4).

74HC/HCT7403

Sequence 2 (FIFO_B runs full)

After the $\overline{\text{MR}}$ pulse, a series of 64 SI pulses are applied. When 64 words are shifted in, DIR_B remains LOW due to FIFO_B being full (5). DOR_A goes LOW due to FIFO_A being empty.

Sequence 3 (FIFO, runs full)

When 65 words are shifted in, DOR_A remains HIGH due to valid data remaining at the output of FIFO_A. Q_{nA} remains HIGH, being the polarity of the 65th data word (6). After the 128th SI pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

Squence 4 (both FIFOs full, starting SHIFT-OUT process)

 SI_A is held HIGH and two \overline{SO}_B pulses are applied (8). These pulses shift out two words and thus allow two empty locations to bubble-up to the input stage of $FIFO_B$, and proceed to $FIFO_A$ (9). When the first empty location arrives at the input of $FIFO_A$, a DIR_A pulse is generated (10) and a new word is shifted into $FIFO_A$. SI_A is made LOW and now the second empty location reaches the input stage of $FIFO_A$, after which DIR_A remains HIGH (11).

Sequence 5 (FIFO, runs empty)

At the start of sequence 5 FIFO_A contains 63 valid words due to two words being shifted out and one word being shifted in, in sequence 4. An additional series of \overline{SO}_B pulses are applied. After 63 \overline{SO}_B pulses, all words from FIFO_A are shifted into FIFO_B. DOR_A remains LOW (12).

Sequence 6 (FIFO_B runs empty)

After the next \overline{SO}_B pulse, DIR_B remains HIGH due to the input stage of FIFO_B being empty. After another 63 \overline{SO}_B pulses, DOR_B remains LOW due to both FIFOs being empty (14). Additional \overline{SO}_B pulses have no effect. The last word remains available at the output Q_n.

4-Bit × 64-word FIFO register;

74HC/HCT7403

Sequence 2 (FIFO, runs full)

After the MR pulse, a series of 64 SI pulses are applied, When 64 words are shifted in, DIR_e remains LOW due to RFO₂ being full (6), DOR, goes LOW due to RFO₂ being empty.

Sequence 3 (FIFO, runs full)

When 65 words are shifted in, DOR, remains HIGH due to valid data remaining at the output of FIFOs. O_M remains HIGH, being the polarity of the 65th data word (6). After the 128th SI pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

Squarce 4 (both FIFOs full, starting SHIFT-OUT process)

 SI_{λ} is held HIGH and two \overline{SO}_{0} pulses are applied (8). These pulses thift out two words and thus allow two empty locations to bubble-up to the input stage of FIFO $_{0}$, and proceed to FIFO $_{\lambda}$ (9). When the first empty location arrives at the input of FIFO $_{\lambda}$, a DIR, pulse is generated (10) and a new word is shifted into FIFO $_{\lambda}$. SI_{λ} is made LOW and now the second arripty location reaches the input stage of FIFO $_{\lambda}$, after which DIR, remains HIGH (11).

Sequence 5 (FIFO, runs empty)

At the start of sequence 5 FIFO_a contains 83 valid words due to two words being shifted out and one word being shifted in, in sequence 4. An additional series of \overline{SO}_8 pulses are applied. After 63 \overline{SO}_8 pulses, all words from FIFO_a are shifted into FIFO_a. DOR_a remains LOW (12).

Sequence 6 (FIPO_e runs empty)

After the next SO₃ pulse, DIR, remains HIGH due to the input stage of FIFO₅ being empty. After another 63 SO₃ pulses, DOR₅ remains LOW due to both FIFOs being empty (14). Additional SO₃ pulses have no effect. The last word remains available at the output Q₂.

5-Bit × 64-word FIFO register; 3-state and a register of 174HC/HCT7404

FEATURES

- · Synchronous or assynchronous operation
- · 3-state outputs
- . 30 MHz (typical) shift-in and shift-out rates
- · Readily expandable in word and bit dimensions
- · Pinning arranged for easy board layout: input pins directly opposite output pins
- Output capability: driver (8 mA)
- · Icc category: LSI.

APPLICATIONS

- High-speed disc or tape controller
- Communications buffer.

GENERAL DESCRIPTION

The 74HC/HCT7404 are high-speed Si-gate CMOS devices specified in compliance with JEDEC standard no.7A.

The "7404" is an expandable, First-In First-Out (FIFO) memory organized as 64 words by 5 bits. A guaranteed 15 MHz data-rate makes it ideal for high-speed applications. A higher data-rate can be obtained in applications where the status flags are not used (burst-mode).

With separate controls for shift-in (SI) and shift-out (SO). reading and writing operations are completely independent, allowing synchronous and asynchronous data transfers. Additional controls include a master-reset input (MR), an output enable input (OE) and flags. The data-in-ready (DIR) and data-out-ready (DOR) flags indicate the status of the device.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_t = t_t = 6 ns.

01/11/201	Dipaueren	CONDITIONS	T	YP.	LINUT
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
t _{PHL} /t _{PLH}	propagation delay SO, SI to DIR and DOR	C _L = 15 pF	15	17	ns
f _{max}	maximum clock frequency	V _{CC} = 5 V	30 8	30	MHz
Cı	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	note 1	475	490	pF

Note

For HC the condition is $V_1 = GND$ to V_{CC} . For HCT the condition is $V_1 = GND$ to $V_{CC} - 1.5 \text{ V}$.

ORDERING INFORMATION

EXTENDED		PAC	KAGE	
TYPE NUMBER	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT7404N	18	DIL	plastic	SOT102
74HC/HCT7404D	20	SO20	plastic	SOT163A

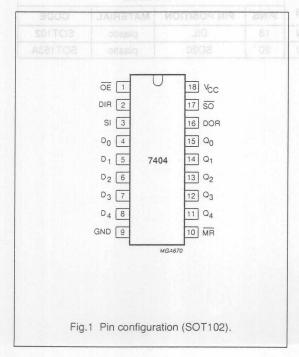
5-Bit × 64-word FIFO register; 3-state 74HC/HCT7404

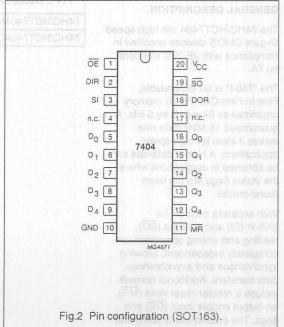
PINNING (SOT102)

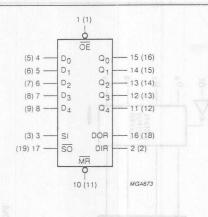
SYMBOL	PIN	DESCRIPTION
ŌĒ	1	output enable input (active LOW)
DIR	2	data-in-ready output
SI	3	shift-in input (active HIGH)
Do to D ₄	4, 5, 6, 7, 8	parallel data inputs
GND	9	ground
MR	10	assynchronous master-reset input (active LOW)
Q ₄ to Q ₀	11, 12, 13, 14, 15	data outputs
DOR	16	data-out-ready output
SO	17	shift-out input (active LOW)
V _{cc}	18	positive supply voltage

PINNING (SOT163A)

SYMBOL	PIN	DESCRIPTION TOTAL
OE JOSM	re 1	output enable input (active LOW)
DIR	2	data-in-ready output
SI	3	shift-in input (active HIGH)
n.c.	4	not connected
D ₀ to D ₄	5, 6, 7, 8, 9	parallel data inputs
GND	10	ground
MR) 11 Dead 11	Assynchronous master-reset input (active LOW)
Q ₄ to Q ₀	12, 13, 14, 15, 16	data outputs ARA Whopened and a
n.c.	17	not connected
DOR	18	data-out ready output
n.c. DAIRE	19019	not connected 19/00/100
V _{cc}	20	positive supply voltage

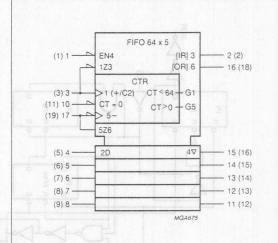






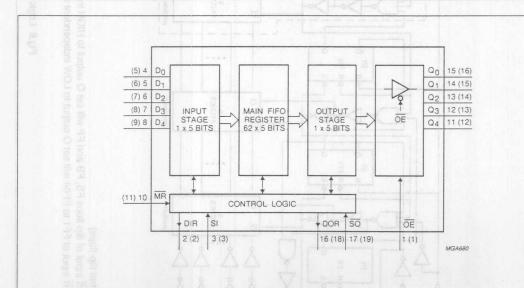
Pin numbers between parentheses refer to the SO package.

Fig.3 Logic symbol.



Pin numbers between parentheses refer to the SO package.

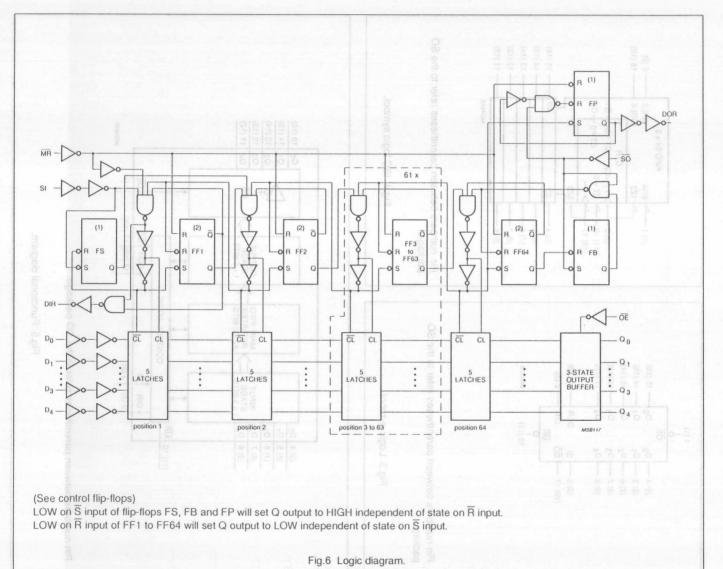
Fig.4 IEC logic symbol.



Pin numbers between parentheses refer to the SO package.

Fig.5 Functional diagram.

Philips Semiconductors



5-Bit × 64-word FIFO register; 3-state elsia-8 metalger OFI 74HC/HCT7404

FUNCTIONAL DESCRIPTION

The DIR flag indicates the input stage status, either empty and ready to receive data (DIR = HIGH) or full and busy (DIR = LOW). When DIR and SI are HIGH, data present at Do to Da is shifted into the input stage; once complete DIR goes LOW. When SI is set LOW, data is automatically shifted to the output stage or to the last empty location. A FIFO which can receive data is indicated by DIR set HIGH.

A DOR flag indicates the output stage status, either data available (DOR = HIGH) or busy (DOR = LOW). When SO and DOR

are HIGH, data is available at the outputs (Qo to Q4). When SO is LOW new data may be shifted into the output stage, once complete DOR is set LOW.

Expanded Format (see Fig.18)

The DOR and DIR signals are used to allow the "7404" to be cascaded. Both parallel and serial expansion is possible. Serial expansion is only possible with typical devices.

Parallel Expansion

Parallel expansion is accomplished by logically ANDing the DOR and

DIR signals to form a composite signal. = 0 v; t = t = 6 ns; 0 = 0MD

Serial Expansion

Serial expansion is accomplished by:

- tying the data outputs of the first device to the data inputs of the second device
- connecting the DOR pin of the first device to the SI pin of the second device
- connecting the SO pin of the first device to the DIR pin of the second device.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS Family Characteristics", section "Family Specifications".

Output capability: parallel outputs, bus driver; serial output, standard I_{CC} category: MSI

Output capability: driver 8 mA Icc category: LSI

Voltages are referenced to GND (ground = 0 V).

DC CHARACTERISTICS FOR 74HC

SYMBOL PARAMETE	o.e	T _{amb} °C						3.0	TEST CONDITION			
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{cc}	n V. DSO	OTHER
	2.0	MIN	TYP	MAX	MIN	MAX	MIN	MAX	2.8	(V)	u-elddud\va	OTHER
V _{OH}	HIGH level output voltage	3.98 5.48	4.32 5.81	1	3.84 5.34	L T	3.70 5.20	er ,	V	4.5 6	V _{IH} or AIG of V _{IC} ALO AIS	$l_0 = -8 \text{ mA}$ $l_0 = -10 \text{ mA}$
V _{OL}	LOW level output voltage	= 21 = 21	0.15 0.15	0.26 0.26	-	0.33 0.33	=	0.4	V V	4.5	V _{IH} SId. or V _{IL} SID.	l ₀ = 8 mA l ₀ = 10 mA

5-Bit × 64-word FIFO register; 3-state state-8 metalger ORI-74HC/HCT7404

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_t = t_t = 6$ ns; $C_t = 50$ pF. 2 2 OZ nerW $(t_t \odot O \circ t_t \odot O)$ stugting

	noisana	edal Es	2	otni bet	T _{amb} °C	in abst	o wen v autoutus	ani	ybsali	TEST C	ONDITION
SYMBOL	PARAMETER	eva recia	+25			to +85	-40 t	0+125	UNIT	ON VCC/O	MAVEFORMS
	lo atuatua eteb e	MIN	TYP	MAX	MIN	MAX	MIN	MAX	is I	3897(V)	WAVEFORMS
t _{PHL} /t _{PLH}	propagation delay MR to DIR, DOR	device second connection	69 25 20	210 42 36	signata to be ta irial exp		E-ROG ant woi altanag i	315 63 54	ns ns ns	2.0 4.5 6.0	rice once com Fig.9. W. WO
t _{PHL}	propagation delay MR to Q _n	second connec	52 19 15	160 32 27	device	200 40 34	lbw eldi	240 48 41	ns ns ns	2.0 4.5 6.0	Fig.9
t _{PHL} /t _{PLH}	propagation delay	second -	66 24 19	205 41 35	s accon the DQ	255 51 43	utel exp	310 62 53	ns ns ns	2.0 4.5 6.0	Fig.7 1 818 908
t _{PHL} /t _{PLH}	propagation delay SO to DOR	- - -	94 34 27	290 58 49	-	365 73 62	-	435 87 74	ns ns ns	2.0 4.5 6.0	Fig.10 AHO 0
t _{PHL} /t _{PLH}	propagation delay DOR to Q _n	SI - SI -	11 4 3	35 7 6.0	racteris tandard	45 9 8	Seriel	55 11 9	ns ns ns	2.0 4.5 6.0	Fig.11 s rugio
t _{PHL} /t _{PLH}	propagation delay SO to Q _n	_	105 38 30	325 65 55	-	406 81 69	- - (V	488 98 83	ns ns ns	2.0 4.5 6.0	Fig.15
t _{PLH} MO	propagation delay/ripple through delay SI to DOR	-	2.2 0.8 0.6	7.0 1.4 1.2	-	8.8 1.8 1.5	- I	10.5 2.1 1.8	μs μs μs	2.0 20 T 21 A 4.5 6.0	BTOARAHO O Fig.16
R3HT0	propagation delay/bubble-up delay		2.8 1.0 0.8	9.0 1.8 1.5	M XA	11.2 2.2 1.9	XAI	13.5 2.7 2.3	μs μs μs	2.0 4.5 6.0	Fig.8
t _{PZH} /t _{PZL}	3-state output enable OE to Q _n	4.5	44 16 13	150 30 26	- 88	190 38 32	28 [-	225 45 38	ns ns ns	2.0 4.5 6.0	Fig.17
t _{PHZ} /t _{PLZ}	3-state output disable OE to Qn	- 0	50 18 14	150 30 26	- 80	190 38 33	- 88.	225 45 38	ns ns ns	2.0 4.5 6.0	Fig.17
t _{THL} /t _{TLH}	output transition time	-	14 5 4	60 12 10	-	75 15 13	-	90 18 15	ns ns ns	2.0 4.5 6.0	Fig.17
t _w	SI pulse width HIGH or LOW	35 7 6	11 4 3	-	45 9 8	-	55 11 9	-	ns ns ns	2.0 4.5 6.0	Fig.7

5-Bit × 64-word FIFO register; 3-state state of the state

					T _{amb} °C	;			DHAY	TEST	CONDITION
SYMBOL	PARAMETER	imily S	+25	ics", ser	-40 1	to +85	-40 t	0 +125	UNIT	V _{cc}	or the DC chara
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	o revir	(V)	WAVEFORMS
t _w	SO pulse width HIGH or LOW	70 14 12	22 8 6	-	90 18 15	-	105 21 18 (V	0_≥ bnu	ns ns ns	2.0 4.5 6.0	Fig.10
t _w	DIR pulse width HIGH	10 5 4	41 15 12	130 26 22	8 4 3	165 33 28	8 4 3	195 39 33	ns ns ns	2.0 4.5 6.0	Fig.8
e t _w To	DOR pulse width HIGH	14 7 6	52 19 15	160 32 27	12 6 5	200 40 34	12 6 5	240 48 41	ns ns ns	2.0 4.5 6.0	Fig.11
t _w = ol	MR pulse / width	120 24 20	39 14 11	- T	150 30 26	A8.8	180 36 31	4.82-	ns ns ns	2.0 4.5 6.0	Fig.9
t _{rem} 8 = ol	removal time MR to SI	80 16 14	24 8 7		100 20 17	-	120 24 20	- -81.0 -	ns ns ns	2.0 4.5 6.0	Fig.16
t _{su}	set-up time D _n to SI	-8 -4 -3	-36 -13 -10	-	-6 -3 -3	-	-6 -3 -3	-	ns ns ns	2.0 4.5 6.0	Fig.14
t _n	hold time D _n to SI	135 27 23	44 16 13	cient st	170 34 29	ol trius	205 41 35	nis vell	ns ns ns	2.0 4.5 6.0	Fig.14
f _{max}	maximum clock pulse frequency SI, SO burst mode	3.6 18 21	9.9 30 36	-	2.8 14 16	DU TUR DERREG	2.4 12 14	-	MHz MHz MHz	2.0 4.5 6.0	Figs 12 and
f _{max}	maximum clock pulse frequency SI, SO using flags	3.6 18 21	9.9 30 36	-	2.8 14 16	1.5 0.73 1.5	2.4 12 14	-	MHz MHz MHz	2.0 4.5 6.0	Figs 7 and 10
f _{max}	maximum clock pulse frequency SI, SO cascaded	_	7.6 23 27	-	-	-	-	-	MHz MHz MHz	2.0 4.5 6.0	Figs 7 and 10

5-Bit × 64-word FIFO register; 3-state state state of 1-74HC/HCT7404

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS Family Characteristics", section "Family Specifications", except that Vol. and Vol. are not valid for driver output. They are replaced by the values given below.

Output capability: driver 8 mA

I_{cc} category: LSI.

Voltages are referenced to GND (ground = 0 V).

DC CHARACTERISTICS FOR 74HCT

	0.0	an EE ET _{amb} °C E					12 22			TEST CONDITION			
SYMBOL	PARAMETER	ns	+25	-40		-40 to +85		-40 to +125		V _{cc}	ealug RC0	071150	
	0.3	MIN	TYP	MAX	MIN	MAX	MIN	MAX		(V)	HOH	OTHER	
V _{OH} @	HIGH level output voltage	3.98	4.32	180 36 - 31	3.84	50 30 -	3.7	-	V	4.5	V _{IH} Plug FIM or dibliw V _{IL} WOJ	l _o = -8 mA	
V _{OL} 81	LOW level output voltage	ns ns	0.15	0.26	-	0.33	-	0.40	V	4.5	V _{IH} or V _{IL}	l ₀ = 8 mA	

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

UNIT LOAD COEFFICIENT

						9.8	
Figs 12 and TUPNI 18	4.5	SHM SHM		NIT LOA		30	
ŌĒ				1			
SI				1.5			
Dr. book Son B Dn	2.0	ZMM	6.3	0.75	0.3 ht	9.9	
MR	0.8	SHM	40	1.5	ari		
SO				1.5			

etste-8 :netaiper OFIF74HC/HCT7404

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_r = 6$ ns; $C_1 = 50$ pF.

	VAW (V)		VA	UL LEIN	T _{amb} °C	4 1616	L br a a	4 097	MIN	TEST	CONDITION
SYMBOL	PARAMETER		+25		-40 t	o +85	-40 t	o +125	UNIT	V _{cc}	MANTEODAG
	s Fig.8	MIN	TYP	MAX	MIN	MAX	MIN	MAX		(V)	WAVEFORMS
t _{PHL} /t _{PLH}	propagation delay MR to DIR, DOR	s s	30	51	5 e	53	67 8	63	ns	4.5 ^{98luq}	Fig.9
t _{PHL}	propagation delay MR to Qn	s _4	22	38		48 8	0-	57 8	ns 8	4.5	Fig.9
t _{PHL} /t _{PLH}	propagation delay SI to DIR	9	25	43		54		65	ns 8	emil lave 4.5 18 o	Fig.7
t _{PHL} /t _{PLH}	propagation delay SO to DOR	s 4	36	61	1	76		92	ns	time 2.4	Fig.10
t _{PHL} /t _{PLH}	propagation delay SO to Q _n		42	72	1	90		108	ns 8	mum coulse c.4	Fig.15
t _{PHL} /t _{PLH}	propagation delay DOR to Q _n		7	12	1	15	1	18	ns	Denst O O O O O O O O O O O O O O O O O O O	Fig.11
Of bos T	propagation delay/ripple through delay SI to DOR	11-12 4	0.8	1.4		1.75	-	2.1	μs ⁸	4.5 your O	Fig.11
t _{PLH} S	propagation delay/bubble-u p delay SO to DIR	iHz 4	1	1.8		2.25	-	2.7	μѕ	4.5 mum 9akuq yangu O	Fig.8
t _{PZH} /t _{PZL}	3-state output enable OE to Q _n	-	16	30	-	38	-	45	ns	4.5	Fig.17
t _{PHZ} /t _{PLZ}	3-state output disable OE to Qn	-	19	30	-	38	_	45	ns	4.5	Fig.17
t _{THL} /t _{TLH}	output transition time	_	5	12	-	15	-	18	ns	4.5	Fig.17
t _w	SI pulse width HIGH or LOW	9	5	-	6	-	8	-	ns	4.5	Fig.7
t _w	SO pulse width HIGH or LOW	14	8	_	18		21		ns	4.5	Fig.10

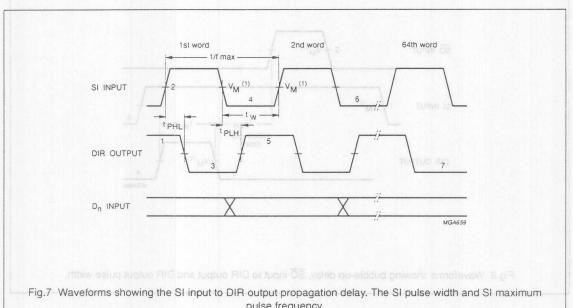
etala-8 register; 3-state

					T _{amb} °C	;			74HC1	TEST	CONDITION	
SYMBOL	PARAMETER		+25		-40 1	to +85	-40 to	0 +125	UNIT	V _{cc}	WAVEFORMS	
	TEST CONT	MIN	TYP	MAX	MIN	MAX	MIN	MAX		(V)	WAVEFORMS	
amao as t _w	DIR pulse width HIGH	5	17KAN	29	4 XAI	36	4 XA	44 3 4	ns Mill	4.5	Fig.8	
t _w	DOR pulse width HIGH	7	21	36	6	45	6	54	ns	4.5 AIQ	Fig.11	
t _w	MR pulse width LOW	26	15	-	33 8	-	39		ns	4.5	Fig.9	
t _{rem}	removal time MR to SI	18	10	1	23		27	A 8	ns	4.5	Fig.16	
t _{su}	set-up time D _n to SI	-5	-16		-4		-4		ns	4.5 Hodisp	Fig.14	
t _h	hold time D _n to SI	30	18	-	38	-	45	8	ns	4.5 _{ROG}	Fig.14	
f _{max}	maximum clock pulse frequency SI, SO burst mode	18	30	4	14		12	5	MHz	4.5 D	Figs 12 and 13	
f _{max}	maximum clock pulse frequency SI, SO using flags	18	30		14		12	8.	MHz	4.5 elgain ysleb at	Figs 7 and 10	
f _{max}	maximum clock pulse frequency SI, SO cascaded	2.	23	_	25	-	8.	-	MHz	nodag u-elddud 4.5 yr	Figs 7 and 10	

etste-8 register; 8-state

AC WAVEFORMS

Shifting in sequence FIFO empty to FIFO full



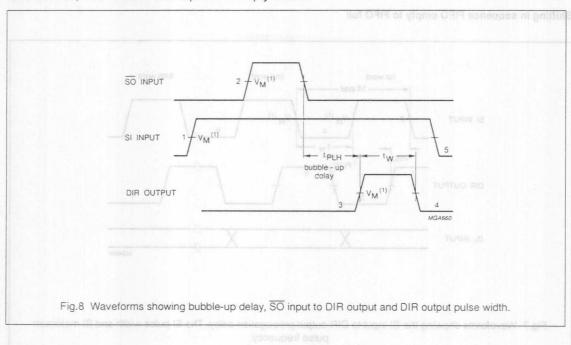
pulse frequency.

- 1. DIR initially HIGH; FIFO is prepared for valid data
- 2. SI set HIGH; data loaded into input stage
- 3. DIR goes LOW, input stage "busy"
- 4. SI set LOW; data from first location "ripple through"
- 5. DIR goes HIGH, status flag indicates FIFO prepared for additional data
- 6. Repeat process to load 2nd word through to 64th word into FIFO DIR remains LOW; with attempt to shift into full FIFO, no data transfer occurs.

etate-8 greateless OFI 74HC/HCT7404

5-Bit × 64-word FIFO register; 3-state

With FIFO full; SI held HIGH in anticipation of empty location



- 1. FIFO is initially full, shift-in is held HIGH
- 2. SO pulse; data in the output stage is unloaded, "bubble-up" process of empty location begins
- 3. DIR HIGH; when empty location reaches input stage, flag indicates FIFO is prepared for data input
- 4. DIR returns to LOW; data shift-in to empty location is complete, FIFO is full again
- 5. SI set LOW; necessary to complete shift-in process, DIR remains LOW, because FIFO is full.

404773H/OH47-IFO register, 3-state

Master reset applied with FIFO full

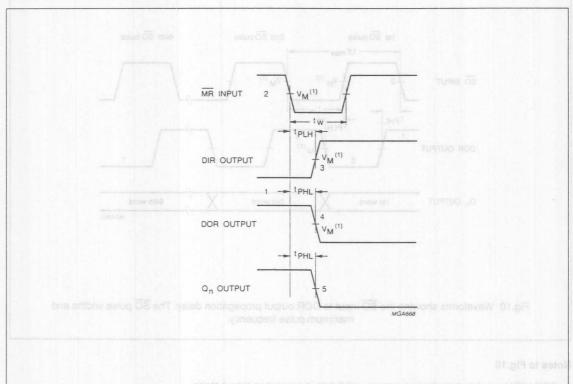
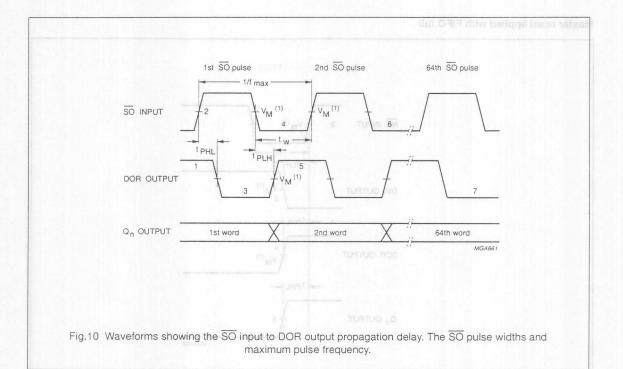


Fig.9 Waveforms showing the $\overline{\text{MR}}$ input to DIR, DOR and Q_n output propagation delays and the $\overline{\text{MR}}$ pulse width.

- 1. DIR LOW, output ready HIGH; assume FIFO is full
- 2. MR pulse LOW; clears FIFO
- 3. DIR goes HIGH; flag indicates input prepared for valid data
- 4. DOR goes LOW; flag indicates FIFO empty
- 5. Q_n outputs go LOW (only last bit will be reset).

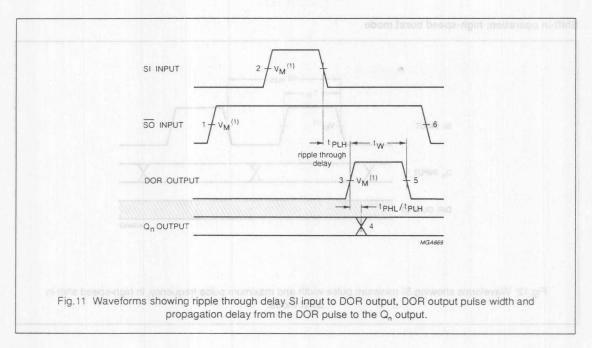




Notes to Fig.10

- 1. DOR HIGH; no data transfer in progress, valid data is present at output stage
- 2. SO set HIGH; results in DOR going LOW
- 3. DOR goes LOW; output stage "busy"
- 4. SO set LOW; data in the input stage is unloaded, and new data replaces it as empty location "bubbles-up" to input stage
- 5. DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay
- 6. Repeat process to unload the 3rd through to the 64th word from FIFO.
- 7. DOR remains LOW; FIFO is empty.

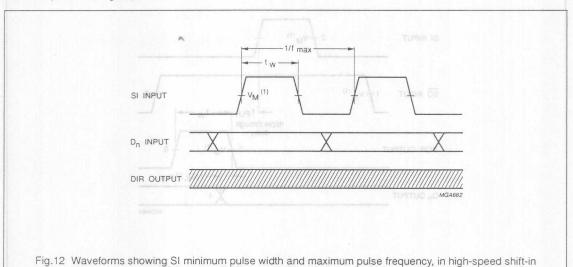
With FIFO empty; SO is held HIGH in anticipation



- 1. FIFO is initially empty, SO is held HIGH
- 2. SI pulse; loads data into FIFO and initiates ripple through process
- 3. DOR flag signals the arrival of valid data at the output stage
- 4. Output transition; data arrives at output stage after the specified propagation delay between the rising edge of the DOR pulse to the Q_n output
- 5. DOR goes LOW; data shift-out is complete, FIFO is empty again
- 6. SO set LOW; necessary to complete shift-out process. DOR remains LOW, because FIFO is empty.

5-Bit × 64-word FIFO register; 3-state elasta-8 refairer OFIF74HC/HCT7404

Shift-in operation; high-speed burst mode



Note to Fig.12

In the high-speed mode, the burst-in rate is determined by the minimum shift-in HIGH and shift-in LOW specifications. The DIR status flag is a don't care condition, and a shift-in pulse can be applied regardless of the flag. A SI pulse which would overflow the storage capacity of the FIFO is ignored. I sload setsillar on SIFO and stable setsillar setsillar on the storage capacity of the FIFO is ignored.

g higher through dispersion and a policy policy policy policy purple output plant and plant plan

Shift-out operation; high-speed burst mode

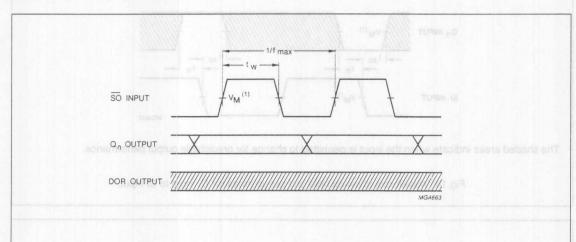
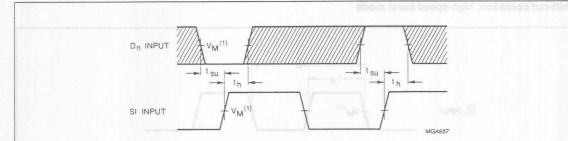


Fig.13 Waveforms showing SO minimum pulse width and maximum pulse frequency, in high-speed shift-out burst mode.

Note to Fig.13

In the high-speed mode, the burst-out rate is determined by the minimum shift-out HIGH and shift-out LOW specifications. The DOR flag is a don't care condition and an SO pulse can be applied without regard to the flag.



The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 14 Waveforms showing hold and set-up times for D_n input to SI input.

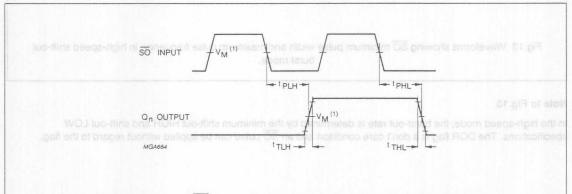


Fig. 15 Waveforms showing SO input to Q_n output propagation delays and output transition time.

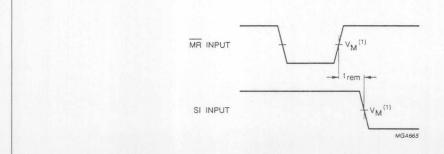
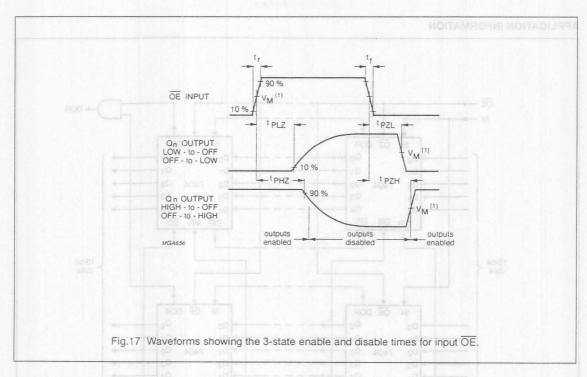


Fig.16 Waveform showing the MR input to SI input removal time.

5-Bit × 64-word FIFO register; 3-state

etata-8 retaiges O = 74HC/HCT7404

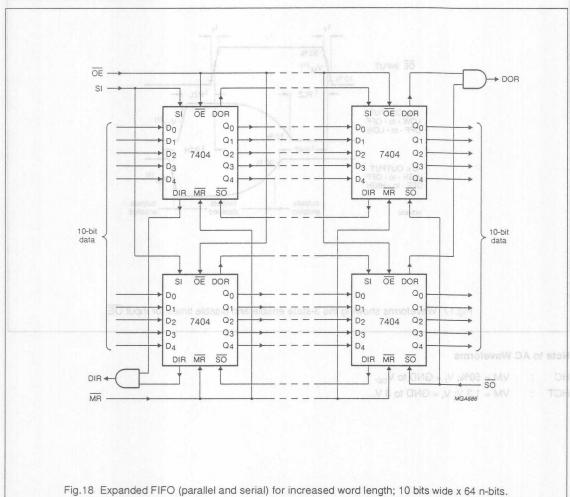


Note to AC Waveforms

HC : VM = 50%; $V_1 = GND$ to V_{CC} .

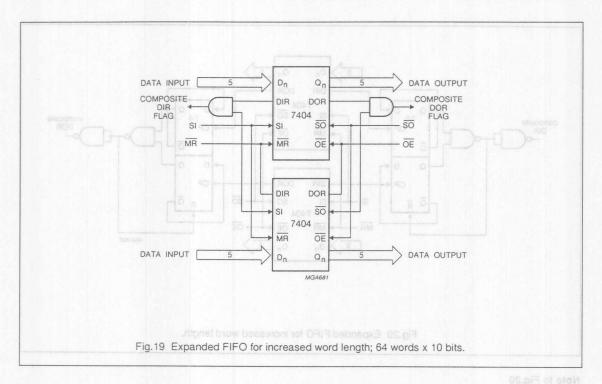
HCT : VM = 1.3 V; $V_1 = \text{GND to } 3 \text{ V}$.

APPLICATION INFORMATION



5-Bit × 64-word FIFO register; 3-state

etata-8 ;retaiper ORI-74HC/HCT7404

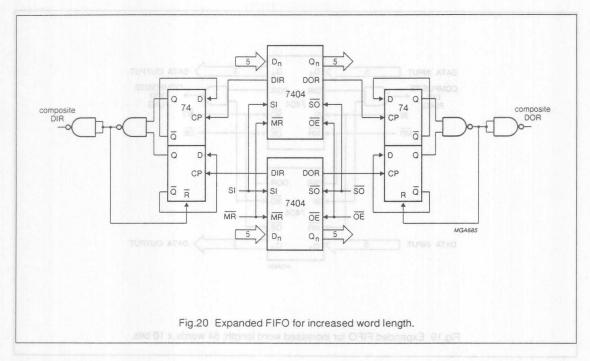


This circuit is only required if the SI input is constantly held HIGH, when the FIFO is empty and the autor 19. gift of all of The "7404" is easily expanded to increase word length. Composite DIR and DOR flags are formed with the addition of an AND gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.

Philips Semiconductors Product specification

5-Bit × 64-word FIFO register; 3-state

etata-8 metalgen OFI-74HC/HCT7404



Note to Fig.20

This circuit is only required if the SI input is constantly held HIGH, when the FIFO is empty and the automatic shift-in cycles are started or if SO output is constantly held HIGH, when the FIFO is full and the automatic shift-out cycles are started (see Figs 8 and 10).

Expanded format

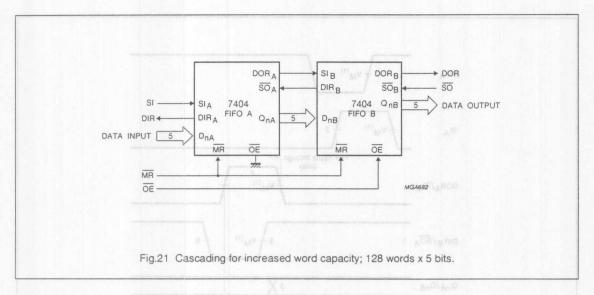
Figure 21 shows two cascaded FIFOs providing a capacity of 128 words x 5 bits. Figure 22 shows the signals on the nodes of both FIFOs after the application of a SI pulse, when both FIFOs are initially empty. After a ripple through delay, data arrives at the output of FIFO_A. Due to \overline{SO}_A being HIGH, a DOR_A pulse is generated. The requirements of SI_B and D_{nB} are satisfied by the DOR_A pulse width and the timing between the rising edge of DOR_A and Q_{nA}. After a second ripple through delay, data arrives at the output of FIFO_B.

Figure 23 shows the signals on the nodes of both FIFOs after the application of \overline{a} \overline{SO}_B pulse, when both FIFOs are initially full. After a bubble-up delay a DIR $_B$ pulse is generated, which acts as a \overline{SO}_A pulse for FIFO $_A$. One word is transferred from the output of FIFO $_A$ to the input of FIFO $_B$. The requirements of the \overline{SO}_A pulse for FIFO $_A$ is satisfied by the pulse width of DOR $_B$. After a second bubble-up delay an empty space arrives at D $_{nA}$, at which time DIR $_A$ goes HIGH. Figure 24 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.

5-Bit × 64-word FIFO register; 3-state

95 Para September 3-state

Product specification



Note to Fig.21

The "7404" is easily cascaded to increase word capacity without any external circuitry. In cascaded format, all necessary communications are handled by the FIFOs. Figures 22 and 23 demonstrate the intercommunication timing between FIFO_A and FIFO_B. Figure 24 provides an overview of pulses and timing of two cascaded FIFOs, when shifted full and shifted empty again.

FIFO, and FIFO, initially empty, SO, held HIGH in anticipation of data

Load one word into FIFO. Stipules applied, results in DIR dutse

mealing data input set-up requirements of PFFO_s

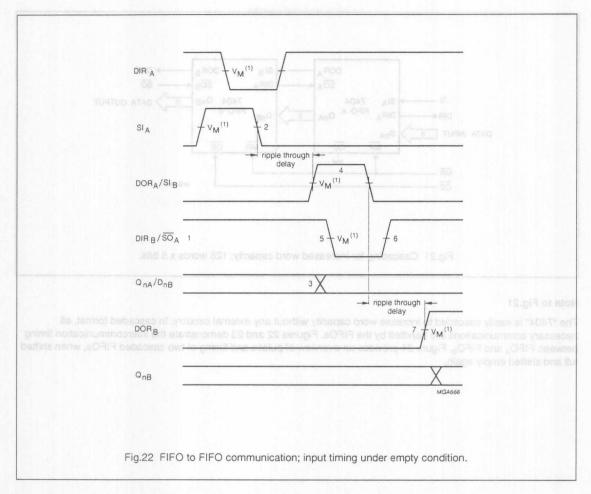
data output ready pulse, data is snifted into FIFO_e

6. DIR₈ and \overline{SO}_{x} go HIGH automatically, the input stage of FIFO₈ is again able to receive data, \overline{SO} is held HIGH in

DOR₈ goes HIGH; (ripple through delay after SI₅ LGW) valid data is present one propagation datay later at the

5-Bit × 64-word FIFO register; 3-state

etata-8 metaipen OFI 74HC/HCT7404

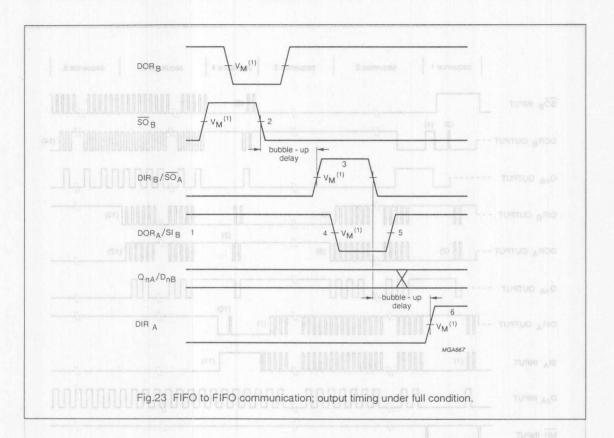


Notes to Fig.22

- 1. ${\rm FIFO_A}$ and ${\rm FIFO_B}$ initially empty, $\overline{\rm SO_A}$ held HIGH in anticipation of data
- 2. Load one word into FIFO_A; SI pulse applied, results in DIR pulse
- Data-out A/data-in B transition; valid data arrives at FIFOA output stage after a specified delay of the DOR flag, meeting data input set-up requirements of FIFOB
- DOR_A and SI_B pulse HIGH; (ripple through delay after SI_A LOW) data is unloaded from FIFO_A as a result of the data output ready pulse, data is shifted into FIFO_B
- 5. DIR_B and \overline{SO}_A go LOW; flag indicates input stage of FIFO_B is busy, shift-out of FIFO_A is complete
- DIR_B and SO_A go HIGH automatically; the input stage of FIFO_B is again able to receive data, SO is held HIGH in anticipation of additional data
- DOR_B goes HIGH; (ripple through delay after SI_B LOW) valid data is present one propagation delay later at the FIFO_B output stage.

Philips Semiconductors Product specification

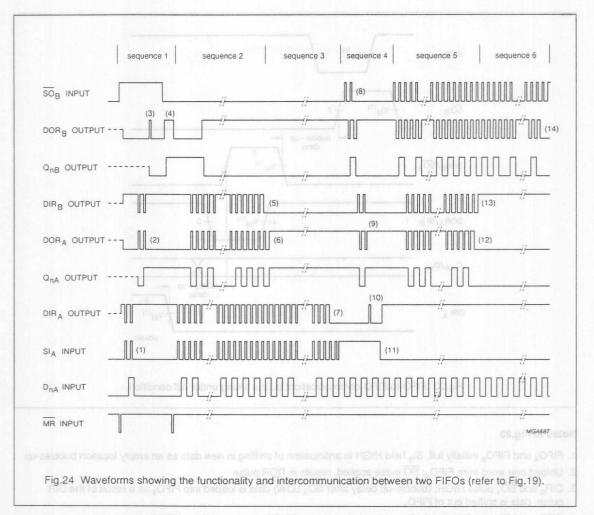
5-Bit × 64-word FIFO register; 3-state etala-8 metalana 03/13/74HC/HCT7404



Notes to Fig.23

- 1. FIFO_A and FIFO_B initially full, SI_B held HIGH in anticipation of shifting in new data as an empty location bubbles-up
- 2. Unload one word from FIFO_B; SO pulse applied, results in DOR pulse
- 3. DIR_B and \overline{SO}_A pulse HIGH; (bubble-up delay after \overline{SO}_B LOW) data is loaded into FIFO $_B$ as a result of the DIR pulse, data is shifted out of FIFO $_A$
- 4. DOR_A and SI_B go LOW; flag indicates the output stage of FIFO_A is busy, shift-in to FIFO_B is complete
- DOR_A and SI_B go HIGH; flag indicates valid data is again available at FIFO_A output stage, SI_B is held HIGH, awaiting bubble-up of empty location
- 6. DIR_A goes HIGH; (bubble-up delay after \overline{SO}_A LOW) an empty location is present at input stage of FIFO_A.

5-Bit × 64-word FIFO register; 3-state



Note to Fig.24

Sequence 1 (both FIFOS empty, starting SHIFT-IN process)

After a MR pulse has been applied FIFO, and FIFO, are empty. The DOR flags of FIFO, and FIFO, go LOW due to no valid data being present at the outputs. The DIR flags are set HIGH due to the FIFOs being ready to accept data. SOs is held HIGH and two SIs pulses are applied (1). These pulses allow two data words to ripple through to the output stage of FIFO_A and to the input stage of FIFO_B (2). When data arrives at the output of FIFO_B, a DOR_B pulse is generated (3). When SO_B goes LOW, the first bit is shifted out and a second bit ripples through to the output after which DOR_B goes HIGH (4).

5-Bit × 64-word FIFO register; 3-state

74HC/HCT7404

Sequence 2 (FIFO_B runs full)

After the $\overline{\text{MR}}$ pulse, a series of 64 SI pulses are applied. When 64 words are shifted in, DIR_B remains LOW due to FIFO_B being full (5). DOR_A goes LOW due to FIFO_A being empty.

Sequence 3 (FIFO, runs full)

When 65 words are shifted in, DOR_A remains HIGH due to valid data remaining at the output of FIFO_A. Q_{nA} remains HIGH, being the polarity of the 65th data word (6). After the 128th SI pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

Squence 4 (both FIFOs full, starting SHIFT-OUT process)

SI_A is held HIGH and two $\overline{\text{SO}}_{\text{B}}$ pulses are applied (8). These pulses shift out two words and thus allow two empty locations to bubble-up to the input stage of FIFO_B, and proceed to FIFO_A (9). When the first empty location arrives at the input of FIFO_A, a DIR_A pulse is generated (10) and a new word is shifted into FIFO_A. SI_A is made LOW and now the second empty location reaches the input stage of FIFO_A, after which DIR_A remains HIGH (11).

Sequence 5 (FIFO_A runs empty)

At the start of sequence 5 FIFO_A contains 63 valid words due to two words being shifted out and one word being shifted in, in sequence 4. An additional series of \overline{SO}_B pulses are applied. After 63 \overline{SO}_B pulses, all words from FIFO_A are shifted into FIFO_B. DOR_A remains LOW (12).

Sequence 6 (FIFO_B runs empty)

After the next \overline{SO}_B pulse, DIR_B remains HIGH due to the input stage of FIFO_B being empty. After another 63 \overline{SO}_B pulses, DOR_B remains LOW due to both FIFOs being empty (14). Additional \overline{SO}_B pulses have no effect. The last word remains available at the output Q_n.

5-Bit x 64-word FIFO register, 3-state

74HC/HCT7404

Sequence 2 (FIFO_e runs full)

After the MR pulse, a series of 64 SI pulses are applied. When 64 words are shifted in. DIR₈ remains LOW due to FIFO₈ being full (5), DOR, goes LOW due to FIFO, being empty.

Sequence 3 (FIFO, runs full)

When 65 words are shifted in, DOR, remains HIGH due to valid data remaining at the output of FIFO_n . $\mathsf{Q}_{n,n}$ remains HIGH, being the polarity of the 85th data word (6). After the 128th SI pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

squence 4 (both FIFOs full, tarring SHIFT-OUT process)

SI_a is held HIGH and two \overline{SO}_B pulses are applied (8). These pulses shift out two words and thus allow two empty locations to bubble-up to the input stage of FIFO_e, and proceed to FIFO_a (8). When the first empty location arrives at the input of FIFO_a, a DIR, pulse is generated (10) and a new word is

penerated (10) and a new word is inited into FIFO_x. SI_x is made LOW and now the second empty location eaches the input stage of FIFO_x, after which DIR, remains HIGH (11).

sequence 5 (FIFO, runs empty)

At the start of sequence 5 FIFO, contains 63 valid words due to two words being shifted out and one word being shifted in, in sequence 4. An additional series of $\overline{\rm SO}_{\rm g}$ pulses are applied. After 63 $\overline{\rm SO}_{\rm g}$ pulses, words from FIFO, are shifted into FIFO, are shifted into FIFO, are shifted into

Sequence 6 (FIFO, runs empty)

After the next SO_g pulse. DIR_g remains HIGH, due to the input stage of FIFO_g being emoty. After another SS SO_g pulses, DOR_g remains LOW due to both FIFOs being empty (14). Additional SO_g pulses have no effect. The last word remains evailable at the output O_g.

SUPERSEDES DATA OF MARCH 1988

OCTAL SCHMITT TRIGGER BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- Inverting outputs
- Schmitt trigger action on all data
- Output capability: bus driver
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT7540 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7540 are octal Schmitt trigger inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs OE₁ and OE₂.

A HIGH on $\overline{\text{OE}}_n$ causes the outputs to assume a high impedance OFF-state.

The Schmitt trigger action in the data inputs transforms slowly changing input signals into sharply defined jitter-free output signals.

The "7540" is identical to the "540" but has hysteresis on the data inputs.

01/11/01	PIN NO. SYMBO	CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER 81.1	CONDITIONS	нс	нст	ONT	
tPHL/	propagation delay A_n to \overline{Y}_n	C _L = 15 pF V _{CC} = 5 V	11	16	ns	
CI	input capacitance	W 17 00	3.5	3.5	pF	
CPD power dissipation capacitance per buffer		notes 1 and 2	29	31	pF	

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μW):

PD = CPD \times VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

f; = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF

VCC = supply voltage in V

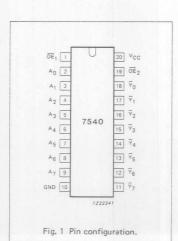
 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

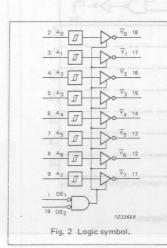
2. For HC the condition is V_I = GND to VCC For HCT the condition is $V_1 = GND$ to VCC - 1.5 V

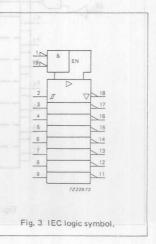
PACKAGE OUTLINES

20-lead DIL; plastic (SOT146).

20-lead mini-pack; plastic (SO20; SOT163A).







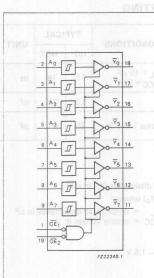


Fig. 4 Functional diagram.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{\text{OE}}_1, \overline{\text{OE}}_2$	output enable inputs (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₇	data inputs data inputs and cyclinder opport
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	∇ ₀ to ∇ ₇	GENERAL DESCRIPTION studios and
20 lug reg sons	Vcc	positive supply voltage

FUNCTION TABLE

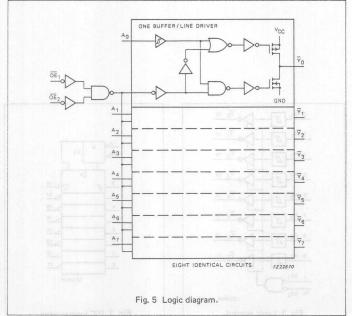
	INPUTS		OUTPUTS
OE ₁	ŌE ₂	An	∇_n
L SH	ancy ig N	upper H	igine H of
antimo i	o ufins = 1	C H	DAX Follo
X	VH nois	X	I OZIOT.
HID =	VX noi	X	TOZ

H = HIGH voltage level

L = LOW voltage level UO BDANDAS

X = don't care

X = don't care Z = high impedance OFF-state



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Transfer characteristics are given below (not applicable for \overline{OE}_n inputs).

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

					T _{amb} (°C)					TEST CONDITIONS	
01/14001		74HC								TIM	HORAGOS FORM	
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			0E2 1.30 Ad 0.20	
tphl/	propagation delay A _n to ∀ _n		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 8	
tPZH/	3-state output enable time $\overline{\text{OE}}_n$ to \overline{Y}_n		41 15 12	150 30 26	(3°) di	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9	
t _{PHZ} /	3-state output disable time $\overline{\text{OE}}_n$ to \overline{Y}_n	351	52 19 15	150 30 26	or 08	190 38 33	35-	225 45 38	ns	2.0 4.5 6.0	Fig. 9	
t _{THL} /	output transition time	XSIII BB	14 5 4	60 12 10	m mi	75 15 13	n .qy	90 18 15	ns	2.0 4.5 6.0	Fig. 8	

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are refered to GND (ground = 0 V)

	a 4.5 Fig. 8	81			T _{amb} (°C)				TEST CONDITIONS		
OVANDOL		74HC								.,		
SYMBOL	PARAMETER	+25			-40	-40 to +85 -40 to +			UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		. 411111	NO 10 Sereier eta aspatio	
V _{T+}	positive-going threshold			1.50 3.15 4.20	10°1 _{de}	1.50 3.15 4.20		1.50 3.15 4.20	V	2.0 4.5 6.0	Figs 6 and 7	
V _T _	negative-going threshold	0.30 1.35 1.80	es (ia	- 28	0.30 1.35 1.80	m	0.30 1.35 1.80	i Leur	٧	2.0 4.5 6.0	Figs 6 and 7	
VH	hysteresis ($V_{T+} - V_{T-}$)	0.10 0.25 0.30	0.40		0.10 0.25 0.30	0	0.10 0.25 0.30		V file	2.0 4.5 6.0	Figs 6 and 7	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below (not applicable for \overline{OE}_n inputs).

Output capability: bus driver ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
OE ₁	1.30
A _n	0.20

AC CHARACTERISTICS FOR 74HCT

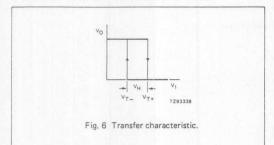
GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_1 = 50 \text{ pF}$

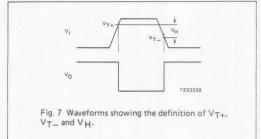
	ns 4.6 Fig. 9 6.0		T _{amb} (°C) 08 31							TEST CONDITIONS		
SYMBOL	PARAMETER	74HCT							UNIT	\/	WAVEFORMS	
STIVIBUL	DL PARAMETER		+25		-40	to +85	-40 to +125		UNIT	VCC	Young	
	2.9	min.	typ.	max.	min.	max.	min.	max.				
tPHL/ tPLH	propagation delay A_n to \overline{Y}_n	81	19	32	1	40		48	ns	4.5	Fig. 8	HJ73
tPZH/	3-state output enable time \overline{OE}_n to \overline{Y}_n		19	32		40		48	ns	4.5	Fig. 9	
tPHZ/ tPLZ	$\frac{3\text{-state output disable time}}{\overline{\text{OE}}_n \text{ to } \overline{Y}_n}$		20	32		40		48	ns	4.5	Fig. 9	
tTHL/101	output transition time		5	12	(0°) er	15		18	ns	4.5	Fig. 8	

TRANSFER CHARACTERISTICS FOR 74HCT

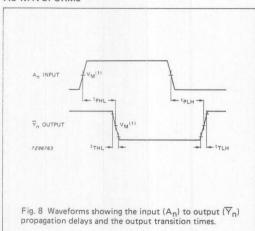
	2.0 V 4.6 Figs 6 and 7 6.0	OS A 74HCT								TEST CONDITIONS		
CYMPOL											Total Strategy = 1	
SYMBOL	PARAMETER O.S	+25			-40	to +85	-40 to +125		UNIT	V _{CC}	WAVEFORMS	
	0.a	min.	typ.	max.	min.	max.	min.	max.				
V _{T+}	positive-going threshold		88	2.0 2.1	25	2.0 2.1	40	2.0 2.1	V	4.5 5.5	Figs 6 and 7	
V _T _	negative-going threshold	0.70 0.80			0.64 0.74		0.60 0.70		V	4.5 5.5	Figs 6 and 7	
VH	hysteresis (V _{T+} - V _T _)		0.23 0.23						٧	4.5 5.5	Figs 6 and 7	

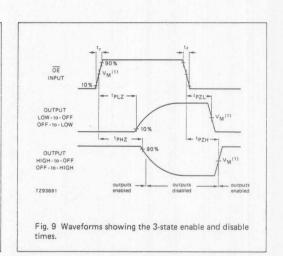
TRANSFER CHARACTERISTIC WAVEFORMS





AC WAVEFORMS





Note to AC waveforms

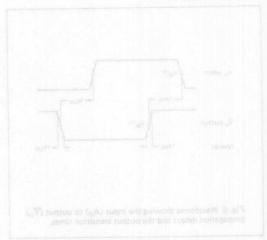
(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

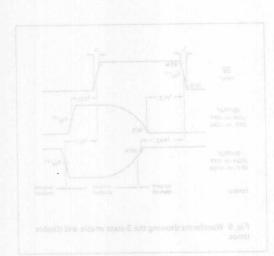
THANSFER CHARACTERISTIC WAVEFORMS



V; and VH.

AC VIAVEPORMS





Note to AC waveform:

(1) MC: V_M = 69%; V_I = GND to V_{CC}

HCT: V_M = 1.3 N; V_I = GND to 3 V.

SUPERSEDES DATA OF MARCH 1988

OCTAL SCHMITT TRIGGER BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Non-inverting outputs
- Schmitt trigger action on all data a public
- Icc category: MS1

GENERAL DESCRIPTION

The 74HC/HCT7541 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7541 are octal Schmitt trigger non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs \overline{OE}_1 and \overline{OE}_2 .

A HIGH on $\overline{\text{OE}}_n$ causes the outputs to assume a high impedance OFF-state.

The Schmitt trigger action in the data inputs transforms slowly changing input signals into sharply defined jitter-free output signals.

The "7541" is identical to the "541" but has hysteresis on the data inputs.

OVANDO!	PIN NO. SYMSO	CONDITIONS	TYF	UNIT		
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT	
PHL propagation delay PLH A _n to $\overline{\forall}_n$		C _L = 15 pF V _{CC} = 5 V	10	16	ns	
CI	input capacitance	ar cY	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	32	pF	

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

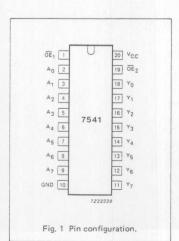
f; = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF VCC = supply voitage in V

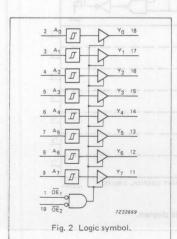
 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

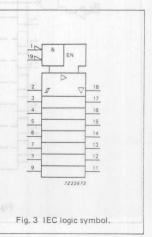
2. For HC the condition is VI = GND to VCC For HCT the condition is $V_1 = GND$ to VCC - 1.5 V

PACKAGE OUTLINES

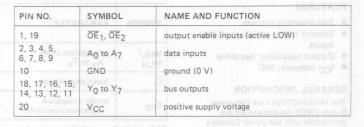
20-lead DIL; plastic (SOT146). 20-lead mini-pack; plastic (SO20; SOT163A).











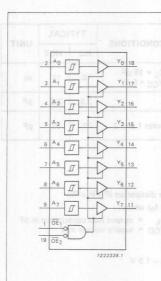


Fig. 4 Functional diagram.

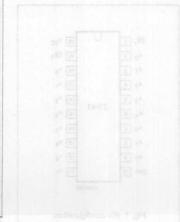
FUNCTION TABLE

	INPUTS		OUTPUTS
OE ₁	OE ₂	An	O - Yn
L	IM ni yor	supent	thom to it
L	L	Н	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level

L = LOW voltage level

X = don't care Z = high impedance OFF-state



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below (not applicable for $\overline{\text{OE}}_n$ inputs).

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

					T _{amb} (°C)					TEST CONDITIONS
		74HC								Tu	BIOPIAGO
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			An 0.20
tPHL/	propagation delay A _n to Y _n		39 14 11	120 24 20		150 30 26		180 36 32	ns	2.0 4.5 6.0	Fig. 8
tPZH/	3-state output enable time $\overline{\text{OE}}_n$ to Y_n		44 16 13	160 32 27	(0°) e	200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 9
tPHZ/ tPLZ	3-state output disable time OE _n to Y _n	25	58 21 17	160 32 27	e of 0	200 40 34	85	240 48 41	ns	2.0 4.5 6.0	Fig. 9
tTHL/ tTLH	output transition time	1	14 5 4	60 12 10	40	75 15 13	32	90 18 15	ns	2.0 4.5 6.0	Fig. 8 4914 1949

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are refered to GND (ground = 0 V)

					T _{amb} (°C)				TEST CONDITIONS			
SYMBOL	PARAMETER	74HC TOHAT								RIST	ANSFER CHARACT		
STWIBOL	FARAMETER		+25		-40	to +85	-40 to +125		UNIT	V _{CC}	WAVEFORMS		
	TEST CONDIT	min.	typ.	max.	min.	max.	min.	max.					
V _{T+}	positive-going threshold	25	1 ± 01 0	1.50 3.15 4.20	TOF 0 to +B	1.50 3.15 4.20	at	1.50 3.15 4.20	V	2.0 4.5 6.0	Figs 6 and 7	.108M/	
V _T _	negative-going threshold	0.30 1.35 1.80	m. 3	iim 3	0.30 1.35 1.80	380 .3	0.30 1.35 1.80	er ein	٧	2.0 4.5 6.0	Figs 6 and 7		
V _H	hysteresis (V _{T+} – V _T _)	0.10 0.25 0.30		0.0	0.10 0.25 0.30	5,0	0.10 0.25 0.30	170	V blo	2.0 4.5 6.0	Figs 6 and 7	-т	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below (not applicable for \overline{OE}_n inputs).

Output capability: bus driver I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD
OE ₁ OE ₂	1.30 1.30
An	0.20

AC CHARACTERISTICS FOR 74HCT

GND = 0 V: t = tr = 6 ps: Cr = 50 pF

	2.0 Fig. 8				T _{amb} (°C)			time	aldens :	TEST CONDITIONS	HES
	0.8		4		74HC	т	27	13			o Y ot nad	PZL
SYMBOL	PARAMETER O.S.	40	+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS	
	6.0	min.	typ.	max.	min.	max.	min.	max.				
tPHL/	propagation delay An to Yn	200 73	19	32	13	40	10	48	ns	4.5	Fig. 8	UHT HJT
tPZH/ tPZL	3-state output enable time OEn to Yn		18	32		40		48	ns	4.5	Fig. 9	
t _{PHZ} / t _{PLZ}	3-state output disable time \overline{OE}_n to Y_n		20	32		40		48	ns	4.5	Fig. 9	RMAR
tTHL/ tTLH	output transition time		5	12		15		18	ns	4.5	Fig. 8	egario

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are referred to GND (ground = 0 V)

		.88	fol J. Ji	im J	T _{amb} (°C)	9. mag	ibt. Sys			TEST CONDITIONS
SYMBOL	DADAMETER 0.5	08			74HC	T			LINUT	.,	WAVEFORMS
STIMBOL	PARAMETER 0.8	20	+25		-40	to +85	-40 t	o +125	UNIT	VCC V	WAVEFORMS
	2.0	min.	typ.	max.	min.	max.	min.	max.	0		
V _{T+}	positive-going threshold		0	2.0 2.1	0	2.0 2.1		2.0	٧	4.5 5.5	Figs 6 and 7
V _T -	negative-going threshold	0.70 0.80		0.0	0.64	0.2	0.60 0.70	25 D.4	٧	4.5 5.5	Figs 6 and 7
VH	hysteresis (V _{T+} – V _T _)		0.23						٧	4.5 5.5	Figs 6 and 7

TRANSFER CHARACTERISTIC WAVEFORMS

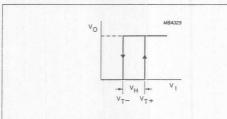


Fig. 6 Transfer characteristic.

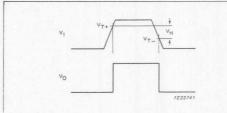


Fig. 7 Waveforms showing the definition of $V_{T+},\ V_{T-}$ and $V_{H}.$

AC WAVEFORMS

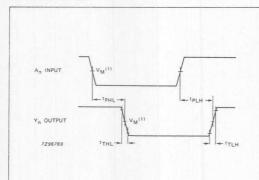


Fig. 8 Waveforms showing the input $({\rm A_n})$ to output $({\rm Y_n})$ propagation delays and the output transition times.

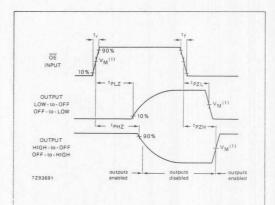


Fig. 9 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

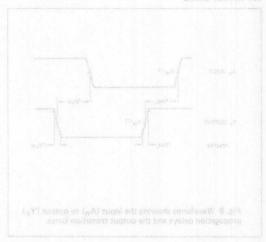
(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

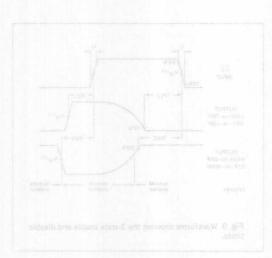
TRANSFER CHARACTERISTIC WAVEFORMS





AC WAVEFORMS





Note to AC waveforms
(1) HC: V_M = 50%: V₁ =

8-BIT SHIFT REGISTER WITH INPUT LATCHES

FEATURES

- · 8-bit parallel input latches
- Shift register has direct overriding load and clear
- Output capability: standard
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT7597 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7597 both consist of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register.

When LE is LOW, data at the Dn inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is HIGH the latches store the information that was present at the D-inputs, a set-up time preceding the LOW-to-HIGH transition of LE.

The shift register has a positive edgetriggered clock, direct load (from storage) and clear inputs.

01/11001	FURCTION TABLE	001101710110	TYP	LINUT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
tPHL/ tPLH	propagation delay SHCP to Q LE to Q PL to Q D ₇ to Q	C _L = 15 pF V _{CC} = 5 V	15 22 20 20	17 27 23 24	ns ns ns ns
f _{max}	maximum clock frequency	T18-8 37H3	99	79	MHz
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	9.0	29	30	pF

GND = 0 V;
$$T_{amb} = 25$$
 °C; $t_r = t_f = 6$ ns

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

 $PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$ where:

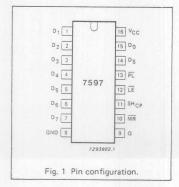
- f; = input frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V fo = output frequency in MHz
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

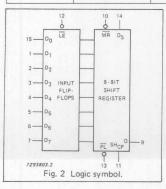
PACKAGE OUTLINES

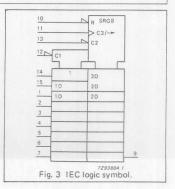
- 16-lead DIL; plastic (SOT38Z).
- 16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9	Q	serial data output
10	MR	asynchronous reset input (active LOW)
11	SHCP	shift clock input (LOW-to-HIGH, edge-triggered)
12	LE	latch enable input (active LOW)
13	PL	parallel load input (active LOW)
14	DS	serial data input
15, 1, 2, 3, 4, 5, 6, 7	D ₀ to D ₇	parallel data inputs
16	Vcc	positive supply voltage







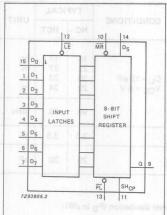


Fig. 4 Functional diagram.

FUNCTION TABLE SERUTAGE

LE	SH _{CP}	PL	MR	FUNCTION THE PROPERTY OF THE P
L ye	X	X	X	data enabled to input latches (transparent
Н	X O d	X	X	data stored into latches (non-transparent)
X	x	L	Н	data transferred from input latches to shift register
X	x 90	L	xsm [†]	invalid logic, state of shift register indeterminate when signals removed
X	X	Н	L	shift register cleared AT on bushness
X	↑ Presidence	Н	H	shift register clocked $Q_n = Q_{n-1}$, $Q_0 = Q_0$

H = HIGH voltage level

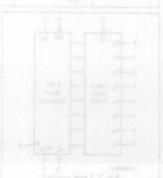
L = LOW voltage level

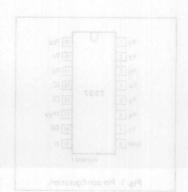
X = don't care

↑ = LOW-to-HIGH CP transition

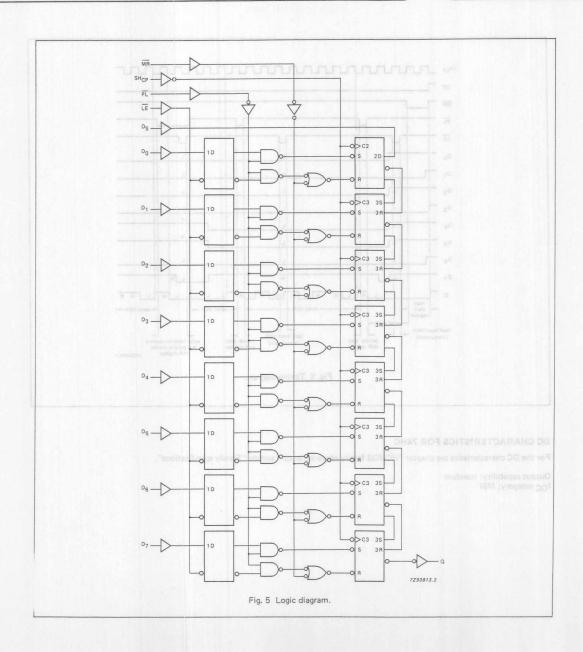
	parallel load input (active LOW)

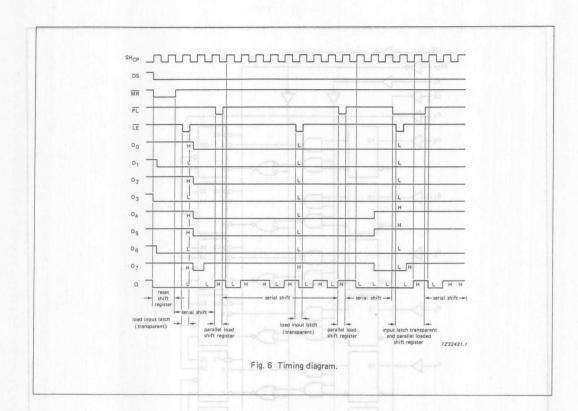






When LE is LOW, data at the On inputs enter the latches. In this condition the





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

AC CHARACTERISTICS FOR 74HC

					T _{amb} (°C)					TEST CONDITIONS
	UNIT VCC WAVEFORM	2000	1	1 20	74H		36.			A	MBOL PARAMETE
SYMBOL	PARAMETER		+25		-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS
	0.0	min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} /	propagation delay SH _{CP} to Q		50 18 14	175 35 30		220 44 37	1.	265 53 45	ns	2.0 4.5 6.0	Fig. 7
PHL	propagation delay MR to Ω		52 19 15	175 35 30		220 44 37	00 00	265 53 45	ns	2.0 4.5 6.0	Fig. 8
tPHL/	propagation delay LE to Q		72 26 21	250 50 43		315 63 54	3	375 75 64	ns	2.0 4.5 6.0	Fig. 9
t _{PHL} /	propagation delay PL to Q		63 23 18	190 38 32		240 48 41	76	285 57 48	ns	2.0 4.5 6.0	Fig. 10
t _{PHL} /	propagation delay D7 to Q	longs V	63 23 18	190 38 32	ics", se	240 48 41	ily che	285 57 48	ns OH" 191	2.0 4.5 6.0	CHARACTERIST Fig. 11
tTHL/	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 10 Villideges 180
tw	SH _{CP} pulse width HIGH or LOW	80 16 14	11 4 3	1 is give	100 20 17	tidu s t	120 24 20	rent (Δi	ns does	2.0 4.5 6.0	Fig. 7 addition of selection of the sele
t _W	LE pulse width	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
tw	MR pulse width	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8 04-0 SM
tw	PL pulse width LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
^t rem	removal time	50 10 9	-3 -1 -1		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 12
^t rem	removal time MR to PL	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 12
t _{su}	set-up time D _n to LE	80 16 14	6 2 2		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 13
t _{su}	set-up time D _S to SH _{CP}	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 13
t _{su}	set-up time PL to SHCP	80 16 14	8 3 2		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 14

AC CHARACTERISTICS FOR 74HC

						T _{amb} (°C)			7		TEST CONDITION	ONS
	TEST CONDIT					74H							
SYMBOL	PARAMETER		U	+25			to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS	JOBMY
			min.	typ.	max.	min.	max.	min.	max.				
th	hold time D _n to LE	2.0	4 4 4	-3 -1 -1	(III.) 18	4 4 4	S. m	4 4 4	e l	ns	2.0 4.5 6.0	Fig. 13	/JH8
t _h	hold time D _S to SH _{CP}	6.0 2.0 4.5	2 2 2	-8 -3 -2		2 2 2	ě	2 2 2	52	ns	2.0 4.5 6.0	Fig. 13	PUN
t _h	hold time PL to SH _{CP}	6.0 2.0 4.6	2 2 2	-8 -3 -2	3	2 2 2	2	2 2 2	7	ns	2.0 4.5 6.0	Fig. 14	/ыня
f _{max}	maximum pu SH _{CP}	lse frequency	6.0 30 35	30 90 107		4.8 24 28	C	4.0 20 24	8 8	MHz	2.0 4.5 6.0	Fig. 7	, JHS

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT	1.0 1.0				
DS Dn PL, MR LE, SHCP	0.25 0.40 1.50	2.0				
EE, SHICP	Fig. 10	2.5 4.5 8.0				

AC CHARACTERISTICS FOR 74HCT

GND = 0 V: tr = tf = 6 ns: C1 = 50 pF

					T _{amb} (°C)					TEST CONDITIONS
					74HC	Т				om ¹ /1	
SYMBOL	PARAMETER	TURNI	+25		-40	to +85	-40 t	+125	UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} /	propagation delay SH _{CP} to Q	TURTU	20	35		44		53	ns	4.5	Fig. 7
^t PHL	propagation delay MR to Q		25	42		53	VORTES.	63	ns	4.5	Fig. 8
tPHL/	propagation delay LE to Ω	notew	31	53		66	атио О	80	ns	4.5	Fig. 9
^t PHL/ ^t PLH	propagation delays to be ve PL to Q	leb no	27	46		58	misson	69	ns	4.5	Fig. 10
t _{PHL} /	propagation delay D7 to Q		28	49		61		74	ns	4.5	Fig. 11
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig. 10
tw	SH _{CP} pulse width HIGH or LOW	16	6		20		24		ns	4.5	Fig. 7
tw	LE pulse width	16	7		20		24		ns	4.5	Fig. 9
tw	MR pulse width	20	11		25		30	- 1885	ns	4.5	Fig. 8
tW	PL pulse width	18	9	aret	23		27		ns	4.5	Fig. 10
^t rem	removal time MR to SHCP	10	-1		13		15		ns	4.5	Fig. 12
^t rem	removal time of polyworks in MR to PL	20	9	Pig. prog	25		30	0 01 100	ns	4.5	Fig. 14
t _{su}	set-up time D _n to LE	16	5	5(0.1)	20		24	, NUUN	ns	4.5	Fig. 13
t _{su}	set-up time DS to SHCP	16	5		20		24		ns	4.5	Fig. 13
t _{su}	set-up time PL to SHCP	16	3		20		24		ns	4.5	Fig. 12
th	hold time D _n to LE	4	-2		4		4	1	ns	4.5	Fig. 13
^t h	hold time DS to SHCP	2	-4		2		2	11007-00-	ns	4.5	Fig. 13
th	hold time PL to SH _{CP}	2	-3		2		2		ns	4.5	Fig. 14
f _{max}	maximum pulse frequency	30	72		24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

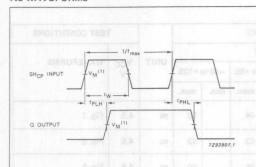


Fig. 7 Waveforms showing the SH $_{CP}$ input to Q output propagation delays, the SH $_{CP}$ pulse width and maximum clock pulse frequency.

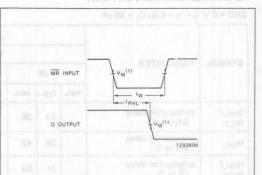


Fig. 8 Waveforms showing the \overline{MR} input to Q output propagation delay and the \overline{MR} pulse width.

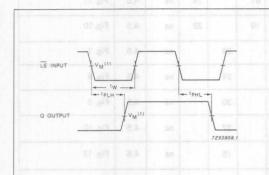


Fig. 9 Waveforms showing the $\overline{\text{LE}}$ input to Q output propagation delays and the $\overline{\text{LE}}$ pulse width.

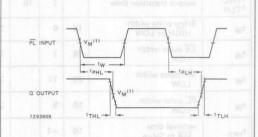


Fig. 10 Waveforms showing the $\overline{\text{PL}}$ input to Q output propagation delays, $\overline{\text{PL}}$ pulse width and output transition times.

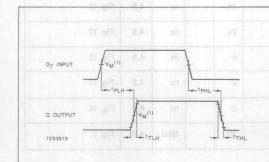


Fig. 11 Waveforms showing the D₇ input to Q output propagation delays and output transition times.

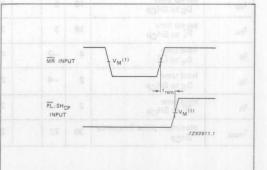


Fig. 12 Waveforms showing the $\overline{\text{MR}}$ input to $\overline{\text{PL}}$, SH_{CP} removal times.

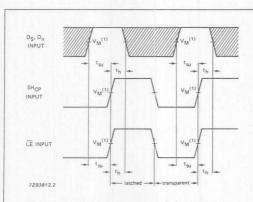
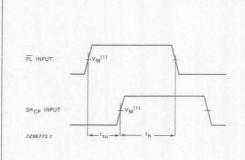


Fig. 13 Waveforms showing hold and set-up times for DS, Dn inputs to SHCP, $\overline{\text{LE}}$ inputs.

Note to Fig. 13

The shaded areas indicate when the input is permitted to change for predictable output performance.



 $\overline{\text{PL}}$.14 Waveforms showing set-up and hold times for $\overline{\text{PL}}$ input to SHCP input.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3$ V; $V_I = GND$ to 3 V.

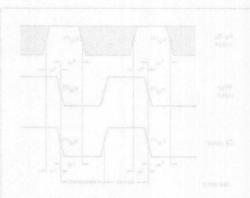


Fig. 13. Waveforms showing hold and set-up nimes for Dc. Dc. inputs to Stirre, LE inputs.

St. self-et etolf

The shaded arees indicate when the input is p chance har emiliated output performance.

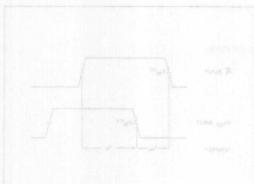


Fig. 14. Waveforms showing set-up and hold times for PL input to SHgp input.

contribution CA of each

(1) HC : VM = 50%, V1 = GNB to VCC HCT VM = 13V V1 = GND to 3V.

reference 74HC/HCT7731

FEATURES

- Frequency range DC to 100 MHz.
- · Separate serial data inputs
- Cascadable
- Functionally compatible with HEF 4731
- · Includes recycling mode
- · Output capability: Standard
- · Icc category: LSI.

APPLICATIONS

- Data storage
- · Delay line.

GENERAL DESCRIPTION

The HC/HCT7731 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The HC/HCT7731 are quad 64-bit static shift registers with a recycling mode. Each register has separate data inputs Da to Da, clock inputs CP, to CP, and data outputs Q, to Q. Data shifts one place towards the output, each LOW to HIGH transition of the clock pulse. Each recycling mode input controls two registers REC_{ab} for registers A and B and REC_{cd} for registers C and D. When the REC input is HIGH, the device is in the recycling mode and data at the output is shifted back into the input of the register, so after 64 clock pulses the contents of a register is again in its original position. This enables the user to tap off data from any position. When the REC input is LOW external data can be shifted in.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25 \, ^{\circ}\text{C}$; $t_r = t_f = 6 \, \text{ns}$.

SYMBOL	PARAMETER	CONDITIONS	T	YP.	UNIT
STIVIBUL	PARAMETER	CONDITIONS	НС	НСТ	DOM
t _{PHL} /t _{PLH}	propagation delay CP _{a-d} to Q _{a-d}	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	15	20	ns
f _{max}	maximum clock frequency	enuarg 8	100	100	MHz
Cı	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per register	notes 1, 2 and 3	58	61	pF

Notes

 C_{PD} is used to determine the dynamic power dissipation (P_{D} in μW):

$$P_{D} = (C_{PD} \times V_{CC}^{2} \times f_{i}) + (C_{L} + V_{CC}^{2} \times f_{o}) + (I_{pull-up} \times V_{CC})$$

where:

 f_i = input frequency in MHz.

f_o = output frequency in MHz.

V_{cc} = supply voltage in V.

C_L = output load capacitance in pF.

I_{pull-up} = pull-up currents in μA.

For HC the condition is $V_1 = GND$ to V_{cc}

For HCT the condition is $V_1 = GND$ to $V_{CC} - 1.5 V$.

See also power dissipation information.

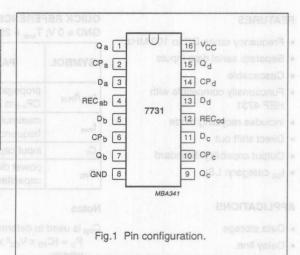
ORDERING INFORMATION

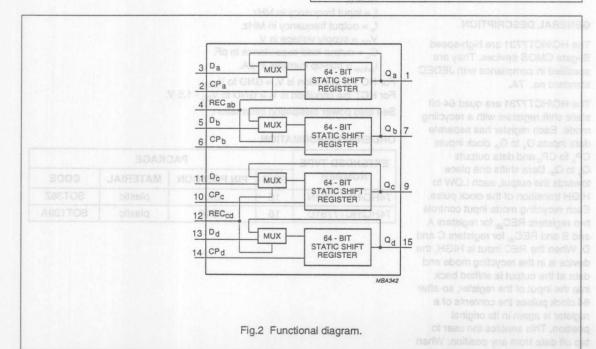
EXTENDED TYPE	PACKAGE								
NUMBER	PINS	PIN POSITION	MATERIAL	CODE					
74HC/HCT7731N	16	DIL	plastic	SOT38Z					
74HC/HCT7731D	16	SO16	plastic	SOT109A					

resigner thing of 74HC/HCT7731

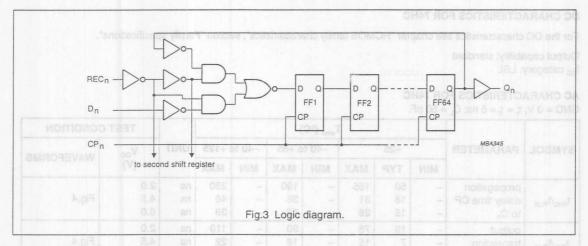
PINNING

SYMBOL	PIN	DESCRIPTION				
Q _a to Q _d	1, 7, 9, 15	data outputs				
CP _a to CP _d	2, 6, 10, 14	clock inputs				
D _a to D _d	3, 5, 11, 13	data inputs				
REC _{ab} , REC _{od}	4, 12	recycled enable input				
GND	8 100	ground (0 V)				
V _{cc}	16	positive supply				





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FUNCTION TABLE

INP	UT	OUTPUT
REC	CP	MODE
L	1	shift
Н	A.n.= ↑	recycle

Notes to Function Table

- 1. L = LOW voltage level
- 2. H = HIGH voltage Level
- 3

↑ = LOW-to-HIGH CP transistion								

retailer thirds o74HC/HCT7731)

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard I_{cc} category: LSI.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_1 = t_2 = 6$ ns; $C_1 = 50$ pF.

			T _{amb} (°C)							TEST CONDITION	
SYMBOL PAR	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{cc}	PO MANAGERA
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	nd shift re	0003 0(V)	WAVEFORMS
t _{PHL} /t _{PLH}	propagation delay time CP to Q _n	-	50 18 15	155 31 26	- - manpait	190 38 32	- - - (即用	230 46 39	ns ns ns	2.0 4.5 6.0	Fig.4
+ /4	output	-	19	75 15	-	90	-	110	ns	2.0 4.5	Fig. 4
t _{THL} /t _{TLH}	transistion time	_	6	13	_	15	-	19	ns ns	6.0	Fig.4
t _w	clock pulse width HIGH or LOW	80 16 14	19 7 6	-	100 20 17	-	120 24 20	-	ns ug ns ns	2.0 4.5 6.0	Fig.4 OBA
t _{su}	set-up time D _n to CP _n	60 12 10	8 3 3	-	75 15 13	- - -	90 18 15	- - -	ns ns elo	2.0 4.5 6.0	Fig.4
t _{su}	set-up time REC _n to CP _n	75 15 13	22 8 7	- - -	90 18 15	- - -	110 22 19	- - -	ns ns ns	2.0 4.5 6.0	Fig.5
t _h	hold time D _n to CP _n	25 5 4	-3 -1 -1	- - -	30 6 5	-	35 7 6	- - -	ns ns ns	2.0 4.5 6.0	Fig.4
t _h	hold time REC _n to CP _n	10 2 2	-8 -3 -3	-	10 2 2	-	15 3 3	- - -	ns ns ns	2.0 4.5 6.0	Fig.5
f _{max}	maximum clock pulse frequency	6 30 35	26 78 93	_ _ _	4.8 24 28	-	4 20 23	- - -	MHz MHz MHz	2.0 4.5 6.0	Fig.4 (note 1)

Note to 74HC AC Characteristics

1. The maximum power dissipation has to be observed. See power dissipation information.

UNIT LOAD COEFFICIENT

INPUT	UNIT LOAD COEFFICIENT
CP _n	0.7
REC _n	0.4
D _n	0.5

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Notes to HCT DC Characteristics

- 1. The RS input has CMOS input switching levels.
- 2. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in Table 1.

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF.$

	-10	115,			T _{amb} (°C	c) ·				TES	T CONDITION
SYMBOL	PARAMETER		+25		-40 t	o +85	-40 to	+125		V _{cc}	WAVEFORMO
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	34 80	(V)	WAVEFORMS
t _{PHL} /t _{PLH}	propagation delay time CP to Q _n	- J£9	24	42	- H.	52	-	63	ns	4.5	Fig.4
t _{THL} /t _{TLH}	output transmission time	-	7	15	TAY .	18	-	22	ns	4.5	Fig.4
t _w	clock pulse width HIGH or LOW	16	7 _H	-4	20	-	24	-	ns	4.5	Fig.4
t _{su}	set-up time D _n to CP _n	12	3	-	15	-	18	-	ns	4.5	Fig.4
t _{su}	set-up time REC _n to CP _n	15	6	-	18	-	22	-	ns	2	Fig.5
thens b	hold time D _n to CP _n	5 (0)	0	o l- tugn	6	and di	7000	the cto	ns	2	Fig.4
t _h	hold time REC _n to CP _n	2	-3	20mit i	2	11_	3	-	ns	4.5	Fig.5
f _{max}	maximum clock pulse frequency	30	80	-	24	-	20	-	MHz	4.5	Fig.4 (note 1)

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AC WAVEFORMS

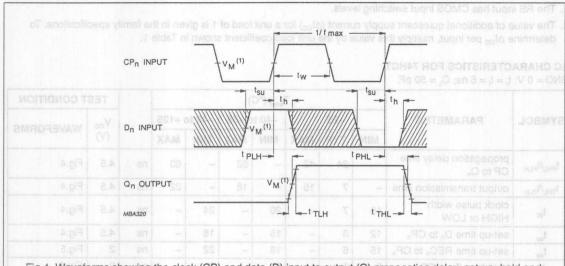


Fig.4 Waveforms showing the clock (CP) and data (D) input to output (Q) propagation delay, set-up, hold and transition times.

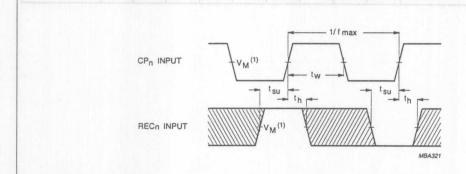


Fig.5 Waveforms showing the clock (CP) to recycle (REC) set-up and hold times.

Note to AC Waveforms

(1) HC: $V_M = 50\%$; $V_I = GND$ to V_{CC}

 $V_M = 1.3 \text{ V}; V_I = \text{GND to 3 V}.$

74HC/HCT7731

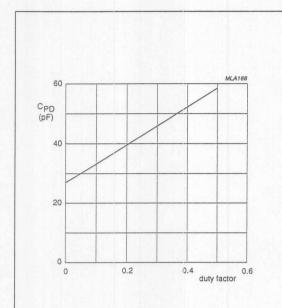


Fig.6 C_{PD} as a function of the duty factor.

POWER DISSIPATION INFORMATION

The power dissipation per register operating at the same frequency is given by:

$$P_D = (C_{PD} \times V_{CC}^2 \times f_i) + (C_L + V_{CC}^2 \times f_o) + (I_{puil-up} \times V_{CC})$$

f_i = clock input frequency

f_o = data output frequency

C_L = output load capacitance in pF

V_{cc} = power supply voltage in V.

As P_D also depends on the frequency at which the contents of the internal bits are changing, the value of C_{PD} is a function of the duty factor (d_f) being the ration between data and clock frequency, see Fig.6.

Example:

f: = 12 MHz

 $f_0 = 3 MHz$

 $C_L = 25 pF$

 $V_{cc} = 5 V$

 $d_t = 3/12 = 0.25$

 $C_{PD} = 42.5 \, pF$

 $P_D = (42.5 \times 5^2 \times 12) + (25 \times 5^2 \times 3) = 14625 \mu W$

As the maximum allowable power dissipation in an SO package at T_{amb} = 125 °C is 60 mW, it is allowed to apply 4 registers at the same time under these conditions.

74HC/HCT7731

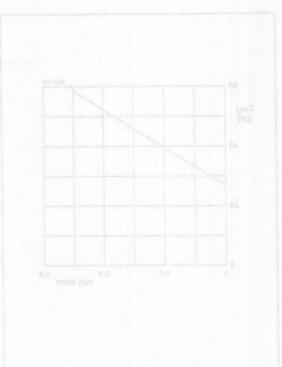


Fig.6 Cen as a function of the duty factor.

POWER DISSIPATION INFORMATION

The power dissipation per register operating at the same frequency is given by:

$$P_0 = (C_{PQ} \times V_{QQ}^2 \times f) + (C_1 + V_{QQ}^2 \times f_0) + (I_{collect} \times V_{QQ})$$

- = clock input frequency
- f. = data output frequency
- C. = output load capacitance in of
 - V_{co} = power supply voltage in V.

As P_o also depends on the frequency at which the contents of the internal bits are changing, the value of $C_{\rm PO}$ is a function of the duty factor (d,) being the ration between data and clock frequency see Fig.6.

elomax3

- sHM SI = 1
- SHM 6 = 1
 - To as a co
 - V3 = 50V
- $d_{\rm c} = 3/12 = 0.25$
 - Con = 12.5 pF

P. = (42.5 x 52 x 12) + (25 x 52 x 3) = 14625 uW

As the maximum allowable power dissipation in an SD package at T_{abo} = 125 °C is 60 mW, it is allowed to apply 4 recestors at the same time under these conditions

SUPERSEDES DATA OF MARCH 1988 NINE WIDE SCHMITT TRIGGER BUFFER/LINE DRIVER; INVERTING

FEATURES

- Schmitt trigger action on all data inputs
- Output capability: standard
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT9014 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT9014 are nine wide Schmitt trigger inverting buffer/line drivers with Schmitt trigger inputs. These inputs transform slowly changing input signals into sharply defined jitter-free output signals.

The "9014" is identical to the "9015" but has inverting inputs.

SYMBOL	PARAMETER	CONDITIONS	TYF	PICAL	UNIT
STINIBUL	PARAMETER	CONDITIONS	нс	нст	UNIT
t _{PHL} / t _{PLH}	propagation delay A_n to \overline{Y}_n	C _L = 15 pF V _{CC} = 5 V	12	13	ns
CI	input capacitance	81 8₹	3.5	3.5	pF
C _{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	32	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

 $PD = CPD \times VCC^2 \times f_i + \Sigma (CL \times VCC^2 \times f_0)$ where:

f_i = input frequency in MHz f_o = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

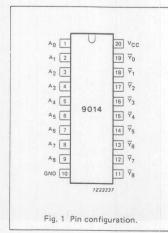
2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V 100 land to 10

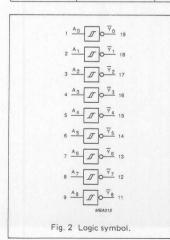
PACKAGE OUTLINES

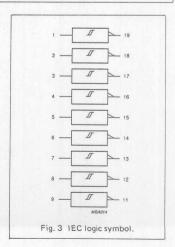
20-lead DIL; plastic (SOT146). 20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTIO	ON TO THE REAL PROPERTY.
1, 2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₈	data inputs	H
10	GND	ground (0 V)	
19, 18, 17, 16, 15, 14, 13, 12, 11	\overline{Y}_0 to \overline{Y}_8	data outputs	
20	Vcc	positive supply voltage	







SUPERSEDES DATA OF MARCH 1988 NINE WIDE SCHMITT TRIGGER BUFFER/LINE DRIVER: INVERTING

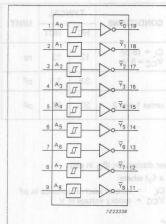
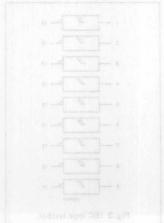


Fig. 5 Logic diagram (one Schmitt trigger).

Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS	OUTPUTS	
An	∇ _n	
L H	H L ziugrii eteb	1, 2, 3, 4, 5, 6, 7, 8, 9 Ag to Ag
H = HIGH voltage level L = LOW voltage level		
E EOW Voltage level		







GENERAL DESCRIPTION, Y

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard

ICC category: MSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are refered to GND (ground = 0 V)

	wolad alder and	TINON T	de dinas	postfile	amb (OC)	lue by	ev sinis va		TES	CONDITIONS
SYMBOL	PARAMETER				74H0				UNIT	Vac	WAVEFORMS
OTHIDOL	TANAMETER		+25		-40	to +85	-40	to+125	OIVII	V	HARDO
		min.	typ.	max.	min.	max.	min.	max.			0.3
V _{T+}	positive-going threshold	0.70 1.75 2.30	2.37	1.50 3.15 4.20	0.70 1.75 2.30	1.50 3.15 4.20	1.75	1.50 3.15 4.20	V som	2.0 4.5 6.0	Figs 6 and 7
VT_SMOI	negative-going threshold	0.30 1.35 1.80	1.80	1.10 2.40 3.30	1.35	1.10 2.40 3.30	1.35	1.10 2.40 3.30	V	2.0 4.5 6.0	Figs 6 and 7
V _H	hysteresis (V _{T+} -V _T _)	0.2 0.4 0.5	0.43 0.57 0.68	1.00	0.40	0.80 1.00 1.10	0.40	0.80 1.00 1.10	V	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	V 5.5 Figs to and	7.3		0 77	amb (oc)			Dionyen	TES	TCONDITIONS
SYMBOL	PARAMETER	8.0		9.	74H	3 8.0	1 44.6	0.2	UNIT	Vcc	WAVEFORMS
			+25		-40 to +85		-40	to+125		V	
		min.	typ.	max.	min.	max.	min.	max.	3.74467	03.20	HARACTERISTI
tPHL/	propagation delay $A_n \text{ to } \overline{Y}_n$		33 12 10	105 21 18	pol du	130 26 22		160 32 27	3q 08 = ns	2.0 4.5 6.0	8 = 11 = 11 (V 0 = Fig.8
tTHL/	output transition time	+128	19 7 6	75 15 13	01 0A-	95 19 16	-26	110 22 19	ns	2.0 4.5 6.0	Fig.8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard

ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
An	0.3

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are refered to GND (ground = 0 V)

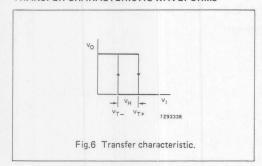
	V 4.5 Figs 6.and 6.0	04.5	1.35	D10	amb (oC)	1,80	1.35	biorizan	TES	T CONDITIONS
		- 000			74H	CT					
SYMBOL	PARAMETER	00.1	+25	00.	-40	to +85	-40	to +125	UNIT	V CC	WAVEFORMS
	0.8	min.	typ.	max.	min.	max.	min.	max.			
V _{T+}	positive-going threshold	0.9	1.50 1.70		0.9	2.0	0.9	2.0	VIIV	4.5 5.5	Figs 6 and 7
T-svoi	negative-going threshold	0.7	1.06 1.27		0.7	1.4 1.7	0.7	1.4 2.7	V	4.5 5.5	Figs 6 and 7
VH ama	hysteresis (V _{T+} - V _{T-})	0.2	0.44		0.2	0.8	0.2	0.8	V	4.5 5.5	Figs 6 and 7

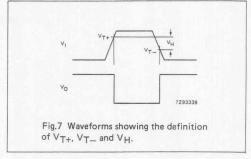
AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

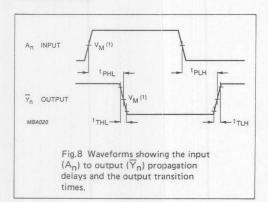
	0.8	1 7		1	amb (oC)				TES	T CONDITIONS
SYMBOL	PARAMETER	nt		1 2	74H	CT	c .		UNIT	Vac	WAVEFORMS
STNIBOL	ns 4,5 Fig.8	2 -	+25	6	-40	to +85	-40	to +125	smit	V	WAVEFORING
	0.6	min.	typ.	max.	min.	max.	min.	max.			
tPHL/	propagation delay A_n to \overline{Y}_n		19	32		40		48	ns	4.5	Fig.8
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig.8

TRANSFER CHARACTERISTIC WAVEFORMS





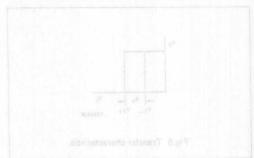
AC WAVEFORMS



Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

TRANSPER CHARACTERISTIC WAVEFORMS



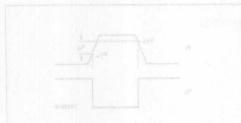
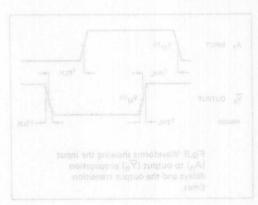


Fig.7 Waveforms showing the definition of VT+, VT+, and Vu,

AC WAVEFORM



Note to AC waveforms: 1) HC: $V_{M} = 50\%$; $V_{I} = GND$ to V_{CC} HCT: $V_{M} = 1.3 V$; $V_{I} = GND$ to 3 V

SUPERSEDES DATA OF MARCH 1988 NINE WIDE SCHMITT TRIGGER BUFFER/LINE DRIVER

FEATURES

- Schmitt trigger action on all data inputs
- Output capability: standard
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT9015 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT9015 are nine wide Schmitt trigger buffer/line drivers with Schmitt trigger inputs. These inputs transform slowly changing input signals into sharply defined jitter-free output signals.

The "9015" is identical to the "9014" but has non-inverting inputs.

01/14001	DADAMETED	CONDITIONS	TYF	PICAL	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
tPHL/ tPLH	propagation delay A _n to Y _n	C _L = 15 pF V _{CC} = 5 V	12	13	ns
CI	input capacitance	****	3.5	3.5	pF
C _P D	power dissipation capacitance per buffer	notes 1 and 2	30	32	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

- f; = input frequency in MHz fo = output frequency in MHz
- CL = output load capacitance in pF VCC = supply voltage in V
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} 1.5 V

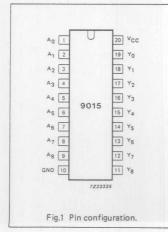
PACKAGE OUTLINES

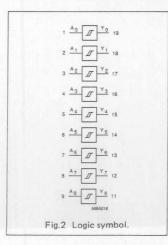
20-lead DIL; plastic (SOT146).

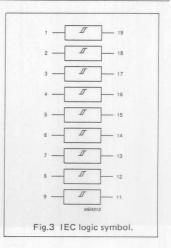
20-lead mini-pack; plastic (SO20; SOT163A).

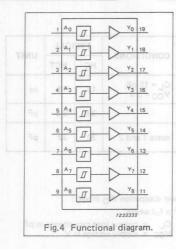
PIN DESCRIPTION

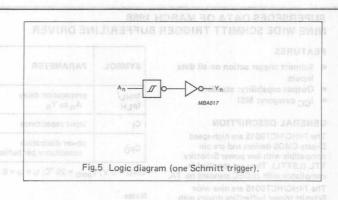
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₈	data inputs
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12, 11	Y ₀ to Y ₈	data outputs
20	Vcc	positive supply voltage







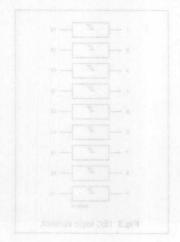




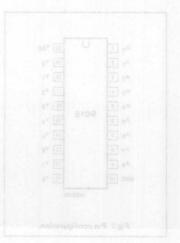
FUNCTION TABLE

INPUTS	OUTPUTS		
An	Yn		
L H	L		

Н	н	
H = HIGH voltage I	NAME AND PUNCTI lave	
L = LOW voltage le	data inputs	







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Transfer characteristics are given below.

Output capability: standard ICC category: MSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are referred to GND (ground = 0 V)

	world alde) and it awi	ONE NOB		Tosa c	amb (a Aldistn	n Jugni	TES	TCONDITIONS		
01/14001	DADAMETED		74HC							QUI	WAVEFORMS
SYMBOL P	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V CC	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			An 0.2
V _{T+}	positive-going threshold	2000		1000000	0.70 1.75 2.30	1.50 3.15 4.20	0.70 1.75 2.30		VEIAET	2.0 4.5 6.0	Figs 6 and 7
V _T OITION	negative-going threshold		0.70 1.80 2.43		0.30 1.35 1.80	1.10 2.40 3.30		1.10 2.40 3.30	V	2.0 4.5 6.0	Figs 6 and 7
V _H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.4 0.5	0.43 0.57 0.68	* 335 GA	100	0.80 1.00 1.10	0.15 0.40 0.50	0.80 1.00 1.10	V	2.0 4.5 6.0	Fig.6

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

	4.5 Figs	T _{amb} (°C)							/= +TV	TEST CONDITIONS	
SYMBOL PA	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	Vcc V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max	AU104	B.S.	E CVD ECIVI
tPHL/	propagation delay An to Yn		33 12 10	105 21 18	mpT	130 26 22		160 32 27	ns	2.0 4.5 6.0	Fig.8
tTHL/ tTLH	output transition time	tios 0.5 em .nin	19 7 6	75 15 13	190	95 19 16	7(1)(110 22 19	ns	2.0 4.5 6.0	Fig.8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications. Transfer characteristics are given below.

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
An	0.3

TRANSFER CHARACTERISTICS FOR 74HCT at 8 at 1 at 8 to 5 et 1 blodeside phiopsyllison

Voltages are refered to GND (ground = 0 V)

	40 V 4.5 Figs	36		30 1.	amb (oC)			ing three	TES	T CONDITIONS
	PARAMETER	£ 98,	08.1 08.8 08.174 HCT 64.5 08.1							Vac	WAVEFORMS
	PARAMETER	.15 0.	+25		-40 to +85		-40 to +125		UNIT	V	
	0.8 0.9	min.	typ.	max.	min.	max.	min.	max.			H
V _{T+}	positive-going threshold	0.9	1.50 1.70		0.9	2.0	0.9	2.0	V HOR S	4.5 5.5	Figs 6 and 7
V _T _	negative-going threshold	0.7	1.06 1.27		0.7 0.8	1.4	0.7	1.4	V JO a	4.5 5.5	Figs 6 and 7
VH	hysteresis (V _{T+} -V _{T-})	0.2	0.44 0.44	-	0.2	0.8	0.2	0.8	V	4.5 5.5	Figs 6 and 7

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

SYMBOL PARAMETER	piR 8,8 Fla	T _{amb} (°C)							valeb r	TEST CONDITIONS		
	DADAMETED								UNIT	Y of	WAVEFORMS	
	2.0	+25			-40 to +85		-40 to +125		it apitis	V	A. A. A. A. A. A. A. A. A. A. A. A. A. A	
	0.8	min.	typ.	max.	min.	max.	min.	max.	HE ROLL	1161770	HJT7	
t _{PHL} /	propagation delay An to Yn		18	32		40		48	ns	4.5	Fig.8	
tTHL/ tTLH	output transition time		7	15		19		22	ns	4.5	Fig.8	

TRANSFER CHARACTERISTIC WAVEFORMS

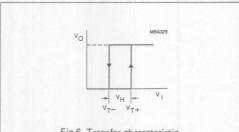


Fig.6 Transfer characteristic.

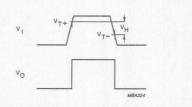


Fig.7 Waveforms showing the definition of V_{T+} , V_{T-} and V_{H} .

AC WAVEFORMS

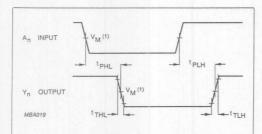


Fig.8 Waveforms showing the input (A_n) to output (Y_n) propagation delays and the output transition times.

Note to AC waveforms

(1) HC: $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to 3 V}$.

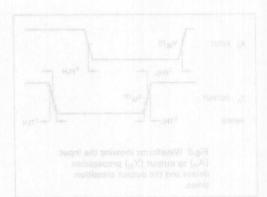
TRANSFER CHARACTERISTIC WAVEFORMS





Fig.7 Waveforms showing the definition of VT4, VT_ and VH.

AC WAVEFORM



MC: V_M = 50%; V_I = GND to V_{CC}.
 HCT: V_M = 1.3 V; V_I = GND to 3 V.

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FEATURES

- · Low power consumption
- Centre frequency up to
 17 MHz (typ.) at V_{cc} = 5.5 V
- Choice of two phase comparators:
 - EXCLUSIVE-OR (PC1)
 - edge-triggered JK flip-flop (PC2)
- No dead zone of PC2.
- Charge pump output on PC2, whose current is set by an external resistor R_b
- Centre frequency tolerance ±10%
- · Excellent VCO linearity
- Low frequency drift with supply voltage and temperature variations
- · On chip bandgap reference
- Glitch free operation of VCO, even at very low frequencies
- Inhibit control for ON/OFF keying and for low standby power consumption
- Operation power supply voltage range 4.5 to 5.5 V
- Zero voltage offset due to op-amp buffering
- · Output capability: standard
- · ICC category: MSI

APPLICATIONS

- FM modulation and demodulation where a small centre frequency tolerance is essential
- Frequency synthesis and multiplication where a low jitter is required (e.g. Video picture-in-picture)

- · Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- · Voltage-to-frequency conversion
- · Motor-speed control.

GENERAL DESCRIPTION

The 74HCT9046A is a high-speed Si-gate CMOS device. It is specified in compliance with JEDEC standard no. 7A.

QUICK REFERENCE DATA

GND = 0 V; $T_{amo} = 25^{\circ}\text{C}$; $t_{i} = t_{i} \le 6 \text{ ns.}$

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
f _o	VCO centre frequency	$C_1 = 40 \text{ pF}$ $R_1 = 4.3 \text{ k}\Omega$ $V_{CC} = 5 \text{ V}$	16	MHz
C ₁	input capacitance	o siuhomah Ot	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	20	pF

Notes

- (1) C_pD is used to determine the dynamic power dissipation (P_D in μW) $P_D = C_pD \times V_{CC}^2 \times f_i + \Sigma (C_1 \times V_{CC}^2 \times f_0)$ where:
- f_i = input frequency in MHz; C_L = output load capacity in pF;
- f_o = output frequency in MHz; V_{CC} = supply voltage in V;
- $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of the outputs.}$
- (2) Applies to the phase comparator section only (inhibit = HIGH). For power dissipation of the VCO and demodulator sections see Figs 24 and 25.

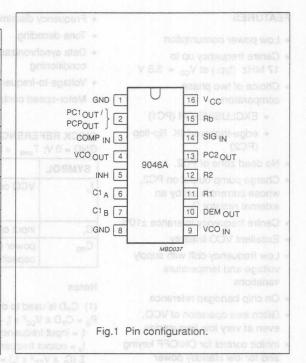
ORDERING INFORMATION

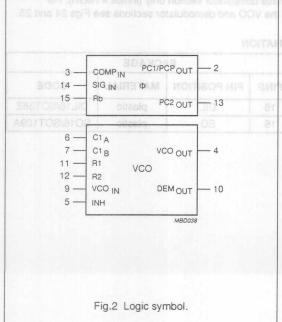
EXTENDED	PACKAGE									
TYPE NUMBER	PINS	PIN POSITION	MATERIAL	CODE						
74HCT9046AP	16	DIL TUO	plastic	DIL16/SOT38Z						
74HCT9046AT	16	SO	plastic	SO16/SOT109A						

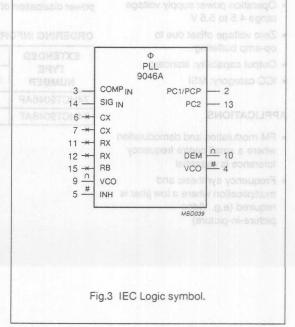
00 / bellownoo gspb 74HCT9046A

GENERAL DESCRIPTION DRINNING

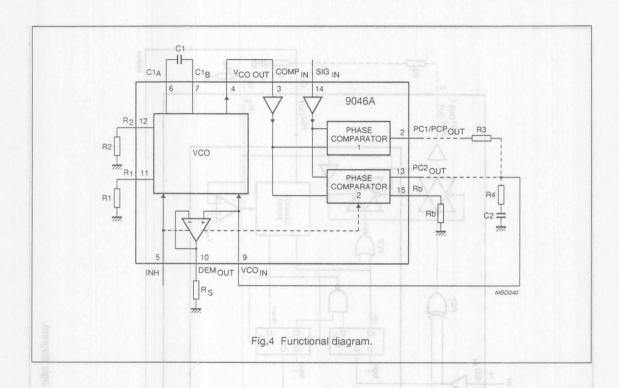
SYMBOL	PIN	DESCRIPTION
GND, SE O HOLE	. dw	ground (0 V) (phase comparators)
PC1 _{out} /PCP _{out}	2	phase comparator 1 output/phase comparator pulse output
COMPIN	3	comparator input
VCO _{OUT}	4	VCO output ATAC
INH	5	inhibit input
C1AU AYT	6	capacitor C1 connection A
C1 _B M at	7	capacitor C1 connection B
GND	8	ground (0 V) (VCO)
VCOIN	9	VCO input
DEM _{OUT}	10	demodulator output
R1	11	resistor R1 connection
R2	12	resistor R2 connection
PC2 _{out}	13	phase comparator 2 output (current source adjustable with R _b)
SIG _{IN}	14	signal input
R _b	15	bias resistor (Rb) connection
V _{cc}	16	positive supply voltage



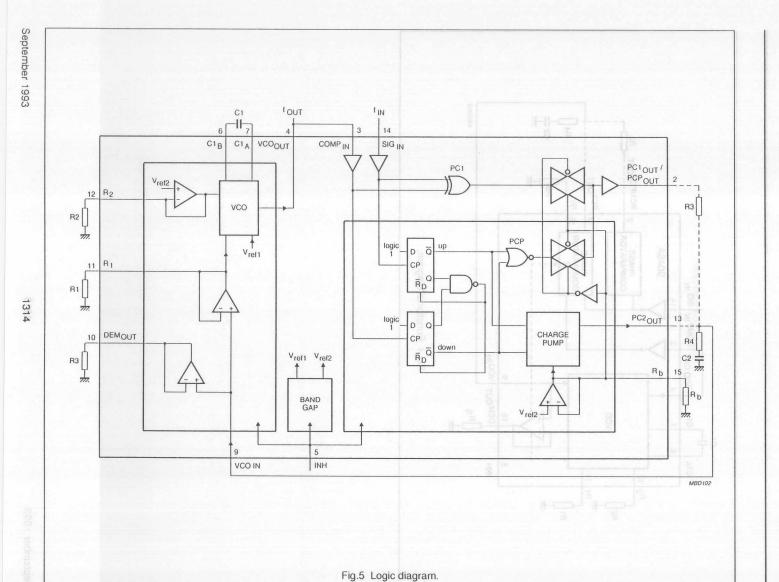




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FUNCTIONAL DESCRIPTION

The 74HCT9046A is a phase-locked-loop circuit that comprises a linear voltage-controlled-oscillator (VCO) and two different phase comparators (PC1 and PC2) with a common signal input amplifier and a common comparator input (see Fig.4). The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the '9046A' forms a second-order loop PLL.

The principle of this phase-locked-loop is based on the familiar HCT4046A. However extra features are built in, allowing very high performance phase-locked-loop applications. This is done, at the expense of PC3, which is skipped in this HCT9046A. The PC2 is equipped with a current source output stage here. Further a bandgap is applied for all internal references, allowing a small centre frequency tolerance. The details are summed up in the next section called: 'Differences which respect to the familiar HCT4046A'. If one is familiar with the HCT4046A already, it will do to read this section only.

DIFFERENCES WITH RESPECT TO THE FAMILIAR HCT4046A

- A centre frequency tolerance of maximum ± 10%
- The on board bandgap sets the internal references resulting in a minimal frequency shift at supply voltage variations and temperature variations

- The value of the frequency offset is determined by an internal reference voltage of 2.5 V instead of V_{CC} - 0.7 V. In this way the offset frequency will not shift over the supply voltage range.
- · A current switch charge pump output on PC2 allows a virtually ideal performance of PC2. The gain of PC2 is independent of the voltage across the low pass filter. Further a passive low pass filter in the loop achieves an active performance now. The influence of the parasitic capacitance of the PC2 output plays no role here, resulting in a true correspondence of the output correction pulse and the phase difference even up to phase differences as small as a few nanoseconds. Because of its linear peerformance without deadzone, higher impedance values for the filter, hence lower C-values, can now be chosen. Correct operation will not be influenced by parasitic capacitances as in the instance with voltage source output of the 4046.
- No PC3 on pin 15 but instead a resistor connected to GND, which sets the load/unload currents of the charge pump (PC2).
- Extra GND pin at pin 1 to allow an excellent FM demodulator performance even at 10 MHz and higher.

- Combined function of pin 2. If pin 15 is tied to V_{CC} (No bias resistor R_b) pin 2 has its familiar function viz. output of PC1. If at pin 15 a resistor (R_b) is connected to GND it is assumed that PC2 has been chosen as phase comparator. Connection of R_b is sensed by internal circuitry and this changes the function of pin 2 into a lock detect output (PCP_{out}) with the same characteristics as PCP_{out} of pin 1 of the well known 74HCT4046A.
- The inhibit function differs. For the HCT4046A a HIGH level at the inhibit input (INH) disables the VCO and demodulator, while a LOW level turns both on. For the 74HCT9046A a HIGH level on the inhibit input disables the whole circuit to allow quiescent supply current testing.

VCO

The VCO requires one external capacitor C1 (between C1_A and C1_B) and one external resistor R1 (between R, and GND) or two external resistors R1 and R2 (between R₁ and GND, and R₂ and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required (see Fig.5). The high input impedance of the VCO simplifies the design of the low-pass filters by giving the

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designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{out}). The DEM_{out} voltage equals that of the VCO input. If DEMOUT is used, a load resistor (Rs) should be connected from pin 10 to GND; if unused, DEMOUT should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input (COMPIN), or connected via a frequency-divider. The VCO output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption. philasi manus vicqui

Phase comparators

The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

PHASE COMPARATOR 1 (PC1)

This is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum

locking range. The transfer characteristic of PC1, assuming ripple (f_r = 2f_i) is suppressed, is:

$$\frac{3\text{K}\sqrt{V_{DEMOUT}}}{\frac{V_{CC}}{\pi}} = \frac{V_{CC}}{\pi} (F_{SIGIN} - F_{COMPIN})$$

where F⊖V_{PCIN} is the demodulator output at pin 10;

V_{PCIN} = V_{PC1OUT} (via low-pass). The phase comparator gain is:

$$\mathsf{Kp} = \frac{V_{CC}}{\pi}(V_r)$$

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIGIN) and the comparator input (COMPIN) as shown in Fig.6. The average of V_{DEMOUT} is equal to 1/2 V_{CC} when there is no signal or noise at SIGIN and with this input the VCO oscillates at the centre frequency (f_o). Typical waveforms for the PC1 loop locked at f, are shown in Fig.7. This figure also shows the actual waveforms across the VCO capacitor at pins 6 and 7 (Vc1a and V_{C1b}) to show the relation between these ramps and the VCO_{OUT} voltage. emus basinu/basi emustas

The frequency capture range (2f_c) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range (2F_c) is

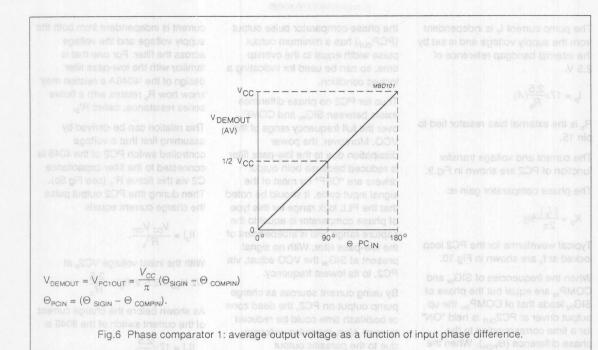
defined as the frequency range of the input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration remains locked even with very noisy input signals. Typical behaviour of this type of phase comparator is that it may lock to input frequencies close to the harmonics of the VCO centre frequency.

ass filter, the '9046A' forms a

PHASE COMPARATOR 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIGin and COMPin are not important. PC2 comprises two D-type flip-flops, control gating and a 3-state output stage with sink and source transistors acting as current sources, henceforth called charge pump output of PC2. The circuit functions as an up-down counter, (Fig.5. where SIG_{in} causes an up-count and COMP_{in} a down count. The current switch charge pump output allows a virtually ideal performance of PC2, due to appliance of some pulse overlap of the up and down signals. See Fig.8a.



SIGN IN SIGN IN VCO OUT SET TO VCO O

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The pump current I_p is independent from the supply voltage and is set by the internal bandgap reference of 2.5 V.

$$I_p = 17 \times \frac{2.5}{R_b}(A)$$

R_b is the external bias resistor tied to pin 15.

The current and voltage transfer function of PC2 are shown in Fig.9.

The phase comparator gain is:

$$K_p = \frac{|I_p|}{2\pi} (A/r)$$

Typical waveforms for the PC2 loop locked at f_0 are shown in Fig.10.

When the frequencies of SIG_{IN} and COMP_{IN} are equal but the phase of SIG_{IN} leads that of COMP_{IN}, the up output driver at PC2_{OUT} is held "ON" for a time corresponding to the phase difference (Θ_{PCIN}). When the phase of SIG_{IN} lags that of COMP_{IN}, the down or sink driver is held "ON".

When the frequency of SIG_{IN} is higher than that of COMPIN, the source output driver is held "ON" for most of the input signal cycle time and for the remainder of the cycle time both drivers are "OFF" (3-state). If the SIG_{IN} frequency is lower than the COMPIN frequency, then it is the sink driver that is held "ON" for most of the cycle. Subsequently the voltage at the capacitor (C2) of the low-pass filter connected to PC2_{OUT} varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition the signal at

the phase comparator pulse output (PCP_{OUT}) has a minimum output pulse width equal to the overlap time, so can be used for indicating a locked condition.

Thus for PC2 no phase difference exists between $SIG_{\rm IN}$ and $COMP_{\rm IN}$ over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both output drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at $SIG_{\rm IN}$ the VCO adjust, via PC2, to its lowest frequency.

By using current sources as charge pump output on PC2, the dead zone or backlash time could be reduced to zero! Also, the pulse widening due to the parasitic output capacitance plays no role here. This enables a linear transfer function, even in the vicinity of the zero crossing. The differences between a current switch charge pump and voltage switch charge pump are shown in Fig. 11.

The design of the low-pass filter is somewhat different when using current sources. The external resistor R3 is no longer present when using PC2 as phase comparator. The current source is set by R_b. A simple capacitor behaves as an ideal integrator now, because the capacitor is charged by a constant current. The transfer function of the voltage switch charge pump may be used. In fact it is even more valid, because the transfer function is no longer restricted for small changes only. Further the

current is independent from both the supply voltage and the voltage across the filter. For one that is familiar with the low-pass filter design of the '4046A a relation may show how R_b relates with a fictive series resistance, called R_3^{\prime} .

This relation can be derived by assuming first that a voltage controlled switch PC2 of the 4046 is connected to the filter capacitance C2 via this fictive R'₃ (see Fig 8b). Then during the PC2 output pulse the charge current equals

$$|I_p| = \frac{V_{CC} V_{C20}}{R'_3}.$$

With the initial voltage VC20 at

$$1/2 \text{ V}_{CC} = 2.5 \text{ V}, \text{ II}_{pl} = \frac{2.5}{R_3}.$$

As shown before the charge current of the current switch of the 9046 is

$$|I_p| = 17 \times \frac{2.5}{R_p}.$$

Hence:

$$R'_3 = \frac{R_b}{17}(\Omega)$$

Using this equivalent resistance R'_3 for the filter design the voltage can now be expressed as a transfer function of PC2; assuming ripple $(f_r = f_i)$ is suppressed, as:

$$K_{PC2OUT} = \frac{5}{4\pi}((v/r)$$

Again this illustrates the supply voltage independent behaviour of PC2.

Examples of PC2 combined with a passive filter are shown in Figs 12 and 13. Fig. 12 shows that PC2 with only a C2 filter behaves as a high-gain filter. For stability the damped version of Fig. 13 with series resistance R4 is preferred.

OOV bellownoo gsp 74HCT9046A

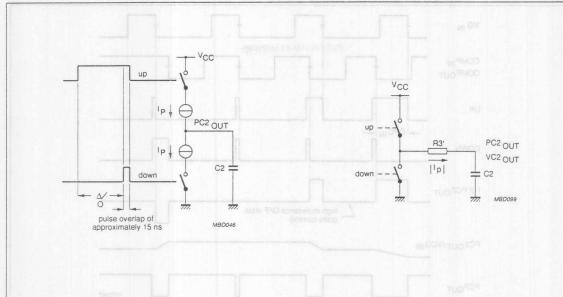


Fig.8 (a) The current switch charge pump output of PC2. At every ΔΘ, even at zero ΔΘ both switches are closed simultaneously for a short period (typically 15 ns). (b) Comparable voltage-controlled switch.

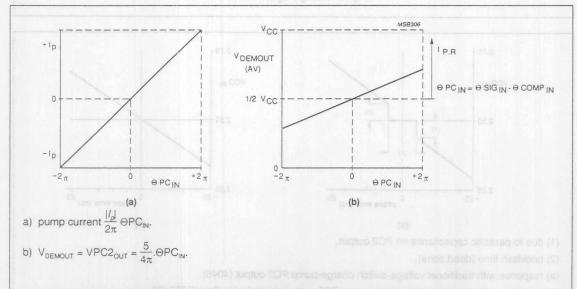
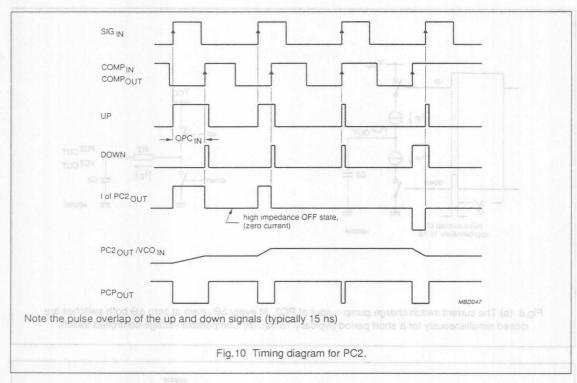
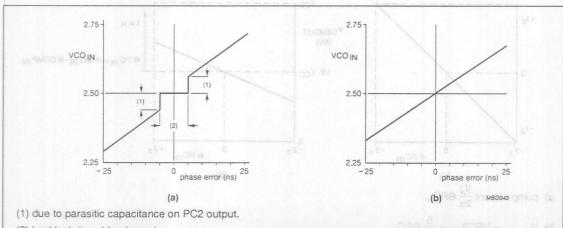


Fig.9 Phase comparator 2. Two kinds of transfer functions may be regarded: the current transfer (a) and the voltage transfer (b). The voltage transfer can be observed at $PC2_{OUT}$ by connecting first a resistance $R = 10 \text{ k}\Omega$ between $PC2_{OUT}$ and $V_{CC}/2$.







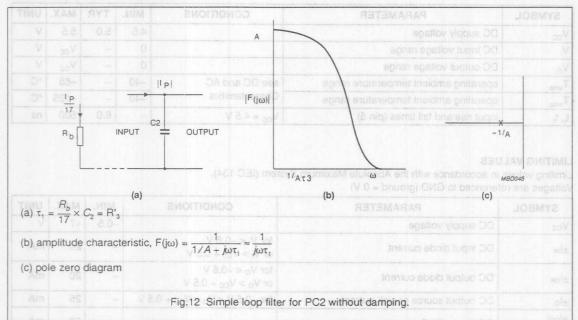
- (2) backlash time (dead zone).
- (a) response with traditional voltage-switch charge-pump PC2 output (4046).
- (b) response with current-switch charge-pump PC2 output as applied in the HCT9046A

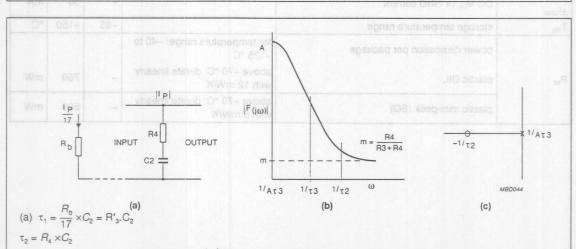
Fig.11 The response of a locked-loop in the vicinity of the zero crossing of the phase error.

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RECOMMENDED OPERATING CONDITIONS FOR 74HCT

LOOP FILTER COMPONENT SELECTION





(b) amplitude characteristic. $F(j\omega) = \frac{1+j\omega\tau_2}{1/A+j\omega\tau_1}$

(c) pole zero diagram

A = DC gain limit, due to leakage.

Fig.13 Simple loop filter for PC2 with damping.

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RECOMMENDED OPERATING CONDITIONS FOR 74HCT

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{cc}	DC supply voltage		4.5	5.0	5.5	V
V ₁	DC input voltage range		0	-	V _{cc}	V
Vo	DC output voltage range		0	-	V _{cc}	V
T _{amb}	operating ambient temperature range	see DC and AC	-40	_	+85	°C
T _{amp}	operating ambient temperature range	Characteristics	-40	-	+125	°C
t _r , t _t	input rise and fall times (pin 5)	V _{CC} = 4.5 V	-	6.0	500	ns

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134). Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Vcc	DC supply voltage		-0.5	+7	V
±lıĸ	DC input diode current	for $V_1 < -0.5 \text{ V}$ or $V_1 > V_{CC} + 0.5 \text{ V}$	chara <u>c</u> te	20	mA
±Ιοκ	DC output diode current	for $V_0 < -0.5 \text{ V}$ or $V_0 > V_{CC} + 0.5 \text{ V}$	lagram	20	mA
±lo	DC output source or sink current	for $-0.5 \text{ V} < \text{V}_0 < \text{V}_{CC} + 0.5 \text{ V}$	-	25	mA
±lcc; ±lgnp	DC V _{CC} or GND current		-	50	mA
T _{stg}	storage temperature range		-65	+150	°C
	power dissipation per package	for temperature range: -40 to +125 °C			
P _{tot}	plastic DIL	above +70 °C: derate linearly with 12 mW/K	-	750	mW
	plastic mini-pack (SO)	above +70 °C: derate linearly with 8 mW/K	-	500	mW

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DC CHARACTERISTICS FOR 74HCT

Quiescent supply current

Voltages are referenced to GND (ground = 0 V).

	TEST CON	T _{amb} (°C)								TEST		
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{cc}	071155	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	bs	(V)	OTHER	
I _{cc}	quiescent supply current (disabled)	V	-	8.0		80.0	2.4	160.0	μA sps	5.5	pin 5 at V _{cc}	
Δl _{cc}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) V _I = V _{CC} -2.1 V	V -	100	360		450	1.9	490	l sge Αμ MP _{IN}	4.5 to 4.5 5.5 6 HE	other inputs at V _{CC} or GND.	

Note

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given above. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the Unit Load Coefficient Table.

	IN	PUT							T LOAD		
Au 09- = of	lor Vic	NH	V	1.0	1.0	~	1.0	0	1.00	PCS	JeV

OOV bellottnoo gsp174HCT9046A

DC CHARACTERISTICS FOR 74HCT

Phase comparator section

Voltages are referenced to GND (ground = 0 V).

	T. I				T _{amb} (°C	()				TEST CONDITION		
SYMBOL	PARAMETER		+25		-40 1	to +85	-0 to	+125	UNIT	V _{cc}	AFV	OTHER
	V. Vac	MIN	TYP	MAX	MIN	MAX	MIN	MAX		(V)	V	OTHER
_{DO} V _{IH} & n	DC coupled HIGH level input voltage SIG _{IN} , COMP _{IN}	3.15	2.4	XAN - 0.0	- NIN	- XAI	5-j	- 100	V V	4.5	jiesceni grent (:	p 20 ¹
	DC coupled LOW level input voltage SIG _{IN} , COMP _{IN}	00:	2.1	1.35	1	- 08	0 38	91	V 1	4.5	Jiesceni Arent p A for un sefficien	
V _{он}	HIGH level output voltage PCPout, PCnout	4.4	4.5		4.4		4.4		V	4.5	V _{IH} or V _{IL}	I _O = -20 μA
V _{OH}	HIGH level output voltage PCP _{OUT} , PC _{nout}	3.98	4.32	d of 1 is licken <u>t</u> s		c) for a sunit_o			Vidibine And Inc.		V _{IH} or V _{IL}	$I_0 = -4.0 \text{ m/s}$
V _{OL}	LOW level output voltage PCP _{OUT} , PC _{nOUT}	1.00 =	0	0.1	-	0.1		0.1	V	4.5	V _{IH} or V _{IL}	Ι ₀ = -20 μΑ
V _{OL}	LOW level output voltage PCP _{OUT} , PC _{nOUT}	_	0.15	0.26	_	0.33	-	0.4	V	4.5	V _{IH} or V _{IL}	l ₀ = -4.0 m/
±I,	input leakage current SIG _{IN} , COMP _{IN}	-	-	30	-	38	-	45	μА	5.5	V _{CC} or GND	
±l _{oz}	3-state OFF-state current PC2 _{OUT}	_	-	0.5	_	5.0	_	10.0	μА	5.5	V _{IH} or V _{IL}	V _O = V _{CC} or GND
R _I	input resistance SIG _{IN} , COMP _{IN}	_	250	-	-	-	-	-	kΩ	4.5	operat $\Delta V_1 = 0$	elf-bias ting point; 0.5 V; gs 14, 15, 16
Rb	resistor range	25	-	250	-	-	-	-	kΩ	4.5		
±lp	charge pump current PC2 _{out}	0.53	1.06	2.12	-	-	-	-	mA	4.5	R ₃ = 4	0 kΩ

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OOV bellottnop asp 74HCT9046A

DC CHARACTERISTICS FOR 74HCT

VCO section

Voltages are referenced to GND (ground = 0 V).

	PARAMETER				T _{amb} (°C		TEST CONDITION					
SYMBOL		+25			-40 1	0 +85	-0 to +125		UNIT	V _{cc}	BMA BA	9 OTHERYS
	ooV MA	MIN	TYP	MAX	MIN	MAX	MIN	MAX		(V)	V ₁	OTHER
V _{IH} S <	DC coupled HIGH level input voltage INH	2.0	1.6	- 1	2.0	- 1	2.0	-	V	4.5 to 5.5	her rain	201 9
V _{IE} uowa V _{IOOVI}	DC coupled LOW level input voltage INH	-	1,2	0.8	-	0.8	-	0.8	V	4.5 to 5.5		
V _{OH}	HIGH level output voltage VCO _{OUT} ,	4.4	4.5	-	4.4	-	4.4	05±	V _	4.5	V _{IH} or V _{IL}	Ι _Ο = -20 μΑ
V _{OH}	HIGH level output voltage VCO _{OUT}	3.98	4.32		3.84	-	3.7	20	V	4.5	V _{IH} or V _{IL}	$I_0 = -4.0 \text{ mA}$
V _{OL}	LOW level output voltage VCO _{OUT}	-	0	0.1		0.1		0.1	V	4.5	V _{IH} or V _{IL}	Ι _O = +20 μΑ
V _{OL}	LOW level output voltage VCO _{OUT}	-	0.15	0.26	-	0.33	-	0.4	V	4.5	V _{IH} or V _{IL}	l _O = +4.0 mA
V _{OL}	LOW level output voltage C1 _A , C1 _B	-	-	0.40	-	0.47	-	0.54	V	4.5	V _{IH} or V _{IL}	l _O = +4.0 mA
±lı	input leakage current INH, VCO _{IN}	3	-	0.1	-	1.0	-	1.0	μА	5.5	V _{CC} or GND	
R1	resistor range	3	-	300	-	-	_	-	kΩ	4.5		
R2	resistor range	3	-	300	-	-	-	-	kΩ	4.5		
C1	Capacitor range	40	-	no limit	-	-	-	-	pF	4.5		
V _{VCOIN}	operating voltage range at VCO _{IN}	1.1 1.1 1.1	-	3.4 3.9 4.4	-	-	-	-	V	4.5 5.0 5.5		over the range specified for R1

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DC CHARACTERISTICS FOR 74HCT

Demodulator section

Voltages are referenced to GND (ground = 0 V).

		TEST		THOIR !	301 - 61	n	T _{amb (°C}) diese T		50		UNIT	TEST CONDITIONS			
SYMBOL	P	PARAME		PARAMETER		+25			-40	to +85	-40	-40 to +125			V _{cc}	OTHER
				MIN	TYP	MAX	MIN	MAX	K MII	N M	AX		(V)	OTHER		
			6.5 5.6	V		2.0		2.0	-	1.6	0.5		val HE	at R _S > 300 kg the leakage		
R _S	resistor range			50	8.0	300	8.0	- 8	8.0	12		kΩ bs	1	current can		
V _{OFF} 05-		et volta O _{IN} to V		- V	±20	44	-	2	-	4.5	4.	mV	V91 H6 14.5 dl -ποΟλ	V _I = V _{VCOIN} = 1/2 V _{CC} ; values taken over R _S range, see Fig.17		
R _o	resi	amic ou stance			25	-	-	-			00.1	Ω	4.5	V _{DEMOUT} = 1/2 V _{CC}		
234, 634	- 01	or V _{IL}			1.0		130		1.0	- 0		flage	TUDOS			

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AC CHARACTERISTICS FOR 74HCT

Phase comparator section

 $GND = 0 V; t_r = t_t = 6 ns; C_t = 50 pF.$

	TEST CO					TEST CONDITION					
SYMBOL	PARAMETER	+125	+25	88+ 01	-40	to +85	-40 to +125		RETER	V _{cc}	SYMBOL
	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		(V)	WAVEFORMS
t _{PHL} /t _{PLH}	propagation delay SIG _{IN} , COMP _{IN} to PCP _{OUT}	-	23	40	30:0	50	_	60	ns	4.5	Fig.18
t _{PHL} /t _{PLH}	propagation delay SIG _{IN} , COMP _{IN} to PCP _{OUT}		35	68	-	85	-	102	ns	4.5	Fig.18
t _{PZH} / t _{PZL}	3-state output enable time SIG _{IN} , COMP _{IN} to PC2 _{OUT}	-	30	56		70		84	ns	4.5	Fig.19
t _{PHZ} / t _{PLZ}	3-state output enable time SIG _{IN} , COMP _{IN} to PC2 _{OUT}	-	36	65	-	81	15.0	98	ns roa =	4.5	Fig.19
t _{THL} /t _{TLH}	output transition time	_	7	15		19	0.4	22	ns	4.5	Fig.18
V _{1(p-p)}	AC coupled input sensitivity (peak-to-peak value) at SIGN _{IN} or COMP _{IN}	-	15	-	-		50		mV	4.5	$f_i = 1 \text{ MHz}$

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AC CHARACTERISTICS FOR 74HCT

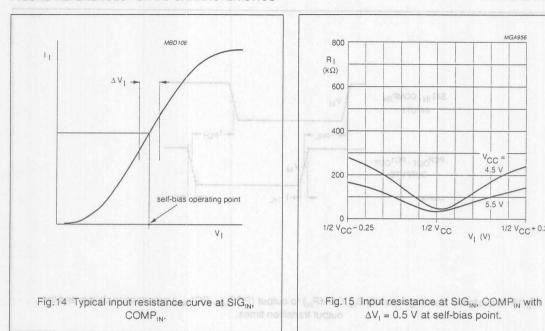
VCO section

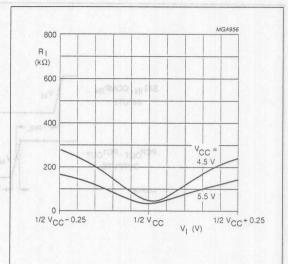
 $GND = 0 V; t_r = t_t = 6 ns; C_L = 50 pF.$

NOITION				(3	T _{amb} (°C)				TEST CONDITION		
SYMBOL	PARAMETER	to +12	01+25	to +85	-40 t	o +85	-40 to +125		A3	V _{cc}	HAS JOSMY	
VEFORMS	Avy (V) X	MIN	TYP	MAX	MIN	MAX	MIN	MAX		(V)	WAVEFORMS	
Δf/T	frequency stability with temperature change	60	_	50	0.06	40	23	_	%/K	noite; of m 4.5 noite; unOl6	$V_{VCOIN} = 1/2 V_{CC};$ recommended range: R1 = 10 k Ω R2 = 10 k Ω C1 = 1 nF see Fig.20	
Δf _{vco} Θ1	centre frequency tolerance	-10		+10	_ =	_ 88	_ 08	-	% 10	5.0	R1 = 10 k Ω ; R2 = 10 k Ω C1 = 1 nF V _{VCOIN} = 3.9 V	
f _o	VCO centre frequency (duty factor = 50%)	11.0	15.0	81	-	85	36 _	-	MHz	4.5	$V_{VCOIN} = 1/2 \ V_{CC};$ $R1 = 4.3 \ k\Omega$ $R2 = \infty$ $C1 = 40 \ pF \ see$ $Fig.21$	
Δf _{VCO}	VCO frequency linearity	22	0.4	19	_	15	7	_	%	4.5 belgu	R1 = 100 kΩ; R2 = ∞ ; C1 = 100 pFsee Figs 22, 23	
δVCO	duty factor at VCO _{OUT}		50				15 -		%	4.5	V ₁₀₋₀₁ (peak-	

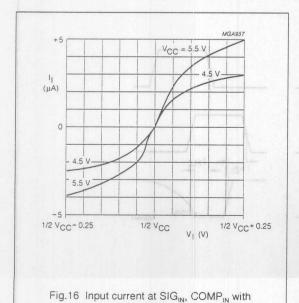
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FIGURE REFERENCES FOR DC CHARACTERISTICS

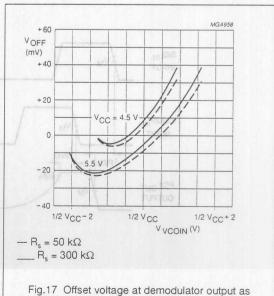




output train $\Delta V_1 = 0.5 \text{ V}$ at self-bias point.



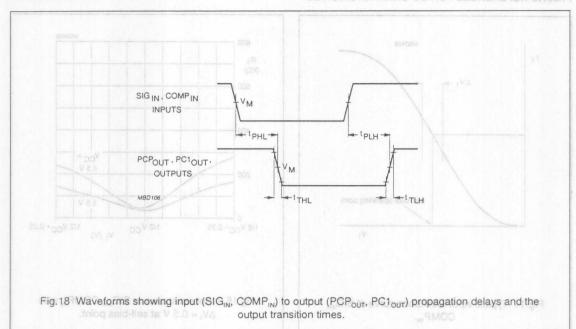
 $\Delta V_1 = 0.5 \text{ V}$ at self-bias point.

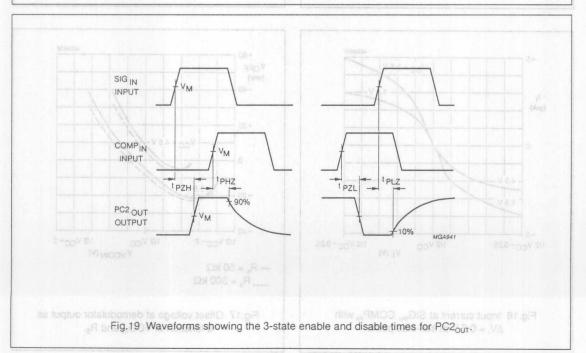


a function of VCO_{IN} and R_s.

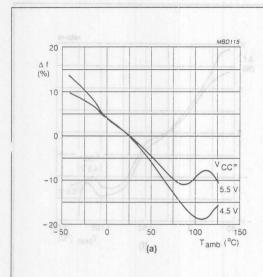
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AC WAVEFORMS





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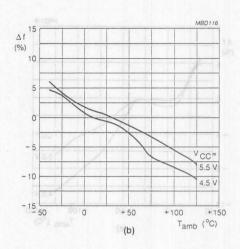
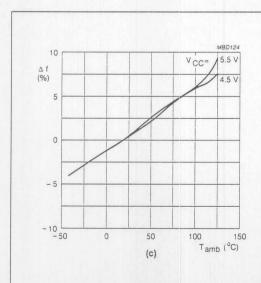


Fig.20 a-b Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.



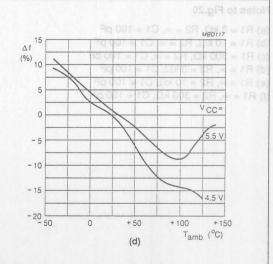
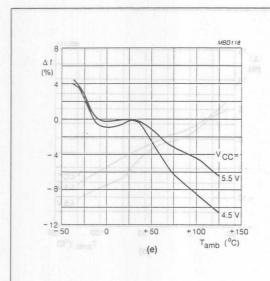


Fig.20 c-d Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.

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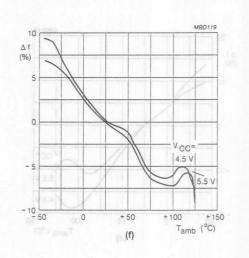


Fig.20 e-f Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.

Notes to Fig.20

(a) R1 = 3 k Ω , R2 = ∞ , C1 = 100 pF

(b) R1 = 10 k Ω , R2 = ∞ , C1 = 100 pF

(c) R1 = 300 k Ω , R2 = ∞ , C1 = 100 pF

(d) R1 = ∞ , R2 = 3 k Ω , C1 = 100 pF

(e) R1 = ∞ , R2 = 10 k Ω , C1 = 100 pF



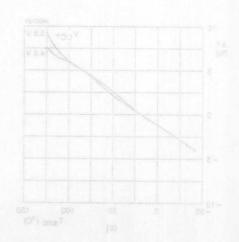
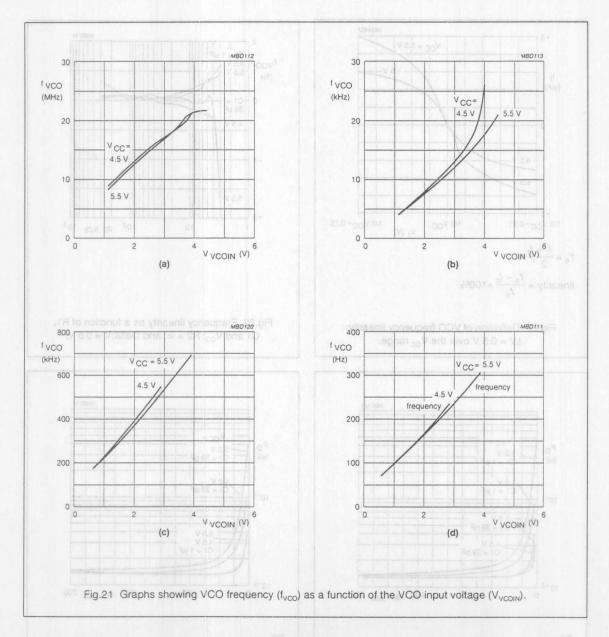


Fig.20 o-d Frequency stability of the VCO as a function of ambient temperature with supply voltage as a





Notes to Fig.21

- (a) R1 = 3 k Ω , C1 = 39 pF.
- (b) R1 = 3 k Ω , C1 = 100 nF.
- (c) $R_1 = 300 \text{ k}\Omega \text{ C1} = 39 \text{ pF}.$
- (d) $R_1 = 300 \text{ k}\Omega \text{ C1} = 100 \text{ nF}.$



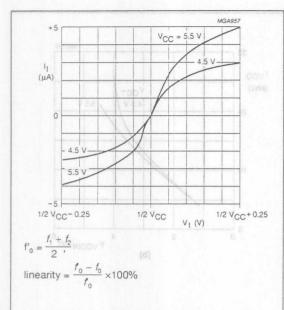


Fig.22 Definition of VCO frequency linearity: $\Delta V = 0.5 \text{ V}$ over the V_{CC} range.

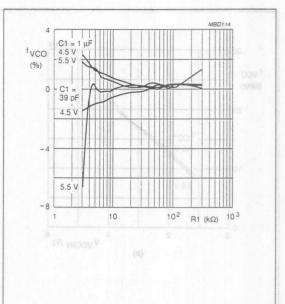


Fig.23 Frequency linearity as a function of R1, C1 and V_{CC} : R2 = ∞ . and Delta; V = 0.5 V.

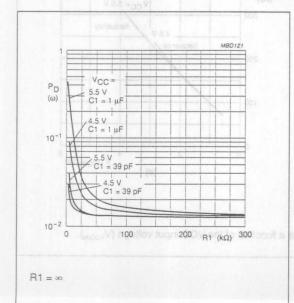
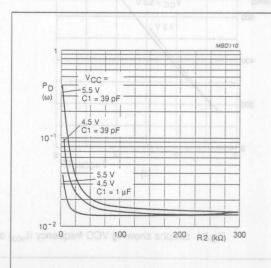


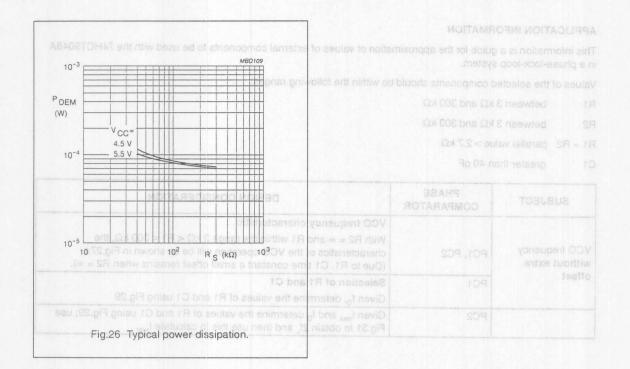
Fig.24 Power dissipation as a function of component values.



R2 = ∞

Fig.25 Power dissipation as a function of component values.

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APPLICATION INFORMATION

This information is a guide for the approximation of values of external components to be used with the 74HCT9046A in a phase-lock-loop system.

Values of the selected components should be within the following ranges:

R1 between $3 k\Omega$ and $300 k\Omega$

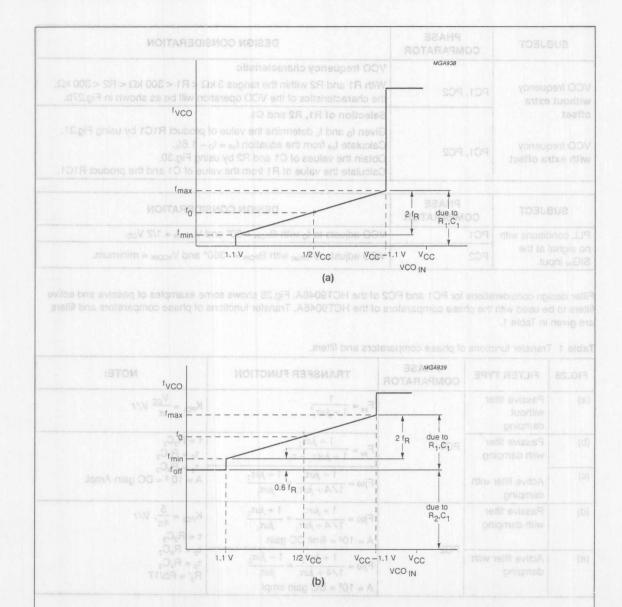
R2 between $3 k\Omega$ and $300 k\Omega$

R1 + R2 parallel value > 2.7 k Ω

C1 greater than 40 pF

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATION						
		VCO frequency characteristic						
VCO frequency PC1, PC2 With F chara	With R2 = ∞ and R1 within the range 3 k Ω < R1 < 300 k Ω , the characteristics of the VCO operation will be as shown in Fig.27a. (Due to R1, C1 time constant a small offset remains when R2 = ∞).							
onset	PC1	Selection of R1 and C1						
		Given fo, determine the values of R1 and C1 using Fig.29						
	PC2	Given f_{max} and f_0 determine the values of R1 and C1 using Fig.29; use Fig.31 to obtain $2f_L$ and then use this to calculate f_{min} .						

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- (a) Operating without offset: f_0 = centre frequency: $2f_L$ = frequency lock range.
- (b) Operating with offset: f_0 = centre frequency: $2f_L$ = frequency lock range.

Fig.27 Frequency characteristic of VCO.



SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATION					
	1260.00	VCO frequency characteristic					
VCO frequency without extra	PC1, PC2	With R1 and R2 within the ranges 3 k Ω < R1 < 300 k Ω < R2 < 300 k Ω , the characteristics of the VCO operation will be as shown in Fig.27b.					
offset		Selection of R1, R2 and C1					
VCO frequency with extra offset	PC1, PC2	Given f_O and f_L determine the value of product R1C1 by using Fig.31. Calculate f_{off} from the equation $f_{off} = f_O - 1.6 f_L$. Obtain the values of C1 and R2 by using Fig.30. Calculate the value of R1 from the value of C1 and the product R1C1.					

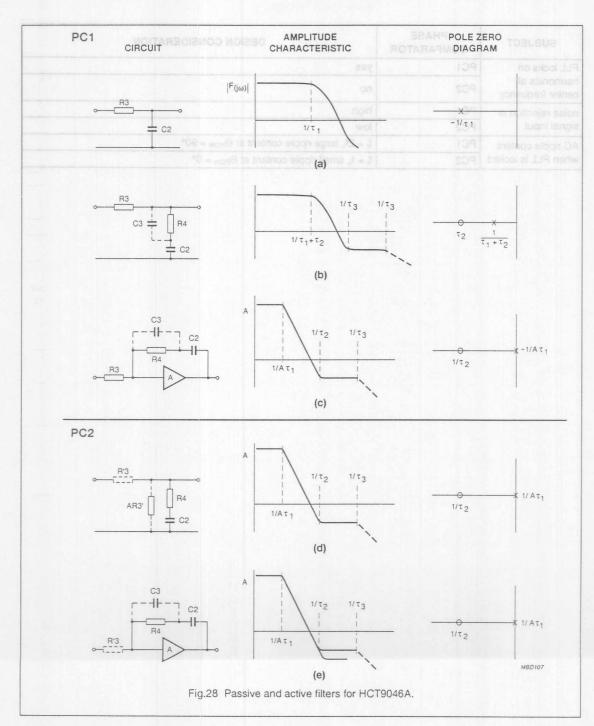
SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATION
PLL conditions with	PC1	VCO adjusts to f_0 with $\Theta_{PCIN} = 90^{\circ}$ and $V_{VCOIN} = 1/2 V_{CC}$.
no signal at the SIG _{IN} input	PC2	VCO adjusts to f_{offset} with $\Theta_{\text{PCIN}} = -360^{\circ}$ and $V_{\text{VCOIN}} = \text{minimum}$.

Filter design considerations for PC1 and PC2 of the HCT9046A. Fig.28 shows some examples of passive and active filters to be used with the phase comparators of the HCT9046A. Transfer functions of phase comparators and filters are given in Table 1.

Table 1 Transfer functions of phase comparators and filters.

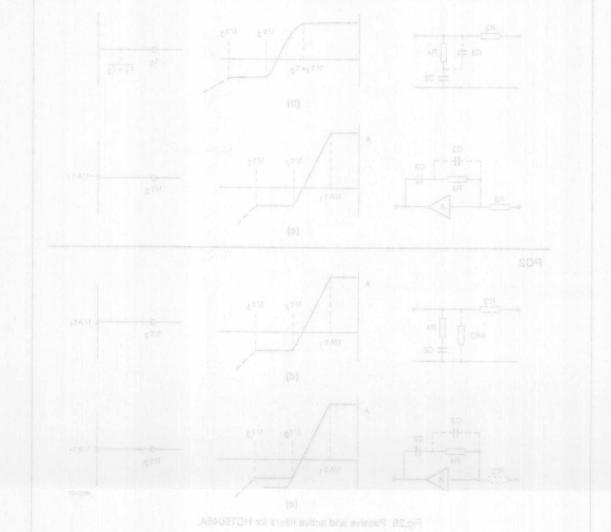
FIG.28	FILTER TYPE	PHASE COMPARATOR	TRANSFER FUNCTION	NOTE:		
(a)	Passive filter without damping		$F_{j\omega} = \frac{1}{1 + j\omega\tau_1};$	$K_{PC1} = \frac{V_{CC}}{\pi} V/r$		
(b)	Passive filter with damping	PC1	$F_{j\omega} = \frac{1 + j\omega\tau_2}{1 + j\omega(\tau_1 + \tau_2)}$	$\tau = R_3 C_2$ $\tau_2 = R_4 C_2$		
(c)	Active filter with damping		$Fj\omega = \frac{1 + j\omega\tau_2}{1/A + j\omega\tau_1} \approx \frac{1 + j\omega\tau_2}{j\omega\tau_1}$	$\tau_3 = R_4C_3$ A = 10 ⁵ = DC gain Ampl.		
(d)	Passive filter with damping	DC2	$Fj\omega = \frac{1 + j\omega\tau_2}{1/A + j\omega\tau_1} \approx \frac{1 + j\omega\tau_2}{j\omega\tau_1}$ $A = 10^5 = \text{limit DC gain}$	$K_{PC2} = \frac{5}{4\pi}. \ V/r$ $\tau = R_3C_2$		
(e) Active filter with damping		PC2	$Fj\omega = \frac{1 + j\omega\tau_2}{1/4 + j\omega\tau_1} \approx \frac{1 + j\omega\tau_2}{j\omega\tau_1}$ $A = 10^5 = DC \text{ gain ampl}$	$\tau_2 = R_4 C_2$ $\tau_3 = R_4 C_3$ $R_3' = Rb/17$		

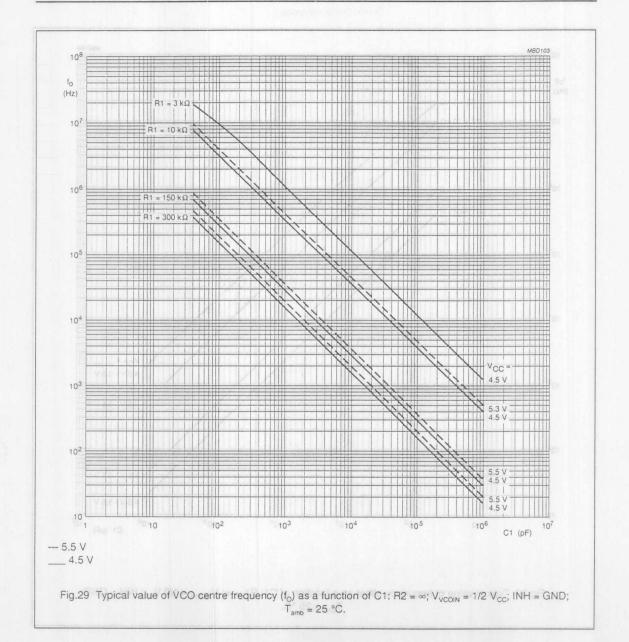
OOV ballownoo gap 74HCT9046A



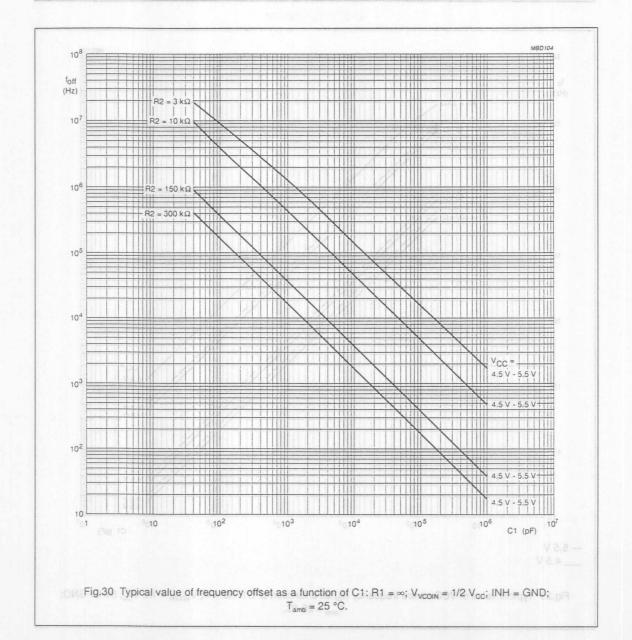
OOV bellottnoo gspb74HCT9046A

SUBJECT MA	COMPARATOR	DESIGN CONSIDERATION TO THE STATE OF THE STA
PLL locks on	PC1	yes
harmonics at centre frequency	PC2	no Rub ³
noise rejection at	PC1	high
signal input	PC2	low / wat was a so the
AC ripple content	PC1	$f_r = 2f_i$, large ripple content at $\Theta_{PCIN} = 90^{\circ}$
when PLL is locked	PC2	$f_r = f_i$, small ripple content at $\Theta_{PCIN} = 0^{\circ}$

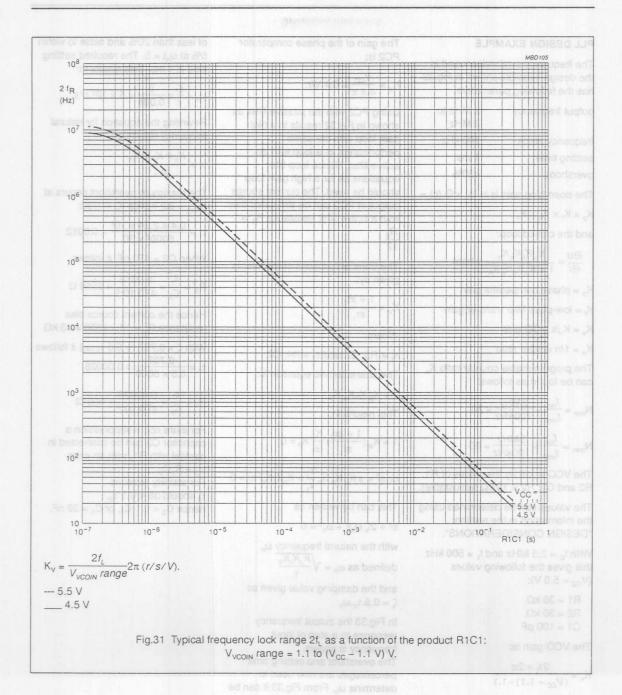




OOV belloving appb74HCT9046A



OOV bellomoo gspl74HCT9046A



OOV bellotings aspl74HCT9046A

PLL DESIGN EXAMPLE

The frequency synthesizer used in the design example shown in Fig.32 has the following parameters:

output frequency : 2 MHz to

3 MHz

frequency steps : 100 kHz settling time : 1 ms

overshoot : <20%

The open loop gain is $H(s) \times G(s) =$

 $K_o \times K_f \times K_o \times K_n$

and the closed loop:

$$\frac{\Theta u}{\Theta i} = \frac{K_{p.}K_{t.}K_{o.}K_{n.}}{1 + K_{p.}K_{t.}K_{o.}K_{n.}}, \text{ where }$$

K_p = phase comparator gain

K_f = low-pass filter transfer gain

K₀ = K_v/s VCO gain

 $K_n = 1/n$ divider ratio

The programmable counter ratio K_n can be found as follows:

$$N_{min} = \frac{f_{out}}{f_{step}} = \frac{2MHZ}{100kHZ} = 20$$

$$N_{\text{max}} = \frac{f_{out}}{f_{step}} = \frac{3MHz}{100kHz} = 30$$

The VCO is set by the values of R1, R2 and C1; R2 = $10 \text{ k}\Omega$ (adjustable).

The values can be determined using the information in the section: "DESIGN CONSIDERATIONS".

With $f_O = 2.5$ MHz and $f_L = 500$ kHz this gives the following values ($V_{CC} = 5.0$ V):

 $R1 = 30 \text{ k}\Omega$

 $R2 = 30 k\Omega$

C1 = 100 pF

The VCO gain is:

$$K_v = \frac{2f_L \times 2\pi}{(V_{CC} - 1.1) - 1.1}$$

$$=\frac{1MHz}{2.8}\times 2\pi \approx \times\, 2.24~.~10^6~r/s/V$$

The gain of the phase comparator PC2 is:

$$K_p = \frac{V_{CC}}{4 \times \pi} = 0.4 \text{ V/r}.$$

Using PC2 with the passive filter as shown in Fig.32 results in a high gain loop with the same performance as a loop with an active filter. Hence loop filter equations as for a high gain loop should be used. The current source output of PC2 can be simulated then with a fictive filter resistance $R_3' = \frac{R_b}{17}$.

The transfer functions of the filter is given by:

$$K_p = \frac{1 + s\tau_2}{s\tau_1}$$

Where:

 $\tau_1 = R3$, C2 and $\tau_2 = R4$, C2.

The characteristic equation is:

$$1 + K_p.K_f.K_o.K_n$$

This results in:

$$1 + K_p \left(\frac{1 + s\tau_2}{s\tau_1}\right) \frac{K_v}{s} K_n = 0$$

or s² + s K_p K_v K_n
$$\frac{\tau_2}{\tau_1}$$
 + K_pK_vK_n/ τ_1 = 0

This can be written as

$$s^2 + 2\zeta \omega_n s + \omega_n^2 = 0$$

with the natural frequency $\omega_{\rm n}$ defined as $\omega_{\rm n} = \sqrt{\frac{K_{\it p} K_{\it v} K_{\it n}}{\tau_{\it n}}}$

and the damping value given as $\zeta = 0.5.\tau_2.\omega_n$

In Fig.33 the output frequency response to a step of input frequency is shown. The overshoot and settling time percentages are now used to determine ω_n . From Fig.33 it can be seen that the damping ratio $\zeta=0.707$ will produce an overshoot

of less than 20% and settle to within 5% at $\omega_n t = 5$. The required settling time is 1 ms. This results in:

$$\omega_{\rm n} = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3 \, r/s.$$

Rewriting the equation for natural frequency results in:

$$\tau_1 = \frac{K_p \times K_v \times K_n}{\omega_n^2}$$

The maximum overshoot occurs at $N_{max} = 30$; hence $K_n = 1/30$:

$$\tau_1 = \frac{0.4 \times 2.24 \times 10^6}{5000^2 \times 30} = 0.0012$$

When C2 = 470 nF, it follows

$$R_3' = \frac{\tau_1}{C_2} = \frac{0.0012}{470 \ 10^{-9}} = 2550 \ \Omega$$

Hence the current source bias resistance $R_b = 17 \times 2550 = 43 \text{ k}\Omega$

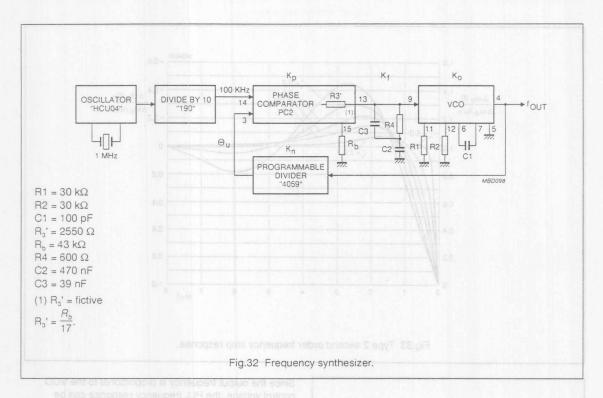
With
$$\zeta = 0.707$$
 (= 0.5 $\tau_2 \omega_n$) it follows
$$\tau_2 = \frac{0.707}{0.5 \times 5000} = 0.00028$$

$$R_4 = \frac{\tau_2}{C_2} = \frac{0.00028}{470.10^{-9}} = 600 \ \Omega$$

For extra ripple suppression a capacitor C3 can be connected in parallel with R4, with an extra $\tau_3 = R_4C_3$. For stability reasons τ_3 should be $< 0.1 \ \tau_2$,

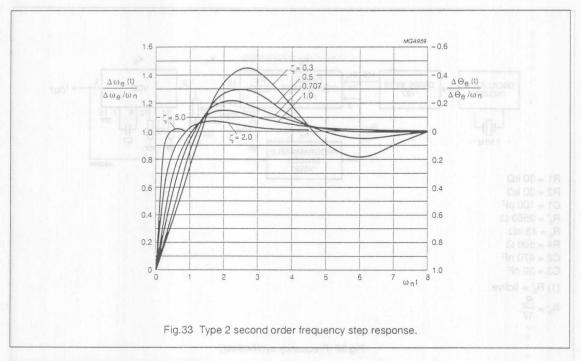
hence $C_3 < 0.1 C_2$, or $C_3 = 39 \text{ nF}$.





Note: to 9 nig panotisom vd agospolisso na diw beviesdo

For an extensive description and application example please refer to application note ordering number 9398 649 90011. Also available a computer design program for PLL's ordering number 9398 961 10061.



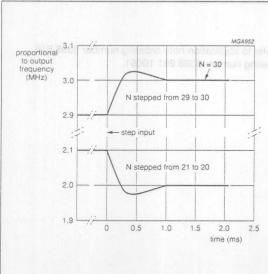


Fig.34 Frequency compared to the time response.

Since the output frequency is proportional to the VCO control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 9 of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin 9 with a simple RC filter, whose time constant is long compared with the phase detector sampling rate but short compared with the PLL response time.

SUPERSEDES DATA OF MARCH 1988 NINE WIDE SCHMITT TRIGGER BUFFER; OPEN DRAIN OUTPUTS; INVERTING

FEATURES

- Schmitt trigger action on all data inputs
- Output capability: standard (open drain)
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT9114 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT9114 are nine wide Schmitt trigger inverting buffer with open drain outputs and Schmitt trigger inputs.

The Schmitt trigger action in the data inputs transform slowly changing input signals into sharply defined jitter-free output signals.

The 74HC/HCT9114 have open-drain N-transistor outputs, which are not clamped by a diode connected to V_{CC}. In the OFF-state, i.e. when one input is LOW, the output may be pulled to any voltage between GND and V_{Omax}. This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

The "9114" is identical to the "9115" but has inverting outputs.

0)/14001	DARAMETER	CONDITIONS	TYF	PICAL	115117
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
tPHL/ tPLZ	propagation delay A_n to \overline{Y}_n	C _L = 15 pF V _{CC} = 5 V	12	13	ns
Cl	input capacitance	at r¥	3.5	3.5	pF
C _{PD}	power dissipation capacitance per buffer	notes 1 and 2	5	5	pF

GND = 0 V;
$$T_{amb} = 25 \,^{\circ}\text{C}$$
; $t_r = t_f = 6 \, \text{ns}$

Notes

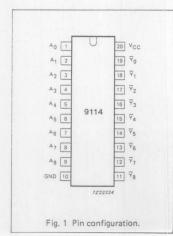
- 1. CPD is used to determine the dynamic power dissipation (PD in μ W): PD = CPD x VCC² x f₁ + Σ (CL x VCC² x f₀) where:
 - f; = input frequency in MHz
 - CL = output load capacitance in pF VCC = supply voltage in V
- f_0 = output frequency in MHz $\Sigma (C_L \times V_{CC}^2 \times f_0)$ = sum of outputs
- 2. For HC the condition is V_I = GND to V_{CC}
- For HCT the condition is $V_1 = GND$ to $V_{CC} 1.5 V$

PACKAGE OUTLINES

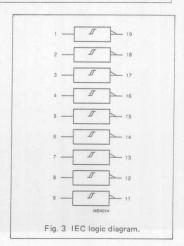
20-lead DIL; plastic (SOT146). 20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION						
1, 2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₈	data inputs lavel epsitor HOTH to lavel epsitor WOJ						
10	GND	ground (0 V) state 330 anneedance OFF-state						
19, 18, 17, 16, 15, 14, 13, 12 11	₹ ₀ to ₹ ₈	data outputs						
20	Vcc	positive supply voltage						







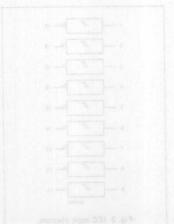
VO 19 MOO

7222336 Fig. 4 Functional diagram.

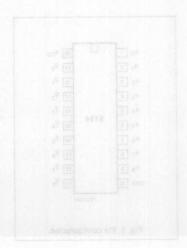
GND MBA021 Fig. 5 Logic diagram (one Schmitt trigger).

FUNCTION TABLE

INPUTS	OUTPUTS	S	Cal Toa :	
An	\overline{Y}_n			
L H	Z NOITCL/IUS		MAM	
H = HIGH voltage L = LOW voltage I		stride	data in	
Z = high impedance OFF-state				







DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard I_{CC} category: MSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are refered to GND (ground = 0 V)

					T _{amb} (°C)				TEST CONDITIONS		
SYMBOL PARAMETER	DADAMETER	74HC									1310111300	
	PARAMETER	+25		-40 to +85 -40 to		-40 to +125		VCC	WAVEFORMS			
		min.	typ.	max.	min.	max.	min.	max.	903.20			
V _{T+}	positive-going threshold	0.70 1.75 2.30	1.13 2.37 3.11	1.50 3.15 4.20	0.70 1.75 2.30		0.70 1.75 2.30	1.50 3.15 4.20	(V) = 6	2.0 4.5 6.0	Fig. 6	
V _T -	negative-going threshold			1.10 2.40 3.30	1.35	1.10 2.40 3.30	0.30 1.35 1.80	1.10 2.40 3.30	V	2.0 4.5 6.0	Fig. 6	
VН	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.4 0.5	0.43 0.57 0.68	0.80 1.00 1.10	0.18 0.40 0.50	1.00	0.15 0.40 0.50	0.80 1.00 1.10	V	2.0 4.5 6.0	Fig. 6	

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_1 = 50 pF$

		T _{amb} (°C) 8.0 4.0 5.0							1-1-1	TEST CONDITIONS		
SYMBOL PARAMI	DADAMETED	74HC								V	W.A.V.EEG.B.A.G	
	PARAMETER			+25		-40 to +85		-40 to +125		VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			VD = 0 V; t ₁ = t ₄ = 6 ns; C	
t _{PHL} /	propagation delay A_n to \overline{Y}_n		36 13 10	110 22 19	tan) ,	140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 7	
^t THL	output transition time	35	19 7 6	75 15 13	* 61 fi	95 19 16	85 sm - 6	110 22 19	ns	2.0 4.5 6.0	Fig. 7	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Transfer characteristics are given below.

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
An	0.3 3 VAW 5

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are refered to GND (ground = 0 V)

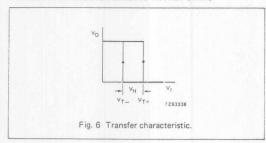
	7 2.0		1 0		T _{amb} (°C)		TEST CONDITIONS			
	4.5 Fig 6	V 04			74HC	CT O	Die Die	dends the	mion-ivitagen - LTV		
SYMBOL	PARAMETER	+25		-40 to +85 -		-40 to +125		UNIT	VCC	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			eV) alumetayri (V-
V _{T+}	positive-going threshold	0.9	1.50 1.70	2.0 2.1	0.9 1.2	2.0 2.1	0.9	2.0	V	4.5 5.5	Fig. 6
V _T _	negative-going threshold	0.7	1.06 1.27	1.4 1.7	0.7 0.8	1.4 1.7	0.7 0.8	1.4 2.7	V	4.5 5.5	Fig. 6
VH swo	hysteresis (V _{T+} – V _T _)	0.2	0.44 0.44		0.2	0.8 0.8	0.2	0.8	٧	4.5 5.5	Fig. 6

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	2.0	15 - 81			T _{amb} (°C)		TEST CONDITIONS				
SYMBOL	PARAMETER 0.8			74HC	т	er or				T THE SHAPE OF THE		
		011+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		11317 DEN	Issuen Indies TH.	
t _{PHL} /	propagation delay A_n to \overline{Y}_n		17	31		39		47	ns	4.5	Fig. 7	
^t THL	output transition time		7	15		19		22	ns	4.5	Fig. 7	

TRANSFER CHARACTERISTIC WAVEFORMS



AC WAVEFORMS

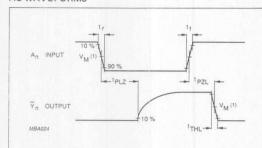


Fig. 7 Waveforms showing the input (An) to output (\overline{Y}_n) propagation delays and the output transition times.

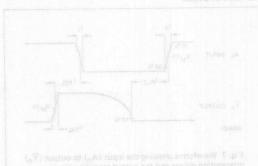
Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

TRANSFER CHARACTERISTIC WAVEFORMS



AC WAVEFORINS



Mote to AC waveforms
(1) HC: V_M = 50%; V₁ = 5ND to V_{CC}
HCT: V_M = 1.3 V; V₁ = 6ND to 3 V

SUPERSEDES DATA OF MARCH 1988 NINE WIDE SCHMITT TRIGGER BUFFER; OPEN DRAIN OUTPUTS

FEATURES

- Schmitt trigger action on all data inputs
- Output capability: standard (open drain)
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT9115 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT9115 are nine wide Schmitt trigger buffer with open drain outputs and Schmitt trigger inputs.

The Schmitt trigger action in the data inputs transform slowly changing input signals into sharply defined jitter-free output signals.

The 74HC/HCT9115 have open-drain N-transistor outputs, which are not clamped by a diode connected to V_{CC}. In the OFF-state, i.e. when one input is HIGH, the output may be pulled to any voltage between GND and V_{Omax}. This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

The ''9115'' is identical to the ''9114'' but has non-inverting outputs.

CVMDOL	PARAMETER	CONDITIONS	TYF	UNIT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	ONT
t _{PHL} / t _{PLZ}	propagation delay A _n to Y _n	C _L = 15 pF V _{CC} = 5 V	12	13	ns
CI	input capacitance	an ar .	3.5	3.5	pF
C _{PD}	power dissipation capacitance per buffer	notes 1 and 2	5	5	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Note

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

 f_i = input frequency in MHz f_0 = output frequency in MHz $\Sigma (C_L \times V_{CC}^2 \times f_0)$ = sum of outputs CL = output load capacitance in pF VCC = supply voltage in V

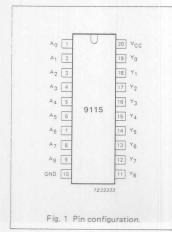
2. For HC the condition is VI = GND to VCC For HCT the condition is VI = GND to VCC - 1.5 V

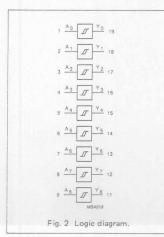
PACKAGE OUTLINES

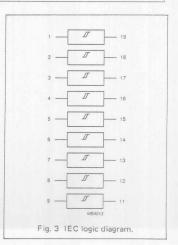
20-lead DIL; plastic (SOT146). 20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

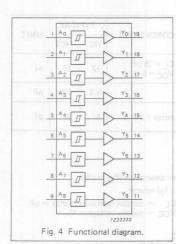
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₈	data inputs lavel egation HEIH = I
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12, 11	Y ₀ to Y ₈	data outputs
20	Vcc	positive supply voltage







SUPERSEDES DATA OF MARCH 1988 NINE WIDE SCHMITT TRIGGER BUFFER: OPEN DRAIN OUTPUTS



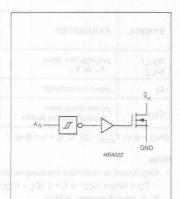


Fig. 5 Logic diagram (one Schmitt trigger).

FUNCTION TABLE

INPUTS	OUTPUTS
An	Yn
L	L
Н	MO Z

H	=	HIGH	voltage	level

L = LOW voltage level Z = high impedance OFF-state

STREET

- Schmitt trigger action on all data
- Ourput capability: standard (open
 - Ice category: MS1

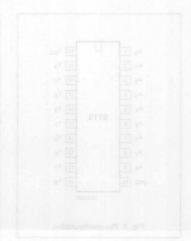
SENERAL DESCRIPTION

in the remarks set its are night-peace heats CMOS devices and are nin constitute with low power Schoricky. The TLETTLI, They are practified in ompliance with JEDEC transport no. 7 The 74HC/HCT81 IS are nine wide.

country trager across reproper areas in participated across in the data pacts transform slowly changing input ionals into sharply defined inter-freq

The TAHOURCTS! 15 have open-oratin Numerisator outputs, which are not clamped by a dipde connected to Voc. In the OFF state, i.e. when one input is worked the output may be patilled to any life. The output may be patilled to any state between OND and Vomar. This allows the device to be used as a LOW to HIGH on HIGH to-LOW sevel LOW to HIGH operation and OR nied output applications, these devices must

The "9)15" is identical to the "9114"



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Transfer characteristics are given below.

Output capability: standard ICC category: MSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are refered to GND (ground = 0 V)

					T _{amb} (°C)				TEST CONDITIONS		
SYMBOL	PARAMETER				74H0		UNIT	Vcc				
	FARAMETER	+25			-40 to +85		-40 to +125		Oldi	V	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		TEIRE	KANSFER CHARACT	
V _{T+}	positive-going threshold			1.50 3.15 4.20	1.75	1.50 3.15 4.20	0.70 1.75 2.30	1.50 3.15 4.20	V 0 = 6	2.0 4.5 6.0	Fig. 6	
V _T _	negative-going threshold	1.35	0.70 1.80 2.43			1.10 2.40 3.30	0.30 1.35 1.80	1.10 2.40 3.30	V	2.0 4.5 6.0	Fig. 6	
VH	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.4 0.5		0.80 1.00 1.10		0.80 1.00 1.10	0.15 0.40 0.50	0.80 1.00 1.10	V	2.0 4.5 6.0	Fig. 6	

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	e pla aa	7	8.0 EU T _{amb} (°C) 8.0 44.0 S.							TEST CONDITIONS		
SYMBOL	PARAMETER		74HC								WANTEODAG	
	PARAMETER	+25		-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.		08 = 1	$0: x_1 = y_2 = 0$	
tPHL/	propagation delay A _n to Y _n		36 13 10	115 22 19	ירט) דמר	140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 7	
^t THL	output transition time	85	19 7 6	75 15 13	e 07 0	95 19 16	25 660 . q	110 22 19	ns	2.0 4.5 6.0	Fig. 7	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Transfer characteristics are given below.

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	COEFFICIENT
An	0.3 AM

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are refered to GND (ground = 0 V)

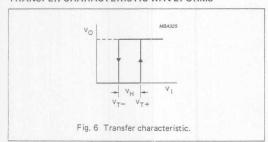
-		US.		-	T _{amb} (°C)		E VE		TEST CONDITIONS		
	2.0 4.5 Eig. 6	40.			74HC	T		35 1.8	bi bi	กก่อเกาก	enion-avizenan	
SYMBOL	PARAMETER 03	ue.	+25	1 10	-40	to +85	-40 t	o +125	UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		TV	N hysteresis (V-r	
V _{T+}	positive-going threshold	0.9	1.50 1.70		0.9	2.0 2.1	0.9	2.0 2.1	V	4.5 5.5	Fig. 6	
V _T	negative-going threshold	0.7	1.06 1.27		0.7 0.8	1.4 1.7	0.7	1.4 2.7	V SHA	4.5 5.5	Fig. 6	
VH SMO	hysteresis ($V_{T+} - V_{T-}$)	0.2	0.44		0.2	0.8	0.2	0.8	٧	4.5 5.5	Fig. 6	

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

	PARAMETER 0.5.	at at			T _{amb} (°C)		TEST CONDITIONS				
SYMBOL		74HCT								Vac	WAVEFORMS	
		01	011+25		-40 to +85		-40 to +125		UNIT	V _{CC}		
		min.	typ.	max.	min.	max.	min.	max.		BITHE CIC	tienest regree	
t _{PHL} / t _{PLZ}	propagation delay A _n to Y _n		18	31		39		47	ns	4.5	Fig. 7	
^t THL	output transition time		7	15		19		22	ns	4.5	Fig. 7	

TRANSFER CHARACTERISTIC WAVEFORMS



AC WAVEFORMS

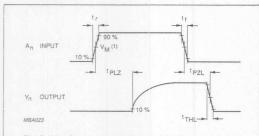
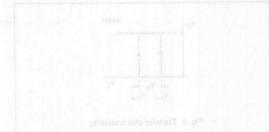


Fig. 7 Waveforms showing the input (A $_{\rm n}$) to output (Y $_{\rm n}$) propagation delays and the output transition times.

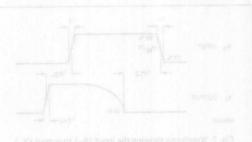
Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

TRANSFER CHARACTERISTIC WAVEFORMS



AC WAVEFORMS



? Waveforms showing the input (\mathbb{A}_n) to output (\mathbb{Y}_n) equation cones and the output transition times



Vote to AC wereforms 1) HC: V_M = SO's, V_L = GND to V_{GC} HCT: Vec = 1.3 V, V_L = GND to BV

8-BIT SYNCHRONOUS BCD DOWN COUNTER

GENERAL DESCRIPTION CARDINAS

- Cascadable
- Synchronous or asynchronous preset
- Output capability: standard
- · ICC category: MSI

GENERAL DESCRIPTION

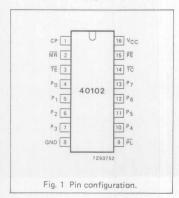
The 74HC/HCT40102 are high-speed Si-gate CMOS devices and are pin compatible with the "40102" of the "40008" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40102 consist each of an 8-bit synchronous down counter with a single output which is active when the internal count is zero. The "40102" is configured as two cascaded 4-bit BCD counters and has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count output (TC) are active-LOW logic.

In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input ($\overline{\text{TE}}$) is HIGH. The terminal count output ($\overline{\text{TC}}$) goes LOW when the count reaches zero if $\overline{\text{TE}}$ is LOW, and remains LOW for one full clock period.

When the synchronous preset enable input ($P\Xi$) is LOW, data at the jam input (P_0 to P_7) is clocked into the counter on the next positive-going clock transition regardless of the state of $\overline{T\Xi}$. When the asynchronous preset enable input ($P\Xi$) is LOW, data at the jam input ($P\Omega$ to P_7) is asynchronously forced into the counter regardless of the state of $\overline{P\Xi}$, $\overline{T\Xi}$, or CP. The jam inputs (P_0 to P_7) represent two 4-bit BCD words.

(continued on next page)



		CONDITIONS	TYP	UNIT	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
t _{PHL} /	propagation delay CP to TC	C _L = 15 pF - V _{CC} = 5 V	30	31	ns
fmax	maximum clock frequency	- vCC = 2 v	30	30	MHz
CI	input capacitance		3.5	3.5	pF
C _{PD} power dissipation capacitance per package		notes 1 and 2	20	25	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

$$PD = CPD \times VCC^2 \times f_1 + \Sigma (CL \times VCC^2 \times f_0)$$
 where:

f; = input frequency in MHz fo = output frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

 Σ (C_L x V_{CC}² x f₀) = sum of outputs 2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} - 1.5 V

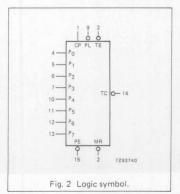
PACKAGE OUTLINES

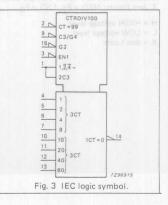
16-lead DIL; plastic (SOT38Z).

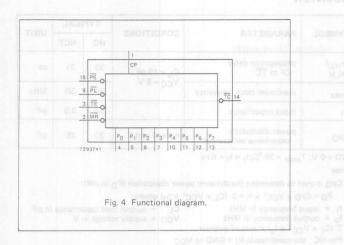
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1 2 3	CP MR TE	clock input (LOW-to-HIGH, edge-triggered) asynchronous master reset input (active LOW) terminal enable input
4, 5, 6, 7, 10, 11, 12, 13	P ₀ to P ₇	jam inputs
8 (4840000115) 9	GND PL TC	ground (0 V) asynchronous preset enable input (active LOW) terminal count output (active LOW)
15 16	PE VCC	synchronous preset enable input (active LOW) positive supply voltage







FUNCTION TABLE

C	CONTRO	L INPUTS		PRESET	N DESCRIPTION			
MR	PL	PEON	JUTE 1	MODE	ACTION JOSHYZ			
	Н	Нэн н	Hour	quori spole	inhibit counter			
Н	H TO	Н	L	synchronous	count down			
Н	Н	L	×	eruqni mei	preset on next LOW-to HIGH clock transition			
Н	L	×	X	V (0) bauong	preset asynchronously			
L	X	×	×	asynchronous	clear to maximum count			

Notes to function table

- 1. Clock connected to CP.
- 2. Synchronous operation: changes occur on the LOW-to-HIGH CP transition.
- 3. Jam inputs: $MSD = P_7$, $LSD = P_0$.
- H = HIGH voltage level
- L = LOW voltage level
- X = don't care

GENERAL DESCRIPTION

When the master reset input (MR) is LOW, the counter is asynchronously cleared to its maximum count (decimal 99) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the function table.

If all control inputs except \overline{TE} are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 clock pulses long.

The "40102" may be cascaded using the TE input and the TC output, in either a synchronous or ripple mode.

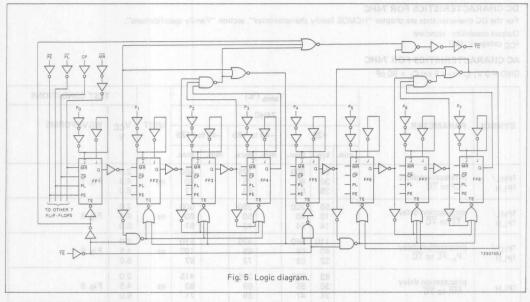
APPLICATIONS

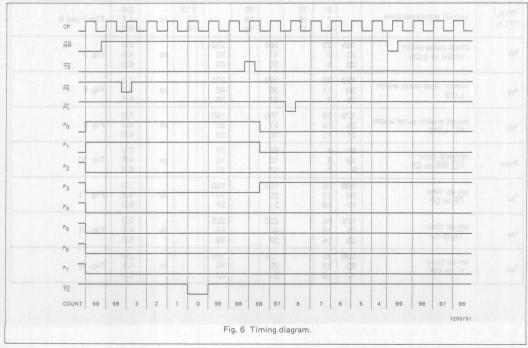
- Divide-by-n counters
- Programmable timers
- Interrupt timers
- Cycle/program counters

- unting is inhibited when the terminal bis input (TE) is HIGH. The terminal or nurger (TE) goes LOW when the
- count reaches sero if TE is COW, and remains COW for one full clock period.
- when the synchronous preset enable input

 (PE) is LOW, data at the jam input (Pp to

 PH) is clocked into the counter on the
- next positive-going clock transition
 regardless of the state of TE.
 When the expectation orders enable
- input (PT) is COW, date at the jam input (Pg to Py) is acynchronously forced into
- TR. or CP. The Jam inputs (Rg to Py)
- (continued on next page)





DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter ''HCMOS family characteristics'', section ''Family specifications''.

Output capability: standard

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

SYMBOL	ź.p.ż	T _{amb} (°C)								TEST CONDITIONS	
		-	m		74HC				UNIT	V _{CC}	WAVEFORMS
	PARAMETER	+25			-40	to +85	-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/	propagation delay CP to TC		96 35 28	300 60 51	Per	375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 7
tPHL/	propagation delay TE to TC		50 18 14	200 40 34	6	250 50 43	7	300 60 51	ns	2.0 4.5 6.0	Fig. 8
^t PHL/ ^t PLH	propagation delay P _n , PL to TC		110 40 32	240 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig. 9
^t PLH	propagation delay MR to TC		83 30 24	275 55 47	li pigo.	345 69 59		415 83 71	ns	2.0 4.5 6.0	Fig. 9
tTHL/ tTLH	output transition time	h	9 7 6	75 15 13		95 19 16	Ln	110 22 19	ns	2.0 4.5 6.0	Figs 7 and 8
tW	clock pulse width HIGH or LOW	165 33 28	22 8 6		205 41 35	H	250 50 43		ns	2.0 4.5 6.0	Fig. 7
tw	master reset pulse width LOW	150 30 26	30 11 9		190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig. 9
tw	preset enable pulse width PL; LOW	125 25 21	39 14 11		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 9
^t rem	removal time PL; MR to CP	50 10 9	8 3 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t _{su}	set-up time PE to CP	100 20 17	36 13 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t _{su}	set-up time TE to CP	175 35 30	50 18 14		220 44 37		265 53 45		ns	2.0 4.5 6.0	Fig. 11
t _{su}	set-up time P _n to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 12

AC CHARACTERISTICS FOR 74HC (Cont'd)

 $GND = 0 V; t_r = t_f = 6 ns; C_1 = 50 pF$

	T _{amb} (°C)								TEST CONDITIONS		
SYMBOL	DADAMETED	74HC								.,	WAVEFORMS
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		-18	
th	hold time PE to CP	2 2 2	-8 -3 -2		2 2 2		2 2 2	38	ns	2.0 4.5 6.0	Fig. 11
th	hold time TE to CP	0 0	-41 -15 -12		0 0 0		0 0 0	65	ns	2.0 4.5 6.0	Fig. 11
th	hold time P _n to CP	2 2 2	-5 -5 -5		2 2 2		2 2 2	8	ns 🔑	2.0 4.5 6.0	Fig. 12
fmax	maximum clock pulse frequency	3 15 18	8.9 27 32		2 12 14		2 10 12	7	MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT					
CP, PE	1.50					
MR	1.00					
TE	0.80					
Pn	0.25					
PL	0.35					

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	TEST CONDIT				T _{amb} (°C)					TEST CONDITIONS
SYMBOL	Margaryaw Loov Tridu	74НСТ									WAVEFORMS
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	VCC	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
tPHL/ tPLH	propagation delay P _n ; CP to TC		38	63		79		95	ns	4.5	Figs 7 and 9
t _{PHL} /	propagation delay TE to TC		25	50		63	1:	75	ns	4.5	Fig. 8
tPHL/	propagation delay PL to TC		49	83		104	2	125	ns	4.5	Fig. 9
^t PLH	propagation delay MR to TC		31	55		69		83	ns	4.5	Fig. 9
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 7 and 8
tW	clock pulse width HIGH or LOW	33	11	2.1	41		50	0	ns	4.5	Fig. 7
tw	master reset pulse width LOW	30	16	" nc/ra	38	enstee	45	mel 20	ns	4.5	Fig. 9 stocked 500 entry
tW	preset enable pulse width PL; LOW	43	25		54		65		ns	4.5	Fig. 9 12M VIOLETED
t _{rem}	removal time PL; MR to CP	10	1	vie at C	13	tions	15	IA) tris	ns	4.5	Fig. 10 Sept T3H at an
t _{su}	set-up time PE to CP	20	10	orts me	25	080 1	30	yd sule	ns elle	4.5	Fig. 11
t _{su}	set-up time TE to CP	40	20		50		60		ns	4.5	Fig. 11
t _{su}	set-up time P _n to CP	20	12		25		30		ns	4.5	Fig. 12
^t h	hold time PE to CP	0	-4		0		0		ns	4.5	Fig. 11
th	hold time TE to CP	0	-15		0		0		ns	4.5	Fig. 11
th	hold time P _n to CP	0	-6		0		0		ns	4.5	Fig. 12
fmax	maximum clock pulse frequency	15	27		12		10		MHz	4.5	Fig. 7

AC WAVEFORMS

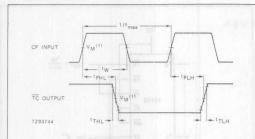
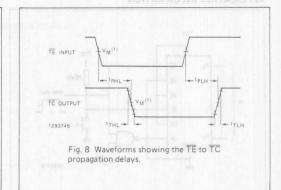


Fig. 7 Waveforms showing the clock input (CP) to \overline{TC} propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.



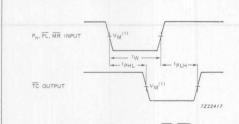
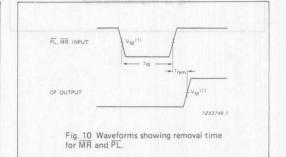
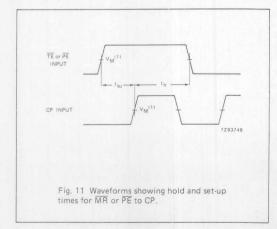


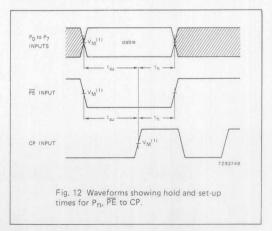
Fig. 9 Waveforms showing \overline{PL} , \overline{MR} , P_n to \overline{TC} propagation delays.







(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.



Note to Fig. 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION INFORMATION

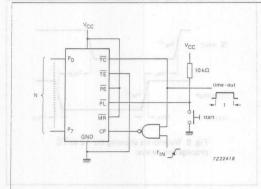


Fig. 13 Programmable timer.

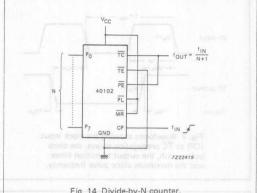
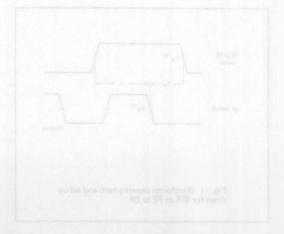


Fig. 14 Divide-by-N counter.





8-BIT SYNCHRONOUS BINARY DOWN COUNTER

FEATURES MANAGED JAMES 1

- Cascadable
- Synchronous or asynchronous preset
- Output capability: standard
- · ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT40103 are high-speed Si-gate CMOS devices and are pin compatible with the "40103" of the "40008" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40103 consist each of an 8-bit synchronous down counter with a single output which is active when the internal count is zero. The "40103" contains a single 8-bit binary counter and has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count output (TC) are active-LOW logic.

In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input (TE) is HIGH. The terminal count output (TC) goes LOW when the count reaches zero if TE is LOW, and remains LOW for one full clock period.

When the synchronous preset enable input (\overline{PE}) is LOW, data at the jam input $(P_0$ to $P_7)$ is clocked into the counter on the next positive-going clock transition regardless of the state of \overline{TE} . When the asynchronous preset enable input $(P_{\overline{L}})$ is LOW, data at the jam input $(P_0$ to $P_7)$ is asynchronously forced into the counter regardless of the state of \overline{PE} , \overline{TE} , or CP. The jam inputs $(P_0$ to $P_7)$ represent a single 8-bit binary word. (continued on next page)

CP 1	U	16 Vcc
MR 2		15 PE
TE 3		14 TC
P ₀ 4	40400	13 P ₇
P ₁ 5	40103	12 P ₆
P ₂ 6		11 P ₅
P3 7		10 P ₄
GND 8		9 PL
	7 7 9 3 7 3	39

SYMBOL	PARAMETER	CONDITIONS	TYI	LIMIT	
STWIBUL	PARAMETER	CONDITIONS	НС	нст	ns MHz pF
^t PHL/ ^t PLH	propagation delay CP to TC	C _L = 15 pF - V _{CC} = 5 V	30	30	ns
f _{max}	maximum clock frequency	_ vCC = 2 v	32	31	MHz
CI	input capacitance	0.00	3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	24	27	pF

$$GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$$

Notes

1. CPD is used to determine the dynamic power dissipation (PD in μ W):

PD = CPD
$$\times$$
 VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:

fi = input frequency in MHz

CL = output load capacitance in pF VCC = supply voltage in V

 f_0 = output frequency in MHz $\Sigma (C_L \times V_{CC}^2 \times f_0)$ = sum of outputs

2. For HC the condition is VI = GND to VCC
For HCT the condition is VI = GND to VCC - 1.5 V

Output

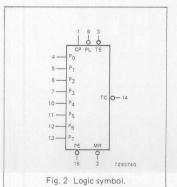
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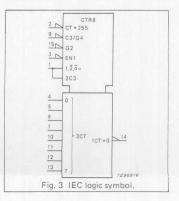
PACKAGE OUTLINES

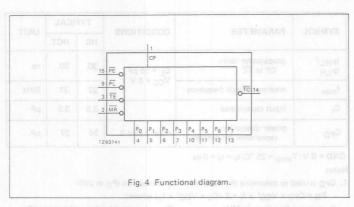
16-lead DIL; plastic (SOT38Z). 16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1 ylavanovils 2 3 raves muliik	CP MR TE	clock input (LOW-to-HIGH, edge-triggered) asynchronous master reset input (active LOW) terminal enable input
4, 5, 6, 7, 10, 11, 12, 13	Po to P7	jam inputs
9	GND PL	ground (0 V) asynchronous preset enable input (active LOW)
14	TC	terminal count output (active LOW) as BOILE
15	PE	synchronous preset enable input (active LOW)
16	Vcc	positive supply voltage







FUNCTION TABLE

-	CONTRO	LINPUTS	3	PRESET	ACTION
MR	PL	PE	TE	MODE	ACTION
Н	Н	Н	Н		inhibit counter
Н	Н	Н	L	synchronous	count down
Н	Н	L NOI	X	OMA BIMAIC	preset on next LOW-to HIGH clock transition
н (1)	neog <u>L</u> n-ng	X	o X	I mani seota	preset asynchronously
L	X	X	X	asynchronous	clear to maximum count

Notes to function table

- 1. Clock connected to CP.
- 2. Synchronous operation: changes occur on the LOW-to-HIGH CP transition.
- 3. Jam inputs: $MSD = P_7$, $LSD = P_0$.
- H = HIGH voltage level
- L = LOW voltage level
- X = don't care

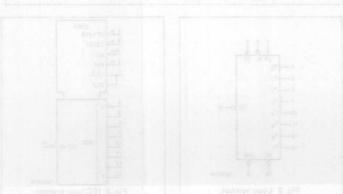
GENERAL DESCRIPTION (Cont'd)

When the master reset input (MR) is LOW, the counter is asynchronously cleared to its maximum count (decimal 255) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the function table.

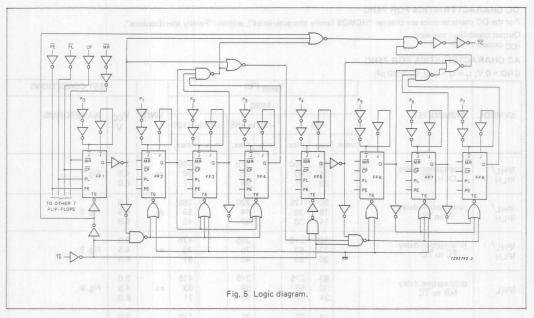
If all control inputs except \overline{TE} are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 256 clock pulses long.

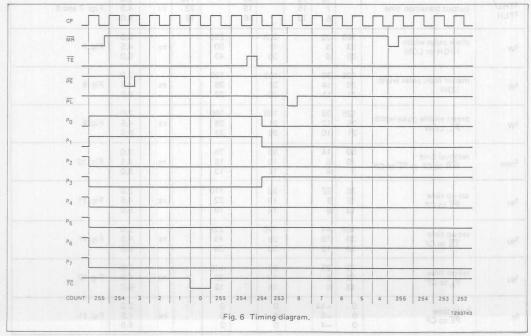
The "40103" may be cascaded using the TE input and the TC output, in either a synchronous or ripple mode.

- Divide-by-n counters
- Programmable timers
- Interrupt timers | see and beautiful |
- Cycle/program counters









DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

AC CHARACTERISTICS FOR 74HC GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

					T _{amb} (°C)					TEST CONDITIONS
SYMBOL	PARAMETER		rs.	5	74H	С		1, 1,	UNIT	V	WAVEFORMS
STIMBUL	PARAMETER		+25	N. C.	-40	to +85	-40 t	o +125	VIVI	V _{CC}	WAVEFORWIS
	JULIA III.	min.	typ.	max.	min.	max.	min.	max.		-	
tPHL/	propagation delay CP to TC	-	96 35 28	300 60 51	3.20	375 75 64	5 E93	450 90 77	ns	2.0 4.5 6.0	Fig. 7
tPHL/	propagation delay TE to TC	Y	50 18 14	175 35 30	6	220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
tPHL/ tPLH	propagation delay		102 37 30	315 63 53		395 79 40		475 95 81	ns	2.0 4.5 6.0	Fig. 9
^t PHL	propagation delay MR to TC		83 30 24	275 55 47	io sigo.	345 69 59		415 83 71	ns	2.0 4.5 6.0	Fig. 9
tTHL/ tTLH	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 7 and 8
tW	clock pulse width HIGH or LOW	165 33 28	22 8 6		205 41 35		250 50 43		ns	2.0 4.5 6.0	Fig. 7
tw	master reset pulse width LOW	125 25 21	39 14 11		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 9
tw	preset enable pulse width PL; LOW	125 25 21	33 12 10		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 9
[†] rem	removal time MR to CP or PL to CP	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t _{su}	set-up time PE to CP	75 15 13	22 8 6		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 11
^t su	set-up time TE to CP	150 30 26	44 16 13		190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig. 11
t _{su}	set-up time P _n to CP	75 15 13	22 8 6		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 12
t _h	hold time PE to CP	0 0 0	-14 -5 -4		0 0	T 0 .n	0 0 0		ns	2.0 4.5 6.0	Fig. 11

AC CHARACTERISTICS FOR 74HC (Cont'd)

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_1 = 50 \text{ pF}$

				Т	amb (°	C)					TEST CONDITIONS
					74H				LINIT	.,	WAVEFORMS
SYMBOL PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
	min.	typ.	max.	min.	max.	min.	max.		G/	ou Timu	
^t h	hold time TE to CP	0 0 0	-30 -11 -9		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11
^t h	hold time P _n to CP	0 0 0	-17 -6 -5		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 12
f _{max}	maximum clock pulse frequency	3.0 15 18	10 29 35		2.4 12 14	ene T	2.0 10 12		MHz	2.0 4.5 6.0	Fig. 7 p = 1 V 0 = 0

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard ICC category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

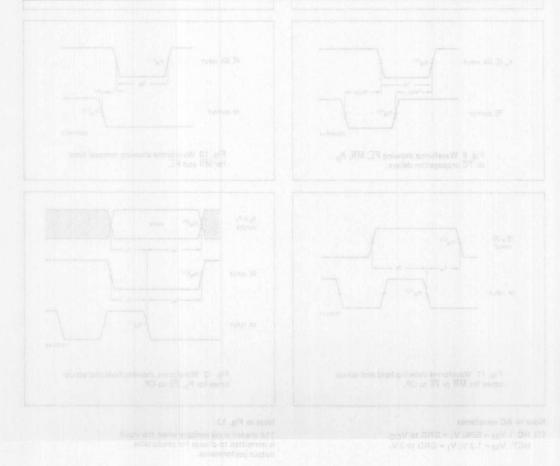
INPUT	UNIT LOAD COEFFICIENT
CP, PE	1.50 1.00
TE	0.80
Pn	0.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_1 = 50 \text{ pF}$

	0.8			21	r _{amb} (°C)		8 3		TEST CONDITIONS		
SYMBOL	PARAMETER				74HC	Т			UNIT	Vcc	WAVEFORMS	
STINDOL	PANAMETER		+25		-40	to +85	-40 t	o +125	ONT	V	WAVELOUMS	
		min.	typ.	max.	min.	max.	min.	max.				
tphl/ tplh	propagation delay CP to TC		35	60		75		90	ns	4.5	Fig. 7	
t _{PHL} /	propagation delay TE to TC		23	40		50		60	ns	4.5	Fig. 8	
t _{PHL} /	propagation delay PL to TC		44	75		94		112	ns	4.5	Fig. 9	
^t PHL	propagation delay MR to TC		29	55		69		83	ns	4.5	Fig. 9	
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Figs. 7 and 8	
tW	clock pulse width HIGH or LOW	33	10		41		50		ns	4.5	Fig. 7	
tW	master reset pulse width LOW	30	16		38		45		ns	4.5	Fig. 9	
tW	preset enable pulse width PL; LOW	38	22		48		57		ns	4.5	Fig. 9	
^t rem	removal time MR to CP or PL to CP	10	1		13		15		ns	4.5	Fig. 10	
t _{su}	set-up time PE to CP	20	11		25		30		ns	4.5	Fig. 11	
t _{su}	set-up time TE to CP	40	20		50		60		ns	4.5	Fig. 11	
t _{su}	set-up time P _n to CP	20	11		25		30		ns	4.5	Fig. 12	
^t h	hold time PE to CP	2	-3		2		2		ns	4.5	Fig. 11	

		17	11		Tamb (TEST CONDITIONS					
SYMBOL PARAME	DADAMETED	not.	74HCT								WAVEFORMS	
	PARAMETER	- 4	+25		-40 to +85		-40 to +125		UNIT	V _{CC}	WAVETONING	
	end'r	min.	typ.	max.	min.	max.	min.	max.				
th	hold time TE to CP	0	-10	51	0		0		ns	4.5	Fig. 11	
th	hold time Pn to CP	0 ten sW 8	-5		0		0		ns and part	4.5	Fig. 12	
fmax	maximum clock pulse frequency	15	28		12		10	ine clock on times equency	MHz	4.5	Fig. 7	



AC WAVEFORMS

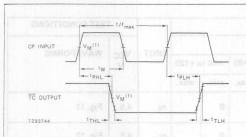


Fig. 7 Waveforms showing the clock input (CP) to TC propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

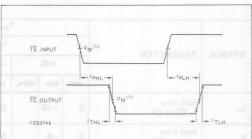
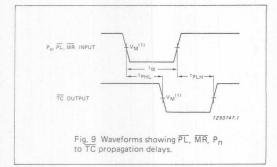
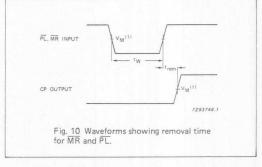
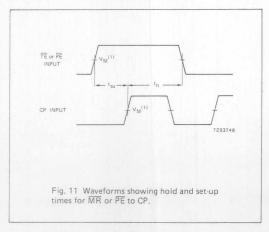
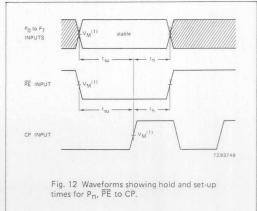


Fig. 8 Waveforms showing the $\overline{\text{TE}}$ to $\overline{\text{TC}}$ propagation delays.









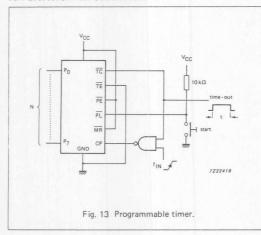
Note to AC waveforms

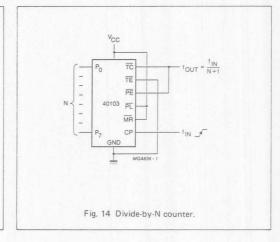
(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Fig. 12

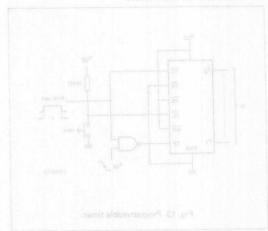
The shaded areas indicate when the input is permitted to change for predictable output performance.

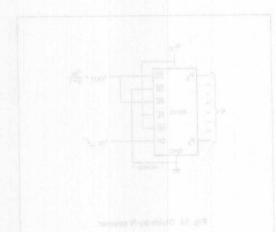
APPLICATION INFORMATION





APPLICATION INFORMATION





4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER; 3-STATE

FEATURES

- Synchronous parallel or serial operating
- 3-state outputs
- · Output capability: bus driver
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT40104 are high-speed Si-gate CMOS devices and are pin compatible with the "40104" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40104 are universal shift registers featuring parallel inputs, parallel outputs, shift-right and shift-left serial inputs and 3-state outputs allowing the devices to be used in bus-organized

In the parallel-load mode (S_0 and S_1 are HIGH), data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input (CP).

During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the shift-right (DSR) and shift-left (DSI) serial inputs, respectively.

Clearing the register is accomplished by setting both mode controls (So and S1) LOW and clocking the register. When the output enable input (OE) is LOW, all outputs assume the highimpedance OFF-state (Z).

APPLICATIONS

- Arithmetic unit bus registers
- Serial/parallel conversion
- General-purpose register for bus organized systems
- General-purpose registers

CVAMPOL	DAD AMETER	CONDITIONS	TYI	LINIT	
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
tPHL/ tPLH	propagation delay CP to Q _n	C _L = 15 pF	13	15	ns
fmax	maximum clock frequency	$V_{CC} = 5 V$	62	57	MHz
Cl	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	75	75	pF

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

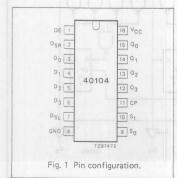
- 1. CPD is used to determine the dynamic power dissipation (P_D in μW):
 - PD = CPD \times VCC² \times f_i + Σ (CL \times VCC² \times f_o) where:
 - f; = input frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V
 - fo = output frequency in MHz $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
- 2. For HC the condition is VI = GND to VCC
- For HCT the condition is $V_I = GND$ to VCC 1.5 V

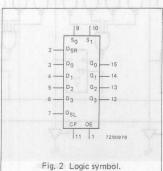
PACKAGE OUTLINES

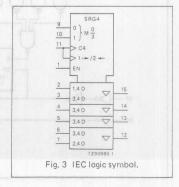
16-lead DIL; plastic (SOT38Z). 16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

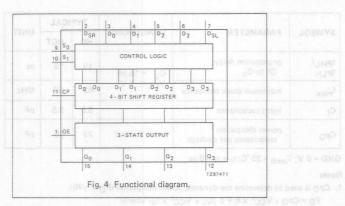
PINA	io. s	YMBOL	NAME AND FUNCTION
1	0	E	3-state output enable input (active HIGH)
2	D	SR	serial data shift-right input
3, 4, 5	5, 6 D	to D ₃	parallel data inputs
7/	D	SL V	serial data shift-left input
8	G	ND	ground (0 V)
9, 10	Sc), S ₁	mode control inputs
11	CF		clock input (LOW-to-HIGH, edge-triggered)
15, 14	I, 13, 12 Q	to Q ₃	3-state parallel outputs
16	V	cc	positive supply voltage







4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER: 3-STATE



SENTINES

- Shounninko a
- e 3-state outputs
- : Althoaded indinch a
 - M ton category: M

GENERAL DESCRIPTION The PAHC/HCT40104 are high spens

Si-gate CMOS devices and are pin

"40008" saries. They are specified in

ampliance with JEDEC standard on 7A.

The /AHC/HCTA010A are universal hift registers featuring penallel inputs.

serial inputs and 3-state outputs allowing the devices to be used in bus-organized

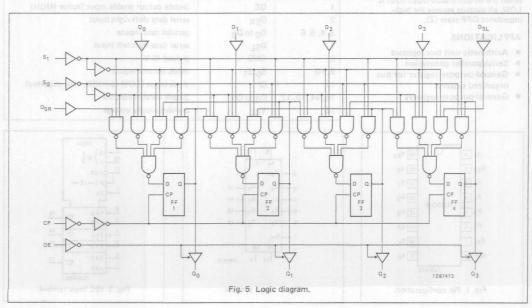
FUNCTION TABLE

H = HIGH voltage level L = LOW voltage level X = don't care

 $t_{n+1} = \text{state after next}$

LOW-to-HIGH transition of CP

OPERATING MODES	medul pert n	IN	PUTS (C	E = HIC	GH)	OUTPUTS at t _{n+1}				
OPERATING MODES	S ₁	s ₀	DSR	DSL	D ₀ to D ₃	00	01	02	03	
reset GMD = Warmoni	e cgm	E Lor	X	X	×	L	L	L	(Cg)	
shift left	ILIT U	LEO LEO	×	L	an XI-Tin	Q ₁ Q ₁	Q ₂ Q ₂	Q3	Н	
shift right	L	Н	L	×	X	L	Q ₀	Q ₁ Q ₁	Q ₂ Q ₂	
parallel load	S H	H	X	×	i (SQ Jrd S) i ster, H	L H	L	L	L	



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver ICC category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \ V; t_r = t_f = 6 \ ns; C_L = 50 \ pF$

					T _{amb} (°C)				TEST CONDITIONS			
					74H								
SYMBOL	PARAMETER	+25			-40 t	o +85	-40 to +125		UNIT	V _{CC}	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.					
tPHL/	propagation delay CP to Q _n		44 16 13	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6	20820	
tPZH/	3-state output enable time OE to Ω_{n}		33 12 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	IV 0 = QM	
tPHZ/	3-state output disable time OE to Ω_{Π}	321-	50 18 14	150 30 26	TOHA	190 38 33	+25	225 45 38	ns	2.0 4.5 6.0	Fig. 7	TOSMAS	
tTHL/ tTLH	output transition time	жен	14 5 4	60 12 10	in stig	75 15 13	n ,dy	90 18 15	ns	2.0 4.5 6.0	Fig. 6	Numerical Control of the Control of	
tW	clock pulse width HIGH or LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6	H Tal	
t _{su}	set-up time D _n , D _{SR} , D _{SL} to CP	80 16 14	17 6 5		100 20 17		120 24 20	E	ns	2.0 4.5 6.0	Fig. 8	Z74) /ZH4;	
t _{SU}	set-up time S ₀ , S ₁ to CP	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	UHT!	
t _h	hold time Dn, DSR, DSL to CP	2 2 2	-8 -3 -2		2 2 2	9	2 2 2	ar	ns	2.0 4.5 6.0	Fig. 8	19 <u>2</u> 2	
th	hold time S ₀ , S ₁ to CP	2 2 2	-14 -5 -4		2 2 2	2	2 2 2 2	os	ns	2.0 4.5 6.0	Fig. 8	190	
fmax	maximum clock pulse frequency	6.0 30 35	19 56 67	2	4.8 24 28		4.0 20 24	2	MHz	2.0 4.5 6.0	Fig. 6	ris	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter, "HCMOS family characteristics", section "Family specifications", see chapter, "HCMOS family characteristics",

Output capability: bus driver I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications, To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
Do to Da	0.35
DSR, DSI	0.35
CP	0.35
S ₀ , S ₁	0.70
OE	1.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

	PARAMETER				Tamb (°C)	10 28			TEST CONDITIONS		
SYMBOL		225 45		08	74HC	т	90 16		UNIT		WAVEFORMS	TPH2
		+25			-40 to +85 -40 to			+125	UNIT	VCC	WAVEFORWS	
	2.0 ns 4.5 Fig. 6	min.	typ.	max.	min.	max.	min.	max.	90	na nabi	enant tugtup	JARTI
tphL/	propagation delay CP to Ω _n		18	34		43	11	51	ns	4.5	Fig. 6	PLA P
tPZH/ tPZL	3-state output enable time OE to Q _n		12	30		38		45	ns	4.5	Fig. 7	W
t _{PHZ} / t _{PLZ}	3-state output disable time OE to Q_n		21	35		44		53	ns	4.5	Fig. 7	1323
^t THL/ ^t TLH	output transition time		5	12	38	15	51	1808	ns	4.5	Fig. 6	ua ^l
tW	clock pulse width HIGH or LOW	16	7	2	20	S	24	2	ns	4.5	Fig. 6	
t _{su}	set-up time D _n , D _{SR} , D _{SL} to CP	16	8	04 04	20	2	24	2	ns 93	4.5	Fig. 8	N ₂
t _{su}	set-up time S ₀ , S ₁ to CP	20	9	\$ 2	25	2 2	30	5 5	ns	4.5	Fig. 8	r)
th	hold time Dn, DSR, DSL to CP	2	-2	4.2	2		2 9	0.8	ns	4.5	Fig. 8	fmax
th	hold time S ₀ , S ₁ to CP	2	-5	(2)	2	2	2	0.00	ns	4.5	Fig. 8	
f _{max}	maximum clock pulse frequency	27	52		22		18		MHz	4.5	Fig. 6	

AC WAVEFORMS

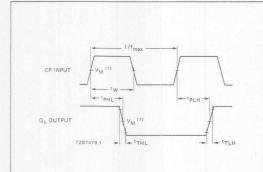


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

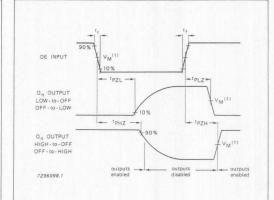


Fig. 7 Waveforms showing the 3-state enable and disable times.

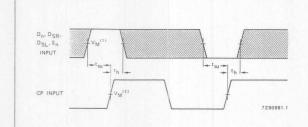


Fig. 8 Waveforms showing the set-up and hold times from the D_n, D_{SR}, D_{SL} and S_n inputs to the clock (CP).

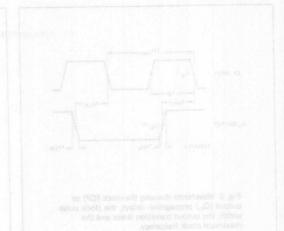
Note to Fig 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} . HCT: $V_M = 1.3 \text{ V}$; $V_I = GND$ to 3 V.

AC WAVEFORM



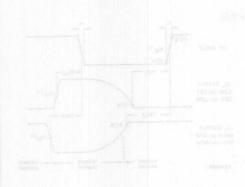


Fig. 7. Waveforms showing the 3-state enable and disable times.

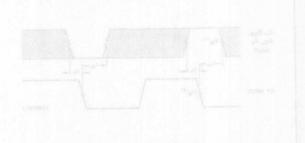


Fig. 8 Wavetorms showing the ser-up and hold hims from the D_{RA} DSR, DSL and S_A inputs to the block (CP).

Note to Fla 8

The shaded areas indicate when the input is carmitted to change for predictable output senterniance.

Note to AC waveforms

(1) MC : V_M = 50%; V_I = 6ND to V_{CC}

HCT: V_M = 1.3 V; V_I = 6 ND to 3 V

4-BIT X 16-WORD FIFO REGISTER

FEATURES

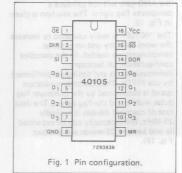
- Independent asynchronous inputs and outputs
- Expandable in either direction
- Reset capability
- Status indicators on inputs and outputs
- 3-state outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT40105 are high-speed Si-gate CMOS devices and are pin compatible with the "40105" of the "40008" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40105 are first-in/firstout (FIFO) "elastic" storage registers that can store sixteen 4-bit words. The "40105" is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems. Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "O" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripples through to the output end, the status of the first control flip-flop (data-in ready output - DIR) indicates if the FIFO is full, and the status of the last flip-flop (data-out ready output - DOR) indicates if the FIFO

(continued on next page)



SYMBOL	PARAMETER	CONDITIONS	TYP	UNIT	
SAMBOL	PARAMETER	sistentia m	НС	нс нст	
tPHL/dens	propagation delay MR to DIR, DOR SO to Qn	edt biswot s	16 37	15 35	ns ns
[†] PHL	propagation delay SI to DIR SO to DOR	VCC = 5 V	16 17	18	ns ns
f _{max}	maximum clock frequency	n be reduced from	33	31	MHz
CI T SILTER	input capacitance	g unused data	3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	134	145	rF.

GND = 0 V;
$$T_{amb} = 25 \,^{\circ}C$$
; $t_r = t_f = 6 \, \text{ns}$

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

PD = CPD x VCC² x f₁ + Σ (CL x VCC² x f₀) where:

fi = input frequency in MHz fo = output frequency in MHz CL = output load capacitance in pF VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

2. For HC the condition is V $_{I}$ = GND to VCC For HCT the condition is V $_{I}$ = GND to VCC $_{I}$ = 0.5 V

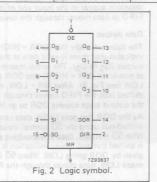
PACKAGE OUTLINES

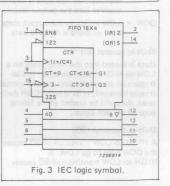
16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
les occurs. Then	ŌĒ	output enable input (active LOW)
2 14 14 (14)	DIR mesque n	data-in ready output
3 stab txen ent u	SI OF MAIN 29	shift-in input (LOW-to-HIGH, edge-triggered)
4, 5, 6, 7	D ₀ to D ₃	parallel data inputs
8	GND	ground (0 V) useds of which box viums
9	MR	asynchronous master reset input (active HIGH)
13, 12, 11, 10	Q ₀ to Q ₃	3-state data outputs
14	DOR	data-out ready output
15 and repuent	SO	shift-out input (HIGH-to-LOW, edge-triggered)
16	Vcc	positive supply voltage
	THE REPORT OF THE PARTY OF THE	A LANGE TO SELECT THE PROPERTY OF THE PROPERTY





GENERAL DESCRIPTION

contains data. As the earliest data is/Coremoved from the bottom of the data stack (output end), all data entered later will automatically ripple toward the output.

INPUTS AND OUTPUTS

Data inputs (Do to Da)

As there is no weighting of the inputs, any input can be assigned as the MSB. The size of the FIFO memory can be reduced from the 4 x 16 configuration, i.e. 3 x 16, down to 1 x 16, by tying unused data input pins to V_{CC} or GND.

Data outputs (Q₀ to Q₃)

As there is no weighting of the outputs, any output can be assigned as the MSB. The size of the FIFO memory can be reduced from the 4 x 16 configuration as described for data inputs. In a reduced format, the unused data output pins must be left open circuit.

Master-reset (MR)

When MR is HIGH, the control functions within the FIFO are cleared, and dat content is declared invalid. The data-in-ready (DIR) flag is set HIGH and the data-out-ready (DOR) flag is set LOW. The output stage remains in the state of the last word that was shifted out, or in the random state existing at power-up.

Status flag outputs (DIR, DOR)

Indication of the status of the FIFO is given by two status flags, data-in-ready (DIR) and data-out-ready (DOR):

- DIR = HIGH indicates the input stage is empty and ready to accept valid data;
- DIR = LOW indicates that the FIFO is full or that a previous shift-in operation is not complete (busy):
- DOR = HIGH assures valid data is present at the outputs Q₀ to Q₃ (does not indicate that new data is awaiting transfer into the output stage);
- DOR = LOW indicates the output stage is busy or there is no valid data.

Shift-in control (S1)

Data is loaded into the input stage on a LOW-to-HIGH transition of SI. It also triggers an automatic data transfer process (ripple through). If SI is held HIGH during reset, data will be loaded at the falling edge of the MR signal.

Shift-out control (SO)

A HIGH-to-LOW transition of \overline{SO} causes the DOR flags to go LOW. A HIGH-to-LOW transition of \overline{SO} causes

upstream data to move into the output stage, and empty locations to move towards the input stage (bubble-up).

Output enable (OE)

The outputs Ω_0 to Ω_3 are enabled when $\overline{OE} = LOW$. When $\overline{OE} = HIGH$ the outputs are in the high impedance OFF-state.

FUNCTIONAL DESCRIPTION

Data input

Following power-up, the master-reset (MR) input is pulsed HIGH to clear the FIFO memory (see Fig. 8). The data-in-ready flag (DIR = HIGH) indicates that the FIFO input stage is empty and ready to receive data. When DIR is valid (HIGH), data present at D0 to D3 can be shifted-in using the SI control input. With SI = HIGH, data is shifted into the input stage and a busy indication is given by DIR going LOW.

The data remains at the first location in the FIFO until DIR is set to HIGH and data moves through the FIFO to the output stage, or to the last empty location. If the FIFO is not full after the SI pulse, DIR again becomes valid (HIGH) to indicate that space is available in the FIFO. The DIR flag remains LOW if the FIFO is full (see Fig. 6). The SI pulse must be made LOW in order to complete the shift-in process.

With the FIFO full, SI can be held HIGH until a shift-out (SO) pulse occurs. Then, following a shift-out of data, an empty location appears at the FIFO input and DIR goes HIGH to allow the next data to be shifted-in. This remains at the first FIFO location until SI goes LOW (see Fig. 7).

Data transfer

After data has been transferred from the input stage of the FIFO following SI = LOW, data moves through the FIFO asynchronously and is stacked at the output end of the register. Empty locations appear at the input end of the FIFO as data moves through the device.

Data output

The data-out-ready flag (DOR = HIGH) indicates that there is valid data at the output (Ω_0 to Ω_3). The initial master-reset at power-on (MR = HIGH) sets DOR to LOW (see Fig. 8). After MR = LOW, data shifted into the FIFO moves through to the output stage causing DOR to go HIGH.

As the DOR flag goes HIGH, data can be shifted-out using the \overline{SO} control input. With \overline{SO} = HIGH, data in the output stage is shifted out and a busy indication is given by DOR going LOW. When \overline{SO} is made LOW, data moves through the FIFO

to fill the output stage and an empty location appears at the input stage. When the output stage is filled DOR goes HIGH, but if the last of the valid data has been shifted-out leaving the FIFO empty the DOR flag remains LOW (see Fig. 9). With the FIFO empty, the last word that was shifted-out is latched at the output Q_0 to Q_3 .

With the FIFO empty, the \overline{SO} input can be held HIGH until the SI control input is used. Following an SI pulse, data moves through the FIFO to the output stage, resulting in the DOR flag pulsing HIGH and as shift-out of data occurring. The \overline{SO} control must be made LOW before additional data can be shifted-out (see Fig. 10).

High-speed burst mode

If it is assumed that the shift-in/shift-out pulses are not applied until the respective status flags are valid, it follows that the shift-in/shift-out rates are determined by the status flags. However, without the status flags a high-speed burst mode can be implemented. In this mode, the burst-in/burst-out rates are determined by the pulse widths of the shift-in/shift-out inputs and burst rates of 35 MHz can be obtained. Shift pulses can be applied without regard to the status flags but shift-in pulses that would overflow the storage capacity of the FIFO are not allowed (see Figs 11 and 12).

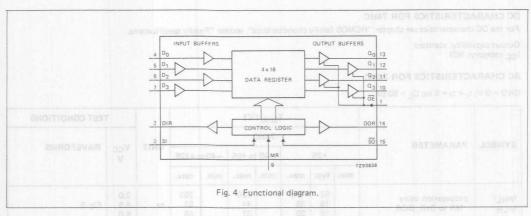
Expanded format

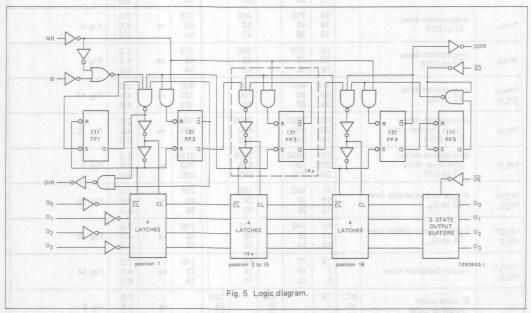
With the addition of a logic gate, the FIFO is easily expanded to increase word length (see Fig. 17). The basic operation and timing are identical to a single FIFO, with the exception of an additional gate delay on the flag outputs. If during application, the following occurs:

 SI is held HIGH when the FIFO is empty, some additional logic is required to produce a composite DIR pulse (see Figs 7 and 18).

Due to the part-to-part spread of the ripple through time, the SI signals of FIFO_A and FIFO_B will not always coincide and the AND-gate will not produce a composite flag signal. The solution is given in Fig. 18.

The "40105" is easily cascaded to increase the word capacity and no external components are needed. In the cascaded configuration, all necessary communications and timing are performed by the FIFOs. The intercommunication speed is determined by the minimum flag pulse widths and the flag delays. The data rate of cascaded devices is typically 25 MHz. Word-capacity can be expanded to and beyond 32-words × 4-bits (see Fig. 19).





Notes to Fig. 5

(see control flip-flops)

- (1) LOW on \overline{S} input of FF1 and FF5 will set Q output to HIGH independent of state on \overline{R} input.
- (2) LOW on \overline{R} input of FF2, FF3 and FF4 will set Q output to LOW independent of state on \overline{S} input.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications.

Output capability: standard I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 \text{ ns}; C_L = 50 pF$

	41,700			-	T _{amb} (°C)	I be		2 (00)	TEST CONDITIONS		
				1	74H0	2			IRI E			
SYMBOL	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.				
tphL/	propagation delay MR to DIR, DOR		52 19 15	175 35 30	sneito	220 44 37	giB	265 53 45	ns	2.0 4.5 6.0	Fig. 8	
^t PHL	propagation delay SI to DIR		52 19 15	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 6	
^t PHL	propagation delay SO to DOR		55 20 16	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 9	
^t PHL/ ^t PLH	propagation delay SO to Q _n	U	116 42 34	400 80 68	6	500 100 85		600 120 102	ns	2.0 4.5 6.0	Fig. 14	
^t PLH	propagation delay/ ripple through delay SI to DOR	V	564 205 165	2000 400 340		2500 500 425		3000 600 510	ns	2.0 4.5 6.0	Fig. 10	
^t PLH	propagation delay/ bubble-up delay SO to DIR	Y	701 255 204	2500 500 425		3125 625 532		3750 750 638	ns	2.0 4.5 6.0	Fig. 7	
^t PZH/	3-state output enable time OE to Q _n	R	41 15 12	150 30 26	- [30	190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 16	
^t PHZ [/]	3-state output disable time OE to Q _n	anota/	41 15 12	140 28 24	2	175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 16	
tTHL/ tTLH	output transition time	motives	19 7 6	75 15 13	24/3	95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 14	
t _W	SI pulse width HIGH or LOW	80 16 14	19 7 6	agram.	100 20 17	19.5	120 24 20		ns	2.0 4.5 6.0	Fig. 6	
tW	SO pulse width HIGH or LOW	120 24 20	39 14 11		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 9 of all toxino	
tw	DIR pulse width	12 6 5	58 21 17	180 36 31	10 5 4	225 45 38	10 5 4	270 54 46	ns ns	2.0 4.5 6.0	Fig. 7	
tw	DOR pulse width LOW	12 6 5	55 20 16	170 34 29	10 5 4	215 43 37	10 5 4	255 51 43	ns	2.0 4.5 6.0	Fig. 9	

AC CHARACTERISTICS FOR 74HC (Cont'd)

	Marian Tally				T _{amb} (°C)				TEST CONDITIONS		
SYMBOL	PARAMETER				74H	3	UNIT					
SAMBOL	MACRIEVAN DOV THE	+25			-40	to +85	-40 to +125		UNIT	V _{CC}	WAVEFORMS	
	Y	min.	typ.	max.	min.	max.	min.	max.				
t _W	MR pulse width HIGH	80 16 14	22 8 6	(43)	100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	
^t rem	removal time MR to SI	50 10 9	14 5 4		65 13 11		75 15 13	2	ns	2.0 4.5 6.0	Fig. 15	
t _{su}	set-up time D _n to SI	-5 -5 -5	-39 -14 -11		-5 -5 -5		-5 -5 -5	(A)	ns	2.0 4.5 6.0	Fig. 13	
th	hold time D _n to SI	125 25 21	44 16 13		155 31 26		190 38 32	81	ns	2.0 4.5 6.0	Fig. 13	
f _{max}	maximum pulse frequency SI, SO using flags or burst mode	3.6 18 21	10 30 36		2.8 14 16		2.4 12 14	24	MHz	2.0 4.5 6.0	Figs 6, 9, 11 and 12	
fmax	maximum pulse frequency SI, SO cascaded	3.6 18 21	10 30 36		2.8 14 16		2.4 12 14		MHz	2.0 4.5 6.0	Figs 6 and 9	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

5 43 24		20.0					
INPUT	UNIT LOA						
		ENI					
OE SI D _n	0.75 0.40 0.30	4.5					
SI D _n MR SO	1.50 0.40	8.8					

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

		T _{amb} (°C)						TEST CONDITIONS				
SYMBOL	PARAMETER			a 216	74HC	Т	35		UNIT	Vcc	WAVEFORMS	
0,1111002		+25			-40 to +85		-40 to +125			V	11.1721 51.1116	
		min.	typ.	max.	min.	max.	min.	max.				
tPHL/	propagation delay MR to DIR, DOR		18	35		44		53	ns	4.5	Fig. 8	
^t PHL	propagation delay SI to DIR		21	42		53		63	ns	4.5	Fig. 6	
^t PHL	propagation delay SO to DOR		20	42		53	9.1	63	ns	4.5	Fig. 9	
tPHL/ tPLH	propagation delay SO to Ω _n		40	80		100	1	120	ns	4.5	Fig. 14	
^t PLH	propagation delay/ ripple through delay SI to DOR		188	400		500		600	ns	4.5	Fig. 10 a 9	
^t PLH ST bri	propagation delay/ bubble-up delay SO to DIR		244	500		625		750	ns	4.5	Fig. 7	
t _{PZH} /	$\frac{3\text{-state output enable time}}{\text{OE}}$ to Ω_n		18	35		44		53	ns	4.5	Fig. 16	
t _{PHZ} /	3-state output disable time OE to Qn		15	30		38		45	ns	4.5	Fig. 16	
^t THL [/]	output transition time	ionge 1	7	15	is , Pani	19	isdo vil	22	ns	4.5	Fig. 14 panerio 00 srh	
tw	SI pulse width HIGH or LOW	16	6		20		24		ns	4.5	Fig. 6	
tw	SO pulse width HIGH or LOW	16	7	vip ai 1	20	Jimi B	24	IZ) jne	ns	4.5	Fig. 9	
tw	DIR pulse width HIGH or LOW	6	20	34	5	43	5	51	ns	4.5	Fig. 7	
tw	DOR pulse width HIGH or LOW	6	19	34	5	43	5	51	ns	4.5	Fig. 9	
tw	MR pulse width HIGH	16	7		20		24		ns	4.5	Fig. 8	
^t rem	removal time MR to SI	15	7		19		22		ns	4.5	Fig. 15	
^t su	set-up time D _n to SI	-5	-14		-4		-4		ns	4.5	Fig. 13	
^t h	hold time D _n to SI	27	16		34		41		ns	4.5	Fig. 13	
f _{max}	maximum pulse frequency SI, SO using flags or burst mode		28		12		10		MHz	4.5	Figs 6, 9, 11 and 12	
max	maximum pulse frequency SI, SO cascaded		28		12		10		MHz	4.5	Figs 6 and 9	

AC WAVEFORMS

Shifting in sequence FIFO empty to FIFO full

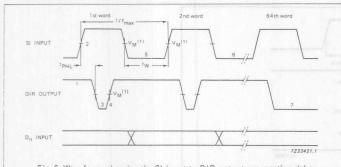


Fig. 6 Waveforms showing the SI input to DIR output propagation delay. The SI pulse width and SI maximum pulse frequency. The SI pulse width and SI maximum pulse frequency.

Notes to Fig. 6

- 1. DIR initially HIGH; FIFO is prepared for valid data.
- 2. SI set HIGH; data loaded into input stage.
- 3. DIR drops LOW, input stage "busy"
- 4. DIR goes HIGH, status flag indicates FIFO prepared for additional data; data from first location "ripple through".
- 5. SI set LOW; necessary to complete shift-in process.
- To the state of the state

With FIFO full; SI held HIGH in anticipation of empty location

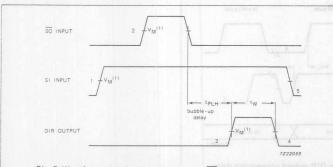


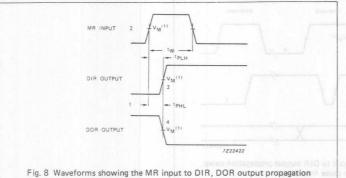
Fig. 7 Waveforms showing bubble-up delay, $\overline{\text{SO}}$ input to DIR output and DIR output pulse width.

Notes to Fig. 7

- 1. FIFO is intially, shift-in is held HIGH.
- 2. \overline{SO} pulse; data in the output stage is unloaded, "bubble-up process of empty locations begins".
- 3. DIR HIGH; when empty location reached input stage, flag indicates FIFO is prepared for data input.
- 4. DIR returns to LOW; FIFO is full again.
- 5. SI brought LOW; necessary to complete whidt-in process, DIR remains LOW, because FIFO is full.

AC WAVEFORMS

Master reset applied with FIFO full



delays and the MR pulse width.

Notes to Fig. 8

- DIR LOW, output ready HIGH; assume FIFO is full.
 MR pulse HIGH; clears FIFO.
- 3. DIR goes HIGH; flag indicates input prepared for valid data.
- 4. DOR drops LOW; flag indicates FIFO empty.

Shifting out sequence; FIFO full to FIFO empty

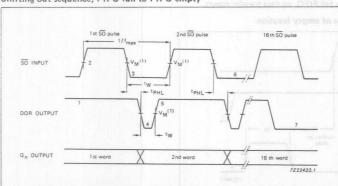


Fig. 9 Waveforms showing the SO input to DIR output propagation delay. The SO pulse width and SO maximum pulse frequency.

Notes to Fig. 9

- 1. DOR HIGH; no data transfer in progress, valid data is present at output stage.
- 2. SO set HIGH.
- 3. SO is set LOW; data in the input stage is unloaded, and new data replaces it as empty location "bubbles-up" to input stage.
- 4. DOR drops LOW; output stage "busy".
- 5. DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay.
- 6. Repeat process to unload the 3rd through to the 16th word from FIFO.
- 7. DOR remains LOW; FIFO is empty.

With FIFO empty; SO is held HIGH in anticipation

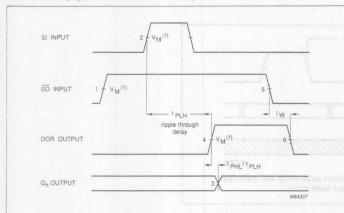


Fig. 10 Waveforms showing ripple through delay SI input to DOR output and propagation delay from the DOR pulse to the Q_n output.

Notes to Fig. 10

- 1. FIFO is initially empty, SO is held HIGH.
- 2. SI pulse; loads data into FIFO and initiates ripple through process.
- 3. DOR flag signals the arrival of valid data at the output stage.
- 4. Output transition; data arrives at output stage after the specified propagation delay between the rising edge of the DOR pulse to the Q_n output.
- 5. SO set LOW; necessary to complete shift-out process. DOR remains LOW, because FIFO is empty.
- 6. DOR goes LOW; FIFO is empty again.

Shift-in operation; high-speed burst mode

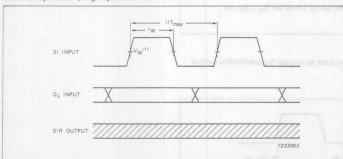


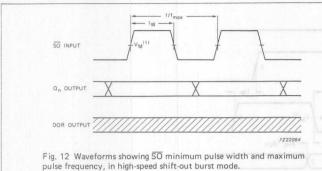
Fig. 11 Waveforms showing SI minimum pulse width and SI maximum pulse frequency, in high-speed shift-in burst mode.

Note to Fig. 11

In the high-speed mode, the burst-in rate is determined by the minimum shift-in HIGH and shift-in LOW specifications. The DIR status flag is a don't care condition, and a shift-in pulse can be applied regardless of the flag. A SI pulse which would overflow the storage capacity of the FIFO is ignored.

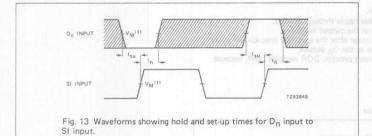
AC WAVEFORMS

Shift-out operation; high-speed burst mode



Note to Fig. 12

In the high-speed mode, the burst-out rate is determined by the minimum shift-out HIGH and shift-out LOW specifications. The DOR flag is a don't care condition and a SO pulse can be applied without regard to the flag.



Note to Fig. 13

The shaded areas indicate when the input is permitted to change for predictable output performance.

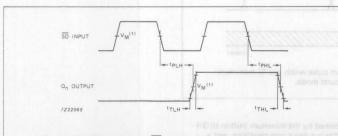
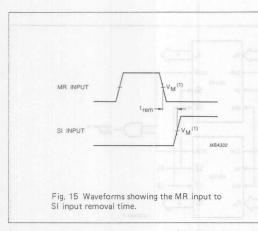


Fig. 14 Waveforms showing $\overline{\text{SO}}$ input to $\mathbf{Q}_{\mathbf{n}}$ output propagation delays and output transition time.



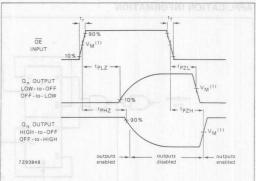
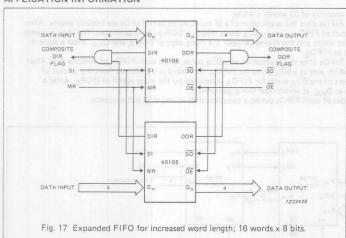


Fig. 16 Waveforms showing the 3-state enable and disable times for input $\overline{\text{OE}}$.

Note to AC waveforms

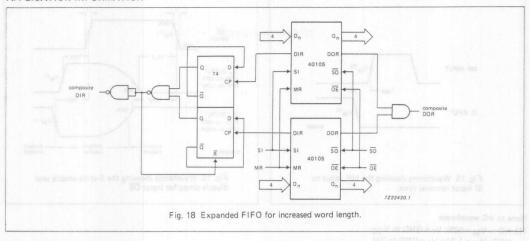
(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION



Note to Fig. 17

The PC74HC/HCT40105 is easily expanded to increase word length. Composite DIR and DOR flags are formed with the addition of an AND gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.



Note to Fig. 18

This circuit is only required if the SI input is constantly held HIGH, when the FIFO is empty and the automatic shift-in cycles are started (see Fig. 7).

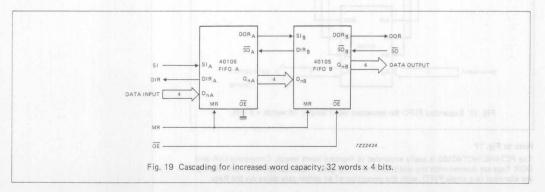
Expanded format

Fig. 19 shows two cascaded FIFOs providing a capacity of 32 words x 4 bits.

Fig. 20 shows the signals on the nodes of both FIFOs after the application of a SI pulse, when both FIFOs are initially empty. After a rippled through delay, data arrives at the output of FIFO_A. Due to \overline{SO}_A being HIGH, a DOR pulse is generated. The requirements of SI_B and D_{nB} are satisfied by the DOR_A pulse width and the timing between the rising edge of DOR_A and Q_{nA} . After a second ripple through delay, data arrives at the output of FIFO_B.

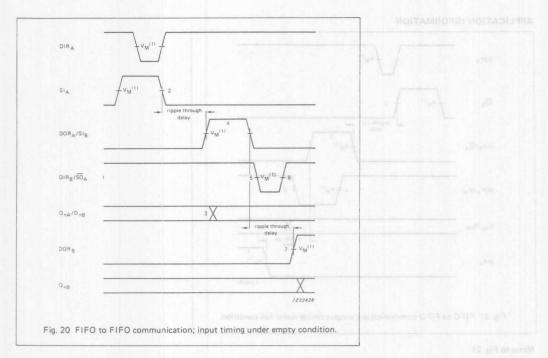
Fig. 21 shows the signals on the nodes of both FIFOs after the application of a \overline{SO}_B pulse, when both FIFOs are initially full. After a bubble-up delay a DIRB pulse is generated, which acts as a \overline{SO}_A pulse for FIFO_A. One word is transferred from the output of FIFO_B to the input of FIFO_B. The requirements of the \overline{SO}_A pulse for FIFO_A is satisfied by the pulse width of DORB. After a second bubble-up delay an empty space arrives at D_{nA} , at which time DIRA goes HIGH.

Fig. 22 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.



Note to Fig. 19

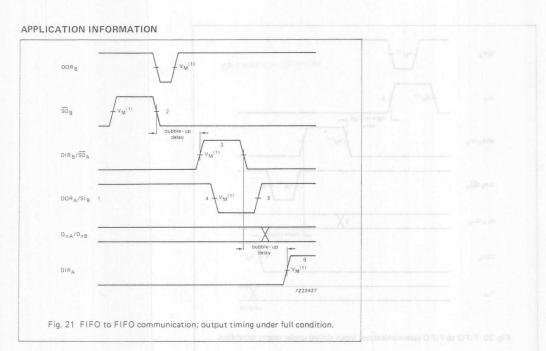
The PC74HC/HCT40105 is easily cascaded to increase word capacity without any external circuitry. In cascaded format, all necessary communications are handled by the FIFOs. Figs 17 and 19 demonstrate the intercommunication timing between FIFOA and FIFOB. Fig. 22 gives an overview of pulses and timing of two cascaded FIFOs, when shifted full and shifted empty again.



Notes to Fig. 20

- 1. FIFOA and FIFOB initially empty, \overline{SO}_A held HIGH in anticipation of data.
- 2. Load one word into FIFOA; SI pulse applied, results in DIR pulse.
- 3. Data out A/data in B transition; valid data arrives at FIFOA output stage after a
- specified delay of the DOR flag, meeting data input set-up requirements of FIFOR.

 4. DORA and SIB pulse HIGH; (ripple through delay after SIA LOW) data is unloaded from FIFOA as a result of the data output ready pulse, data is shifted into FIFOB.
- 5. DIRB and SOA go LOW; flag indicates input stage of FIFOB is busy, shift-out of FIFOA is complete.
- 6. DIRB and SOA go HIGH automatically; the input stage of FIFOB is again able to receive data, SO is held HIGH in anticipation of additional data.
- 7. DORR goes HIGH; (ripple through delay after SIR LOW) valid data is present one propagation delay later at the FIFOB output stage.



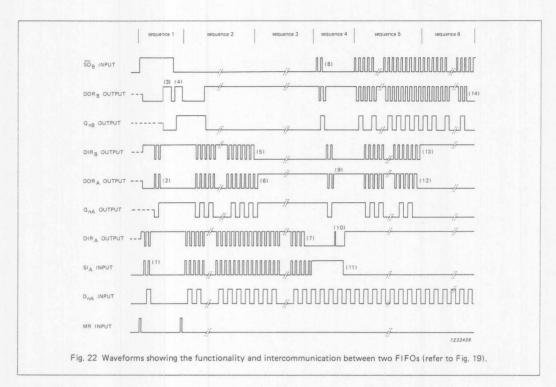
Notes to Fig. 21

- 1. FIFO $_{\mbox{\scriptsize A}}$ and FIFO $_{\mbox{\scriptsize B}}$ initially full, SI $_{\mbox{\scriptsize B}}$ held HIGH in anticipation of shifting in new

- FFO A and FIFO'S Initially full, SIS held HIGH in anticipation of shifting in new data as empty location bubbles-up.
 Unload one word from FIFO'S, SO pulse applied, results in DOR pulse.
 DIRB and SOA pulse HIGH; (bubble-up delay after SOB LOW) data is loaded into FIFO'S as a result of the DIR pulse, data is shifted out of FIFO'A.
 DORA and SIB go LOW; flag indicates the output stage of FIFO'A is busy, shift-in to FIFO'S is complete.
- 5. DORA and SIg go HIGH; flag indicates valid data is again available at FIFOA output stage, SIg is held HIGH, awaiting bubble-up of empty location.
 6. DIRA goes HIGH; (bubble-up delay after SOA LOW) an empty location is present at
- input stage of FIFOA.

Note to application waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.



Note to Fig. 22

Sequence 1 (Both FIFOs empty, starting shift-in process):

After a MR pulse has been applied FIFO_A and FIFO_B are empty. The DOR flags of FIFO_A and FIFO_B go LOW due to no valid data being present at the outputs. The DIR flags are set HIGH due to the FIFOs being ready to accept data. \overline{SO}_B is held HIGH and two \overline{SI}_A pulses are applied (1). These pulses allow two data words to ripple through to the output stage of FIFO_A and to the input stage of FIFO_B (2). When data arrives at the output of FIFO_B, a DOR_B pulse is generated (3). When \overline{SO}_B goes LOW, the first bit is shifted out and a second bit ripples through to the output after which DOR_B goes HIGH (4).

Sequence 2 (FIFOB runs full):

After the MR pulse, a series of 16 SI pulses are applied. When 16 words are shifted in, DIRB remains LOW due to FIFOB being full (5). DORA goes LOW due to FIFOB being empty.

Sequence 3 (FIFO_A runs full):

When 17 words are shifted in, DORA remains HIGH due to valid data remaining at the output of FIFOA. Q_{DA} remains HIGH, being the polarity of the 17th data word (6). After the 32th SI pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

Sequence 4 (Both FIFOs full, starting shift-out process):

SI_A is held HIGH and two SOB pulses are applied (8). These pulses shift out two words and thus allow two émpty locations to bubble-up to the input stage of FIFOB, and proceed to FIFOB, (9). When the first empty location arrives at the input of FIFOB, a DIRA pulse is generated (10) and a new word is shifted into FIFOB, SI_A is made LOW and now the second empty location reaches the input stage of FIFOB, after which DIRA remains HIGH (11).

Sequence 5 (FIFOA runs empty):

At the start of sequence 5 FIFO_A contains 15 valid words due to two words being shifted out and one word being shifted in in sequence 4. An additional series of \overline{SO}_B pulses are applied. After 15 \overline{SO}_B pulses, all words from FIFO_A are shifted into FIFO_B. DOR_A remains LOW (12).

Sequence 6 (FIFOB runs empty):

After the next \overline{SO}_B pulse, DIRB remains HIGH due to the input stage of FIFOB being empty (13). After another 15 \overline{SO}_B pulses, DORB remains LOW due to both FIFOs being empty (14). Additional \overline{SO}_B pulses have no effect. The last word remains available at the output Q_n .



Fig. 22. Waveforms showing the functionality and intercommunication between two FIFCs (later to Fig. 19)

Note to Fig. 22

Requested 1 (Both F1EOs empty, starting shift-in process):

After a MR pulse has been applied FIFOn and FIFOg are entirty. The DOR flees of FIFOn, and FIFOn go LOW due to no veild data being present at the aurouts. The DIR flees are set AIGH due to the FIFOs being present at the aurouts. The DIR flees are set AIGH due to the FIFOs being made to accept data. Suppose a public the pulses allow two data words to ripple stronger to the output of FIFOs, a DOR pulse is generated 13). When data arrives at the output of FIFOs, a DOR pulse is generated 13). When SO gloss LOW, the first bit is shifted out and a strong bit ripples through fur the output affect which (4).

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After the MR guiss, a sense of 16 St pulses are applied. When 15 words are shifted in, DIR's remains LOW due to FIFOs being but
15. DORA goes LOW due to FIFOs being enjoy.

Sequence 3 (FIFO x roms full):

When 17 words are shifted in DORA remains HIGH due to valid data remaining at the output of FIFOA Drug remains HIGH, bring the 17th data word (St. After the 32th S) gates. Other remains LOW and cosh FIFOs are full (7). Additional pulses have no effect.

sequence 4 (Born FTP Os full, starting shift our arrosses)

SIA is held HIGH and two SÜg goles on applied (8). These pulses shift our two words and thus allow redesignty breatists to bubble up to the input stage of FIFOg, and preced to FIFOA (9). When the time empty location actives at the input of FIFOA and fire shifted and FIFOA, all is stade LOW and how the second empty location reaches the location creatives.

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At the start of sequence 5 FIFO_A contains 15 valid words due to two words being distract out and one word being shifted in in servement A. An edutional service of 50g outless are applied. After 15 Stag pulses, all words from FIFO_A are distract into FIFO_B professional services. LOW 151.

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The time next SOB pures. DIRBy remains HISM due to the input, sage of FIF Ob being empty (13). After another 15 SOB output, 100 pures to a first. Of the last word remains swellable at 100 pures. The last word remains swellable at the output (0...) to output (0...).

APPLICATION NOTES

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APPLICATION NOTES

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1401

CONT

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Handling precautions

ower supply decoupling

Power dissipation

HANDLING PRECAUTIONS

Electrostatic charges

Electrostatic charges can be stored in many things; for example, man-made fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depends on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our CMOS ICs are internally protected against electrostatic discharge, but they can be damaged if the following precautions are not taken.

Work station

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is 1 $k\Omega$ to $0.5~\mathrm{M}\Omega$ per cm². The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work-bench should be earthed via a wrist strap and a resistor
- All electrical equipment should be connected to the mains via an earth-leakage switch and the equipment cases should be earthed.
- Relative humidity should be maintained between 50% and 65%
- An ionizer should be used to neutralize objects with immobile static charges.

Receipt and storage

CMOS ICs are packed for despatch in antistatic/conductive boxes, rails or blister tape. The fact that the ICs are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The ICs should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the task should be performed at a protected work station. Any CMOS ICs that are temporarily stored should be packed in conductive or antistatic packing or carriers.

Assembly

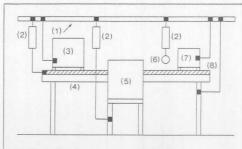
CMOS ICs must be removed from their protective packing with earthed component-pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Don't remove more ICs from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the CMOS ICs are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand-tools should be of conductive or antistatic material and, where possible, not

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board doesn't touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Handle assembled circuit boards containing CMOS ICs in the same way as unmounted CMOS ICs. They should also carry warning labels and be packed in conductive or antistatic packing.



- (1) Earthing rail
- (5) Chair
- (2) Resistor (500 k Ω ± 10%, (6) Wrist strap
- 0.5 W) (3) Ionizer (4) Work bench
- (7) Electrical equipment (8) Conductive surface/
- antistatic sheet

Fig. 1 Protected work station.

ANDLING PRECAUTIONS

Electrostatic charges

Electrostatic charges can be stored in many things; for example, man-made fibre electhing, moving mechinery, objects with air blowing ecross them, plastic storage bins, shedts of paper stored in plastic envelopes, paper from electrostatic coopying machines, and papels. The charges are caused by fiction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the trianges depends on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding six.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different botentials and occurs with direct contact or when induced by an electrostatic field. All of our CMOS ICs are internally protected against electrostatic discharge, but they can be damaged if the following precautions are not taken.

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- Persons at a work-bench should be earthed via a wrist
 areap and a resistor.
- All electrical equipment should be connected to the mains via an earth-leakage switch and the equipment cases should be earth-leakage.
- Relative humidity should be maintained between 50% and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

Receipt and storage

CMOS IGs are packed for despetch in antistatio/conductive boxes, rails or bilister tape. The fact that the IGs are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The JCs should be kept in their original pecking whilst in norage. If a bulk compliner is partially unpecked, the task thould be performed at a protected work station. Any CMOS ICs there are temporarily stored should be pecked in conductive or antistatio pecking or carriers.

Assembly

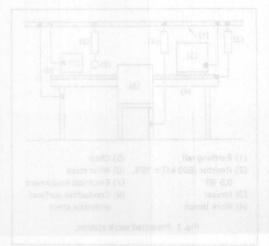
CMOS ICs must be removed from their protective packing with vertised component-pincers or stront-elecuit office. Shart-circuit dies must remain in place during mounting soldering and cleansing dirving processes. Don't remove more ICs from the storage packing than are needed at any one time. Production/essembly documents should state that the product contains electrostatic censive devices and that conceils present to be raken.

During assembly, ensure that the CMOS JOs are the lest of the components to be mounted and that this is done at a protected work station.

All tools used during assambly, including soldsring tools and solder better, must be sarthed. All hand-tools should be of conductive or antistatic material and, where possible, not insulated.

Mescuring and teating of dompleted circuit boards must be done at a protested work station, Place the soldened side of the circuit board on conductive or antistatic form and remove the short-circuit slips. Remove the short-circuit slips. Remove the short-circuit sloped from the form, holding the board only at the edges. Make are the circuit board doesn't touch the conductive surface of the work bench, After resting, replace the circuit board on the conductive foam to swell packing.

Handle assembled circuit boards containing CMOS ICs in the same way as unmounted CMOS ICs. They should also carry warning labels and be packed in conductive or antistatic packing.



POWER SUPPLY LINE LAYOUT AND DECOUPLING RECOMMENDATIONS

Spikes due to output current switching and the charging and discharging of parasitic capacitance, are the two main sources of noise on the power lines of HCMOS logic systems. To minimize noise, the power supply should be decoupled. However, if switching speed is high, not only the voltage dips on the power lines must be considered but also the effects of di/dt radiation. Decoupling requirements are a balance between the precautions necessary to reduce the effects of these two phenomena.

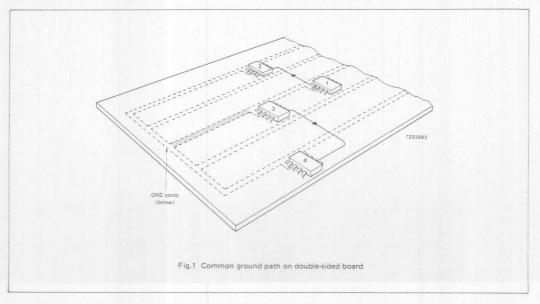
The first requirement for minimizing noise is a well designed power distribution network. For instance, it is essential to have a good ground (GND) connection pattern on a pcb. Even the commonly used GND pattern shown in Fig.1 can cause problems. In Fig.1, an output from IC1 drives an input of IC2, and an output from IC3 drives an input of IC4. Since the signal paths between IC1 and IC2, and between IC3 and IC4 are not coupled, there should be no crosstalk between them. However, IC1 and IC3 share the hatched section of the GND comb, and, when the output of IC1 switches, a spike could be generated on the GND of IC3. This could be transmitted to IC4 via the IC3-IC4 signal connection causing the output of IC4 to switch erroneously. If a double-sided board is used, it is therefore advisable to reduce the length of individual sections of the GND comb by installing links on the opposite side of the board as shown in Fig.2. This is especially important for boards on which high level currents are switched.

It is bad practice to use jumpers to connect GND/V_{CC} pins of ICs to pcb tracks (Fig.3). Jumpers are unlikely to be used on production boards, but they should not be used on prototype or one-off boards either because the inductance they introduce into the lines causes coupling between outputs. Printed connections should therefore be used to interconnect power tracks and IC pins. An even better solution is to use multi-layer boards so that individual layers can be used as a V_{CC} plane and a groundplane. The power supply can then be connected directly to the IC supply pins. Also, the inherent capacitance between the V_{CC} plane and the groundplane will reduce the amplitude of any high frequency noise on the power supply.

This inherent capacitance has the distinct advantage of being free from the inductance associated with discrete decoupling capacitors. A less expensive alternative to a multi-layer board is a multi-wire board which offers the same high frequency noise characteristics. With double-sided boards, it is not possible to dedicate a layer to a VCC plane and a groundplane. Nevertheless, if at all possible, it is still best to have the VCC and ground tracks on opposite sides of the board.

Connectors on any type of pcb should each have at least five ground pins to obtain good distribution of ground current.

The precautions outlined for ground tracks on the pcb are equally applicable to the power (VCC) lines.



POWER SUPPLY DECOUPLING

The wide HCMOS power supply range of 2 V to 6 V may suggest that voltage regulation is not necessary, but it must be remembered that supply voltage level variations will influence switching speed, noise immunity and power consumption. Supply voltage differences between ICs must also be avoided because a difference of as little as 0,5 V between power lines can cause unwanted effects. To isolate noise sources and avoid the use of a large voltage stabilizer with its heavy gauge (low impedance) wiring to each board, it is better to have a separate stabilizer for each board. However, care must be taken because a fault on a stabilizer for one board may be transmitted via the HCMOS input structure to other boards, possibly causing damage.

No matter how good the V_{CC} and GND connections are, all line inductance cannot be eliminated. This is where decoupling plays its part.

Ceramic capacitors are best for decoupling because they have very low series inductance. The advantage of using them will, however, be lost if they are connected too far from the IC. The inductance of the long tracks in conjunction with the capacitor will then form a very high-Q LC tuned-circuit, and the oscillations produced will have a worse effect than not having any decoupling at all. If it is impossible to make connections between decoupling capacitors and ICs shorter than 20 mm, then use several tracks connected in parallel and separated by at least one track-width (Fig.4). Some ceramic capacitors have preformed leads as shown in Fig.5(a). These leads introduce

unwanted inductance. It is better to use capacitors with straight leads mounted as shown in Fig.5(b).

In general, the minimum requirements for good decoupling are:

- one 47 μF bulk capacitor per Eurocard
- one $1\,\mu\text{F}$ tantalum capacitor per 10 packages of SSI logic
- one 22 nF ceramic capacitor for each octal IC and for each counter/shift register (MSI logic)
- one 22 nF ceramic capacitor per 4 packages of SSI logic

An example showing how to determine the value of decoupling capacitor follows. Assume a buffer output sees a 100 Ω dynamic load and the output LOW-to-HIGH transition is 5 V; the current demand is therefore 50 mA per output. For an octal buffer, the current demand would be 0.4 A for 6 ns.

The instantaneous current in the capacitor is:

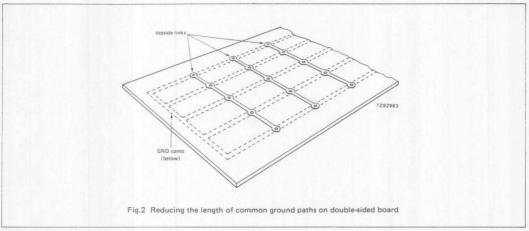
$$i = \frac{\Delta Q}{\Delta t}$$

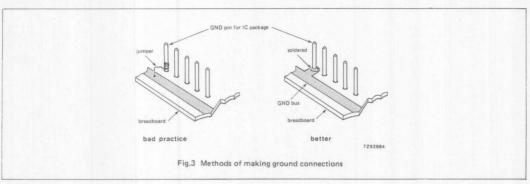
And
$$i = \frac{C\Delta V}{\Delta t}$$
 (from Q = CV)

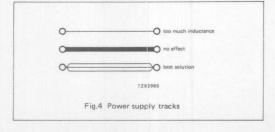
Therefore,
$$C = \frac{i\Delta t}{\Delta V}$$

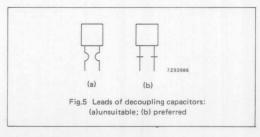
For an octal buffer and a change in VCC of 0,4 V say,

$$C = \frac{0.4 \text{ A} \times 6 \times 10^{-9} \text{ ns}}{0.4 \text{ V}} = 6 \text{ nF}.$$









POWER DISSIPATION CONSIDERATIONS

For LSTTL logic ICs operating below 10 MHz, the most significant part of the total power dissipation is the quiescent power dissipation due to the many bipolar transistors that continuously conduct. With HCMOS logic ICs however, the converse is true because quiescent power dissipation is only due to leakage currents through reverse-biased junctions and is so low that it is practically negligible compared with the frequency-dependent dynamic power dissipation.

Since the logic functions in most systems only change state during brief periods, the average system frequency is between one and two orders of magnitude lower than the system clock frequency and the ICs therefore only draw quiescent current for most of the time. This means that replacing LSTTL ICs with equivalent 74HCT ICs, with their much lower quiescent power dissipation, results in a very significant reduction of overall system power dissipation without loss of operating speed.

However, total system power dissipation, is the sum of both the quiescent and the dynamic power dissipation of all the ICs and must be determined and minimized during system design. For LSTTL, where the quiescent power dissipation is the most significant contributor to the total power dissipation, the total power dissipation can be simply derived from the product of VCC and ICC given in the data sheets. For HCMOS circuits however, the dynamic power dissipation which is the most significant part of the total power dissipation is influenced by circuit design. It cannot be read direct from the data sheets but must be calculated from the supply voltage, average switching frequency, load capacitance, internal capacitances of the IC, and transient switching currents.

This article explains how our method of specifying HCMOS ICs in the data sheets makes it very simple to calculate their quiescent, dynamic and total power dissipation.

QUIESCENT POWER DISSIPATION

Quiescent power is dissipated by an IC when it is not switching and $V_1 = V_{CC}$ or GND. Figure 1(a) will be used to illustrate this power dissipation in HCMOS ICs. In the quiescent state, either the PMOS or the NMOS transistor is fully off and, in theory, no direct MOS transistor channel path exists between V_{CC} and GND. In practice however, thermally generated minority charge-carriers, which are present in all reverse-biased diode junctions, allow a very small leakage current to flow between V_{CC} and GND. This quiescent supply current (I_{CC}) is specified in the published

Three factors influence the value of ICC, and therefore the quiescent power dissipation, for a particular IC. They are:

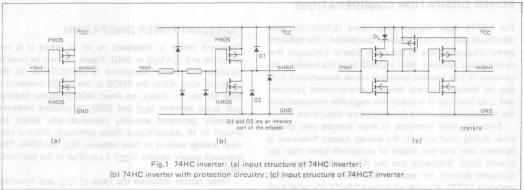
Temperature: increasing temperature causes I_{CC} to increase because the minority charge-carriers in the reverse-biased diode junctions are thermally generated.

Device Complexity: MSI circuits dissipate more power than SSI circuits because they have a proportionally greater reverse-biased diode junction area.

Supply voltage: the number of minority charge-carriers is linearly related to reverse junction voltage.

Table 1 shows the JEDEC industry standard for the worst-case I_{CC} in HCMOS ICs. It shows the effect of temperature and circuit complexity on I_{CC} at the maximum recommended supply voltage V_{CC} . I_{CC} can be linearly derated for other supply voltages and would be approximately one-third of the value in Table 1 for a 74HC IC with $V_{CC} = 2$ V. Typical I_{CC} values are well below the maximum specified values.

	JEDEC	industry	stand DC c	dard for	ABLE 1 d.c. characteristics for 74HC/H	stics of	HCMOS	ICs			
		16.00			T _{amb} (°C)	ed blu	po rodais	en qu-flu	te	st condi	tions
	parameter	+25		74HC/HCT							
symbol					-40 to +85 -40 to +125						V _I other
		min.	typ.	max.	min. max.			u ad ato			
	quiescent supply current				JEI row						
Icc	SSI	-	-	2,0	20,0	tu to	40,0	μΑ	5,5	Vcc	10 = 0
lcc	flip-flops	-	-	4,0	40,0	TEL	80,0	μА	5,5	or	10 = 0
Icc	MSI	up ylago	3 E.pli	8,0	80,0	iU Tine	160,0	μΑ	5,5	GND	10 = 0
* for HC,	V _{CC} = 6 V.	= 95V			Mapsaup o Tert The						

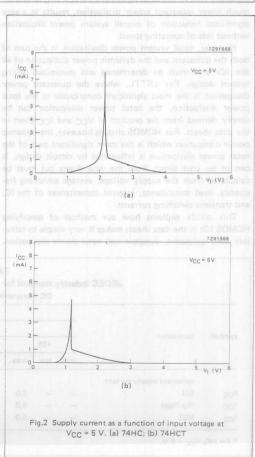


Another factor which influences quiescent power dissipation is the steady-state input voltage level which may slightly turn-on one of the input transistors shown in Fig.1(a) and yet not fully turn-off the other. This causes a small additional quiescent supply current (ΔI_{CC}) to flow between V_{CC} and GND. The level of ΔI_{CC} depends on the size of the input transistors and is different for each device.

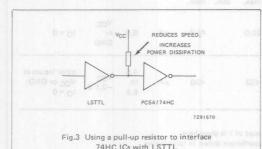
In a system consisting entirely of 74HC ICs, the additional quiescent supply current ΔI_{CC} is so small that it can be omitted from practical power dissipation calculations. This is because 74HC outputs swing from GND to V_{CC}. The worst-case output levels with $|I_{O}|=20\,\mu\text{A}$ are V_{OL}=0,1 V max. and V_{OH}=V_{CC}-0,1 V min., very close to GND and V_{CC} respectively. Figure 2(a) shows that ΔI_{CC} is negligible when these levels are applied to 74HC inputs because they always turn one of the input transistors fully off.

However, if 74HC input levels are held close to the switching threshold (typically V_{CC}/2), Fig.2 shows that the additional quiescent supply current (Δ_{CC}) becomes much greater than quiescent supply current I_{CC}. This occurs if the mistake is made of driving a 74HC input from a TTL output. With a minimum TTL V_{OH} of 2,4 V driving a 74HC input, not only will a logic "1" probably not be recognized, but several milliamps of (Δ_{CC}) will flow. To overcome this problem, an external pull-up resistor could be used as shown in Fig.3 but the resistor would dissipate significant power because its value would have to be low to maintain switching speed. 74HCT ICs have TTL input switching levels and should therefore be used instead of 74HC ICs whenever it is necessary to interface HCMOS with TTL logic.

Unlike 74HC ICs, 74HCT ICs can be substituted for LSTTL ICs and/or mixed with LSTTL, ALSTTL, ASTTL or FAST-TTL family ICs in the same system. Under some conditions, they may dissipate somewhat more quiescent power than 74HC ICs. For example, Fig.2(b) shows that a worst-case TTL VOL of 0,5 V max. is close enough to GND



to turn the input NMOS transistor fully off so that ΔI_{CC} is close to zero. However, a worst-case TTL VOH of 2,4 V min. causes some ΔI_{CC} to flow. For this reason, 74HCT data sheets specify I_{CC} at the worst-case input voltage of $V_{CC}-2.1\,V$ for V_{CC} ranging from 4,5 V to 5,5 V. It is further specified on a per input pin basis to allow more accurate power dissipation calculations if all the functions within an I_{CC} are not being used, or are being driven by different input voltage levels.



Our proprietary 74HCT input structure shown in Fig.1(c) considerably reduces the additional quiescent supply current ΔI_{CC} . The structure is identical to that for 74HC circuits except for a level-shifting diode between the PMOS transistor and V_{CC} , and the connection of the substrate of the CMOS transistor to V_{CC} . The effect is to reduce the input level switching threshold to 28WVC_{C} instead of 50WVC_{C} as is the case with 74HC ICs. This therefore reduces the additional quiescent current ΔI_{CC} when a TTL minimum HIGH level of 2,4 V is applied to a 74HCT input by ensuring that the PMOS transistor is fully turned off. Figure 2(b) shows that ΔI_{CC} is negligible when a 74HCT input is held at a typical TTL HIGH output level (3,4 V) or LOW output level (0,25 V).

Calculating 74HC quiescent power dissipation

For power-critical applications such as battery-powered equipment, it may be necessary to calculate 74HC quiescent power dissipation as a standby value of battery drain. It is given by:

VCC is dependent upon the particular application, we recommend that a $\pm 10\%$ variation be allowed. ICC at VCCmax is obtained from the data sheet for the particular IC. For critical battery-powered applications, the value of ICC can be linearly derated for any desired VCC; for example, at VCC = 2 V, use one-third of the limits shown in Table 1 for 74HC ICs.

Calculating 74HCT quiescent power dissipation

Assume that an LSTTL IC with an output duty factor of 0,5 is switching one gate input in a 74HCT11 (triple 3-input AND gate) with a 5 V supply and an ambient temperature of 25 °C. Quiescent power dissipation is calculated from:

$$P_{QHCT} = V_{CC}(I_{CC} + \delta \Delta I_{CC})$$
 (2)

where δ = switching duty factor.

 ΔI_{CCmax} is calculated on a unit-load basis from the part of the data sheet reproduced in Table 2:

 $\Delta I_{CCmax} = 360 \,\mu\text{A}$ per input pin x 1 pin x 0,5 unit-load coefficient = 180 μA .

Inserting this current and the values for V_{CC} (5,5 V), I_{CC} = 2μ A from Table 2, and δ (0,5) into equation (2) gives:

POHCT =
$$5.5 \text{ V} [2 \mu\text{A} + (0.5 \times 180 \mu\text{A})] = 506 \mu\text{W}.$$

This is only 2% of the 25,5 mW maximum quiescent power that would be dissipated by the equivalent LSTTL IC. Furthermore, as previously stated, the ΔI_{CC} of $360\,\mu\text{A}$ per input pin quoted in Table 2 for the 74HCT11 IC is based on a worst-case HIGH input level of $V_{CC}-2,1\,V$. In a typical application, the TTL HIGH input level driving the IC would be much higher than this, resulting in a reduction of ΔI_{CC} by an order of magnitude.

If all the inputs of a 74HCT IC are driven by 74HC or equivalent CMOS outputs, the input levels are such that the additional quiescent supply current Δ I_{CC} is so small that it can be omitted from 74HCT power dissipation calculations. 74HC quiescent power dissipation equation (1) can then be used to calculate 74HCT quiescent power dissipation.

DYNAMIC POWER DISSIPATION

Unlike quiescent power dissipation, dynamic power dissipation is calculated in the same manner for both 74HC and 74HCT ICs. All equations presented here for dynamic power dissipation are therefore applicable to both 74HC and 74HCT ICs.

Three factors influence the dynamic power dissipation of HCMOS ICs. They are load capacitance, internal capacitance and switching transient currents (through-currents of transistor pairs when both transistors momentarily conduct during logic level transitions).

TABLE 2
Specification of ICC, Δ ICC and unit load coefficient for 74HCT11 triple 3-input AND gate

		T _{amb} (°C)							test conditions			
symbol	parameter	OHO ST 74HCT more functional and line if a						photologic		erragizali	מסטראות חסשופר נ	
		b paints +25 = 6 stante		-40 to +85 -40 to +12		to +125	unit	V _{CC}		other		
from the p	sind beekling a no baral	min.	typ.	max.	min.	max.	min.	max.		-219	val agaziro	rterent input vi
Icc	quiescent supply current			2,0		20,0		40,0	μΑ	5,5	VCC or GND	10 = 0
ΔICC	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μА	4,5 to 5,5	V _{CC} -2,1 V	other inputs at VCC or GND:

Note:

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
 To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in table below.

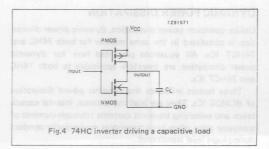
0.01.11.100	unit load
input	coefficient
nA, nB, nC	0,5

Load capacitance

The first contribution to dynamic power dissipation is caused by the charging and discharging of external capacitive loads. Figure 4 illustrates an HCMOS inverter with a capacitive load and, together with the following equations, will help to illustrate how load capacitance consumes power. The energy dissipated (joules) in charging and discharging the capacitive load is:

$$P_{CL}t = C_L V_{CC}^2$$
 (3

where t = $1/f_0$ and C_L = total external load capacitance due to interconnections, driven inputs and any sockets that are used.



The dynamic power dissipation due to capacitive loads is therefore:

$$P_{CL} = C_L V_{CC}^2 f_0 \tag{4}$$

Equation (4) is only applicable if all the outputs are switching the same load. If they are not, the equation becomes:

$$P_{CL} = \Sigma(C_L V_{CC}^2 f_0)$$
 (5)

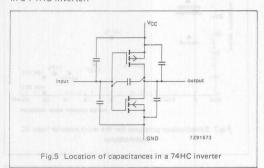
For multiple output ICs, it is important to calculate with the appropriate output frequency. For example, at either output from a flip-flop, $f_0 = f_i/2$; for a 7-stage binary ripple counter (type 74HC/HCT4024), f_0 is halved for each successive output stage so that $f_0 = f_i/64$ for the final output stage.

Internal capacitance

All MOS logic ICs have internal parasitic capacitance caused by diode junctions, MOS transistor structures, and the aluminium and polysilicon interconnections. It has the same effect as external capacitive loads, and its magnitude depends on the complexity of the circuit.

HCMOS ICs are manufactured with a self-aligned polysilicon gate process ($3\mu m$ gate length) and local oxidation to reduce internal capacitance by minimising gate-to-source

and gate-to-drain capacitances. The junction capacitances, which are proportional to junction area, are smaller than those in HE4000B CMOS ICs because the diffusions are shallower. Figure 5 shows the location of the capacitances in a 74HC inverter.



For power dissipation calculation purposes, the total load caused by internal capacitances and by switching transient currents is defined as a single effective internal no-load power dissipation capacitance CPD. It is defined in the data sheet for each HCMOS IC on a 'per function' basis and, where appropriate, it is also separately specified for each different logic function (e.g. gate or flip-flop) within an IC. This allows more accurate power dissipation calculations to be made if logic functions within the same IC are operating at different frequencies.

The published figure for CPD is valid for the worst-case operating mode under typical operating conditions. For example, in the case of a NAND gate, the state of the inputs is assumed to be such that the output is changing state; for a shift register or D-type flip-flop, it is assumed that alternately HIGH/LOW data is being clocked in. The specified value for CPD however is a typical one; nevertheless, some protection will already be built-in to dynamic power dissipation calculations because the assumed worst-case operating modes don't always occur. Although we're not yet prepared to officially publish a maximum value for CPD, a rough guide would be to increase the published figure by 50% for worst-case calculations. The method of measuring CPD is explained in the chapter "User Guide".

Switching transient currents

The final factor that contributes to the dynamic power dissipation of HCMOS is internal switching transient currents. When the output of a basic HCMOS inverter as shown in Fig.6(a) changes state, either from a logic "1" to a logic "0" or vice-versa, there is a brief period during which both transistors conduct. This creates a temporary low-resistance path between VCC and GND as shown in

Fig.6(b). In this transistory state, additional supply current (ΔI_{CC}) flows and power is dissipated, so input rise and fall times should be kept short. The average value of this transient current increases linearly with increasing switching frequency. In other words, power dissipation due to switching (like power dissipation due to internal capacitance) increases linearly with increasing switching frequency. However, since it is small compared to the power dissipation due to internal capacitance, its effect is included in the published value of power dissipation capacitance (CPD) which has discussed under the previous heading.

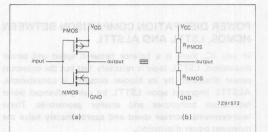


Fig.6 When an HCMOS inverter changes state, both input transistors momentarily conduct: (a) inverter input structure; (b) equivalent circuit when the input level is between logic levels

Total dynamic power dissipation

Since CPD represents the load imposed by both internal capacitance and switching transient currents, the total dynamic power dissipation due to these factors is:

$$P_{DYN} = C_{PD}V_{CC}^2 f_i$$
 (6)

The total dynamic power dissipation of HCMOS ICs is obtained by adding equation (6) to the power dissipation due to the total external capacitive load (equation 5) and is given by:

$$P_{D} = C_{PD}V_{CC}^{2}f_{i} + \Sigma (C_{L}V_{CC}^{2}f_{o})$$
 (7)

CALCULATING TOTAL POWER DISSIPATION FOR 74HC AND 74HCT ICs

Total HCMOS power dissipation is a summation of the appropriate quiescent and dynamic power dissipation formulae previously described.

For 74HC/HCT ICs driven by CMOS levels:

$$P_{tot} = V_{CC}I_{CC} + C_{PD}V_{CC}^2f_i + \sum (C_LV_{CC}^2f_o)$$
 (8)

For 74HCT ICs driven by TTL:

$$P_{tot} = V_{CC}(I_{CC} + \delta \Delta I_{CC}) + C_{PD}V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o)$$
 (9)

POWER DISSIPATION IN OSCILLATORS AND ONE-SHOTS

The information presented so far is only valid for ICs switching rapidly between logic levels. Additional quiescent supply current ΔI_{CC} is greater for one-shots, oscillators and gates arranged as oscillators because, in these applications, the input slowly passes through the switching threshold (typically 50%VCC for 74HC ICs and 28%VCC for 74HCT ICs) causing flow-through current as shown in Fig.2.

POWER DISSIPATION COMPARISON BETWEEN HCMOS, LSTTL AND ALSTTL

In any IC, there is a balance between speed and power dissipation. LSTTL logic is relatively fast but the quiescent power dissipated by its bipolar circuitry is considerable. ALSTTL improves upon LSTTL by using advanced wafer fabrication techniques and smaller geometries. These improvements increase speed and approximately halve the quiescent power dissipation.

CMOS ICs dissipate negligible quiescent power compared with all bipolar TTL logic ICs but, until the development of the HCMOS family, CMOS ICs were relatively slow. Use of advanced wafer fabrication techniques and smaller geometries has now made it possible for HCMOS to match the speed of LSTTL and yet retain the substantial power savings afforded by CMOS. Figure 7 shows the speed-power products for today's most popular logic IC technologies.

Figures 8 and 9 compare the dynamic power dissipation of SSI and MSI for 74HC, and LSTTL ICs. These graphs show that 74HC ICs maintain their power dissipation advantages for switching frequencies up to several MHz. This is because power is only dissipated during switching. The constant, frequency-independent power dissipation exhibited by LSTTL ICs is caused by the many bipolar transistors that continuously conduct.

Figures 8 and 9 also show that, as device complexity increases, the frequency at which HCMOS ICs dissipate the same amount of power as LSTTL ICs also increases. This is because, as LSTTL complexity increases, there are more resistive paths between VCC and GND which carry more quiescent bias current and thus cause more quiescent power dissipation. HCMOS ICs also dissipate more quiescent power as their complexity increases, but the leakage currents which cause it are so small that it can be ignored.

The power dissipation of the different logic IC technologies is translated into total system power as a function of frequency in Fig.10 which is for a small system consisting of one gate and two flip-flops. The graph shows that HCMOS also dissipates substantially less power than LSTTL at the system level.

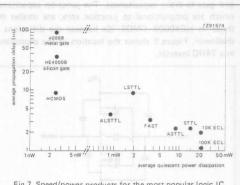
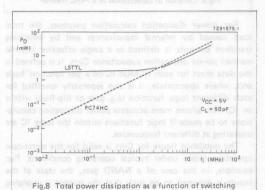
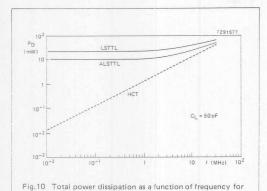


Fig.7 Speed/power products for the most popular logic IC technologies



frequency for gates and all the land

a dual flip-flop with one of the flip-flops toggling



a small system comprising one gate and two flip-flops

INFLUENCE OF HCMOS ICs ON APPLICATIONS

The significantly lower power dissipation in an HCMOS logic system, compared with its LSTTL or ALSTTL equivalent, is the primary reason why HCMOS ICs should be used for new system designs and to replace LSTTL or ALSTTL ICs in many existing designs where power consumption and/or dissipation is a problem.

For new designs, HCMOS is the only suitable family of logic ICs for battery-powered portable personal computers. The use of HCMOS is *the* major trend in personal computers using all CMOS microprocessors, RAMs, ROMs, and peripherals. All CMOS designs can be powered-down to 2 V standby to extend battery life.

For non-portable equipment, the use of HCMOS logic and CMOS LSI is also preferred because it not only reduces power dissipation, but also significantly reduces, in order of priority, cost, size, and weight. Cost reductions stem from major reductions of power supply current and regulation, cooling fans, heatsinks, and copper buses.

An equally powerful motivating force for using HCMOS logic ICs with their lower power dissipation is the inherent and proven increase of component and equipment reliability. Equipment life is considerably extended because IC junction temperatures are much reduced and other components are exposed to lower ambient temperatures.



9.10 Total power dissipation as a function of frequency for a small system comprising one gets and two flip-flops

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PACKAGE INFORMATION

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Outline drawings

Soldering 1429

PACKAGE INFORMATION

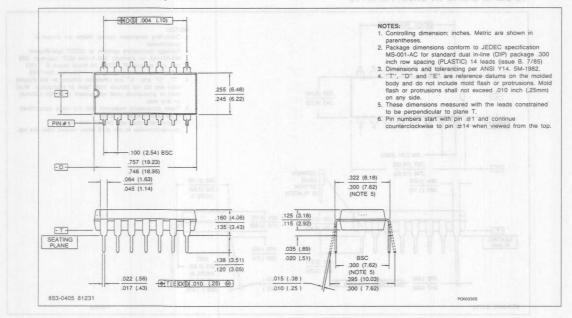
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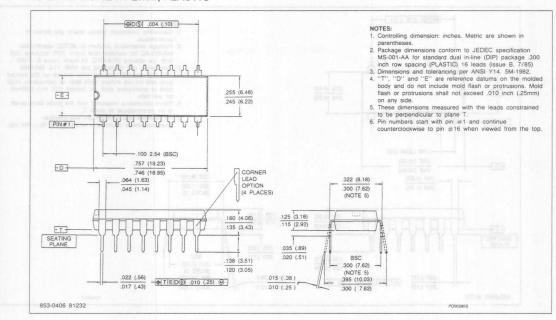
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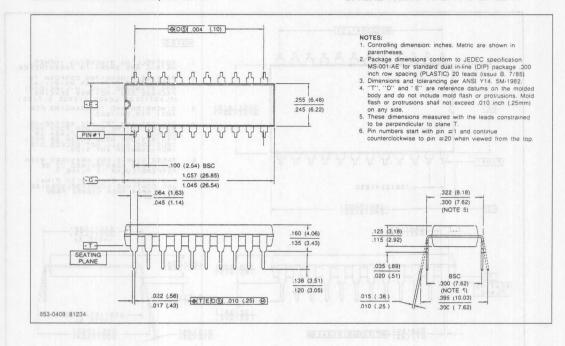
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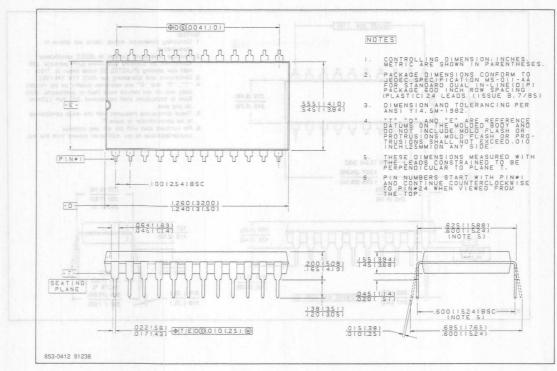
Outline drawings

Soldering

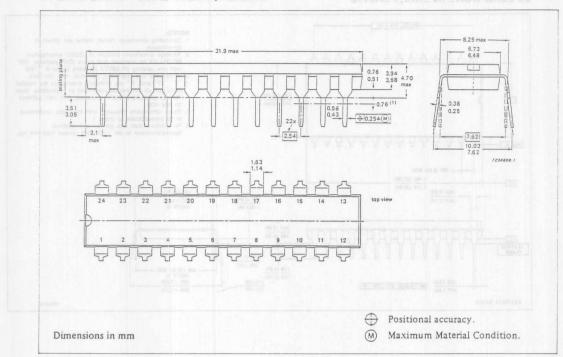


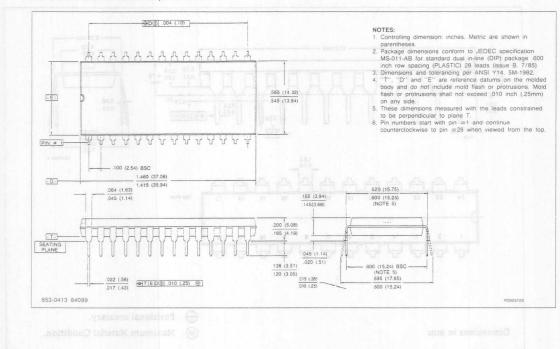


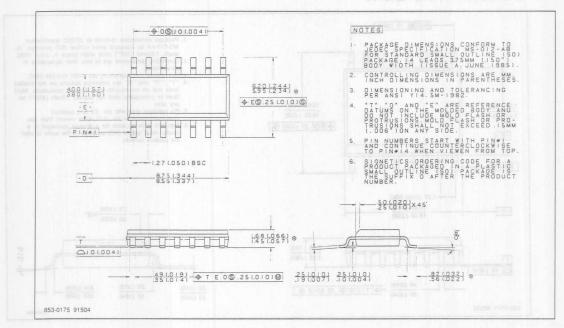


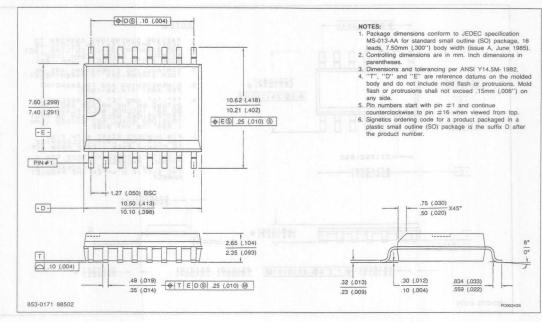


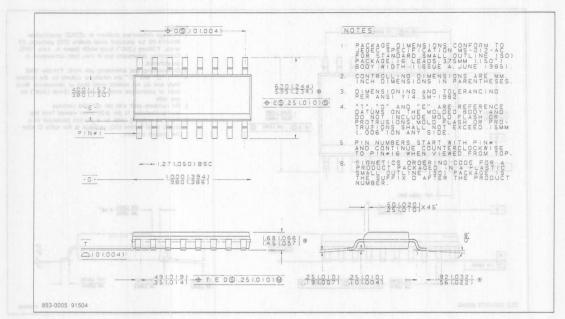
24-LEAD SKINNY DUAL IN-LINE; PLASTIC



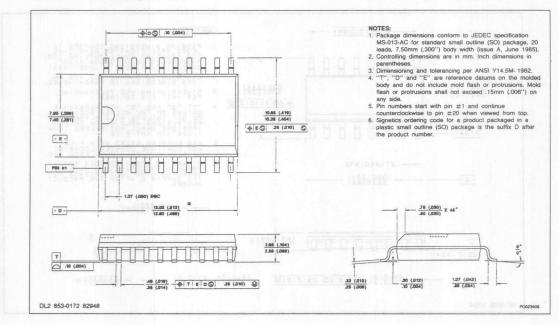




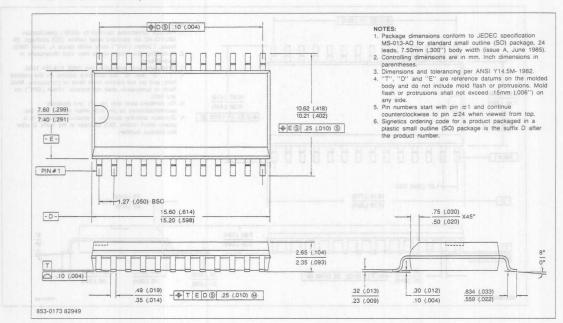


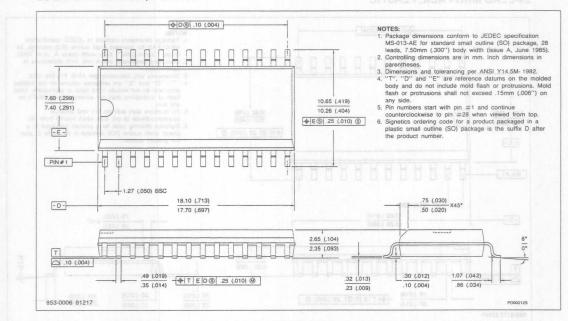


16 J EAD MINI-PACK - PLASTIC



Package outlines





SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is $260\,^{\circ}$ C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than $150\,^{\circ}$ C within 6 seconds. Typical dwell time is 4 seconds at $250\,^{\circ}$ C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement. Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is $260\,^{\circ}\text{C}$; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

SOLDERING PLASTIC MINI-PACKS

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2. By wave

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Maximum permissible solder temperature is 260°C. and maximum duration of package immersion in solde bath is 10 seconds, if allowed to cool to less than 150°C within 6 seconds. Typical dwall time is 4 seconds at 250°C.

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Data handbook system

DATA HANDBOOK SYSTEM

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IC02	Semiconductors for Television and Video Systems
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IC04	CMOS HE4000B Logic Family

IC05	Advanced Low-power Schottky (ALS)
	Logic Series

IC06	High-speed CMOS Logic Family
IC08	100K ECL Logic Family

a la	HISTORY FAM IN
IC10	Memories

IC11	General-purpose/Linear ICs	

IC12	Display Drivers and Microcontroller
	Peripherals (planned)

1013	Programmable Logic Devices (PLL
IC14	8048-based 8-bit Microcontrollers

1014	8048-based	8-bit Microcontrolle
IC15	FAST TTI I	ogic Series

IC16 ICs for Clocks and Watc	hes

IC18 Semiconductors for In-car Electronics and General Industrial Applications (planned)

IC19 Semiconductors for Datacom: LANs, UARTs, Multi-protocol Controllers and Fibre Optics

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IC21 68000-based 16-bit Microcontrollers (planned)

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IC23 QUBIC Advanced BiCMOS Interface Logic ABT, MULTIBYTE™

IC24 Low Voltage CMOS & BiCMOS Logic

Discrete semiconductors

Book	Title EXOCBONAH	
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SC02	Power Diodes odonan stab sylenanes	
SC03	Thyristors and Triacs	
SC04	Small-signal Transistors Member 199	
SC05	Low-frequency Power Transistors and	
	Hybrid IC Power Modules	
SC06	High-voltage and Switching	
	NPN Power Transistors	
SC07	Small-signal Field-effect Transistors	
SC08a	RF Power Bipolar Transistors	
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SC15	Microwave Transistors	
SC16	Wideband Hybrid IC Modules	
SC17	Semiconductor Sensors	
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PC01	High-power Klystrons and Accessories	
PC06	Circulators and Isolators	

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Our sister product division, Philips Components, also has a comprehensive data handbook system to support their products. Their data handbook titles are listed here.

Display components of annual langue-lisma

Book Title

DC01	Colour Display Components Colour TV Picture Tubes and Assemblies Colour Monitor Tube Assemblies	
DC02	Monochrome Monitor Tubes and Deflection Units	
DC03	Television Tuners, Coaxial Aerial Input Assemblies	
DC05	Flyback Transformers, Mains Transformers a	1
	General-purpose FXC Assemblies	
Magne	etic products and STERROT polibuloni	
MA01	Soft Ferrites Telephone Te	
MA03	Piezoelectric Ceramics	
MA04	Dry-reed Switches	
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PA01	Electrolytic Capacitors	
PA02	Varistors, Thermistors and Sensors	
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PA06	Ceramic Capacitors	
PA07	Quartz Crystals for Special and Industrial	

PA08 Fixed Resistors all assembles and applications

Quartz Crystals for Automotive and Standard

Plumbicon Camera Tubes and Accessories

Vidicon and Newvicon Camera Tubes and

Applications

Applications

Professional components

PA11

PC04

PC05

PC07

PC08

PC12

Quartz Oscillators

Photo Multipliers

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